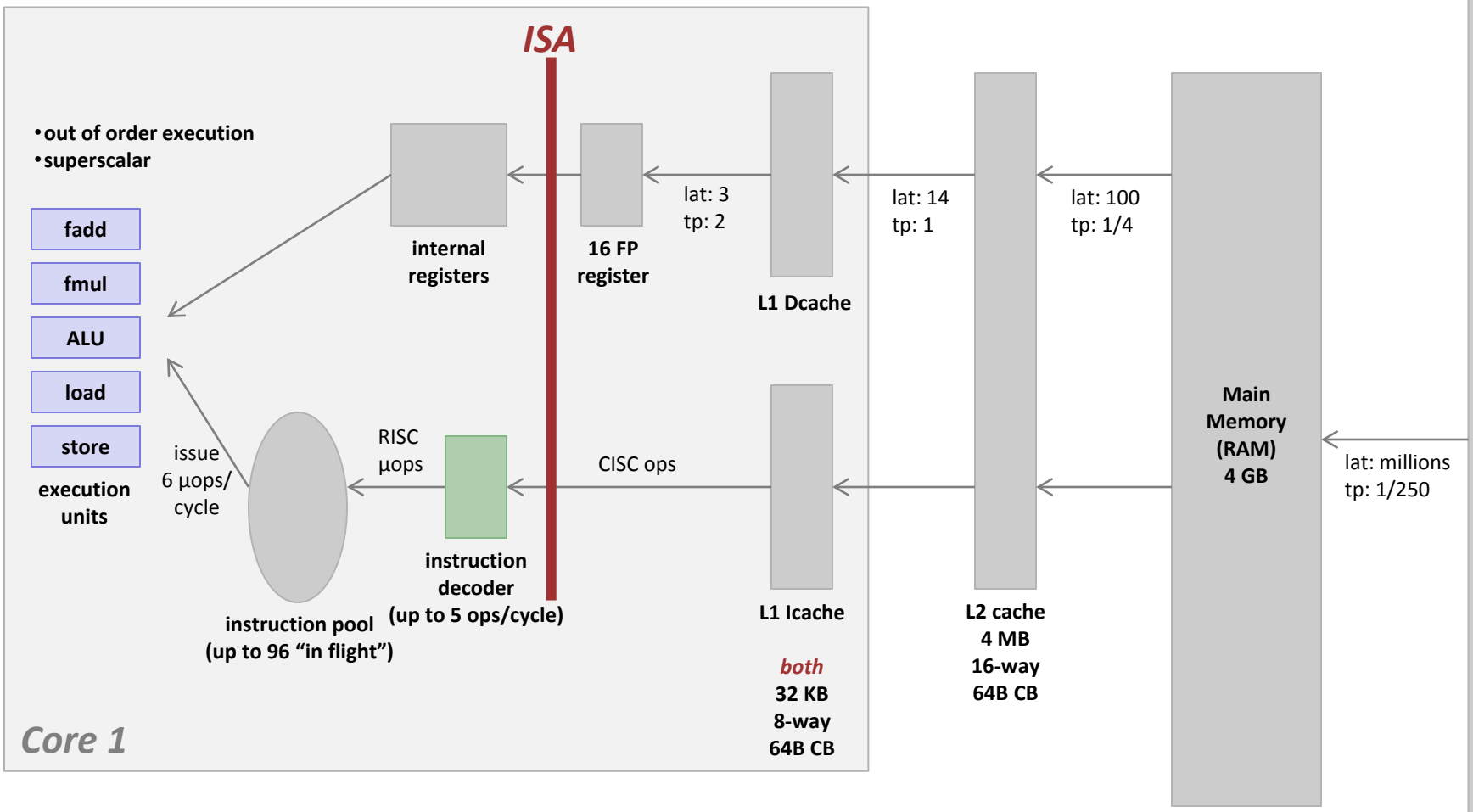
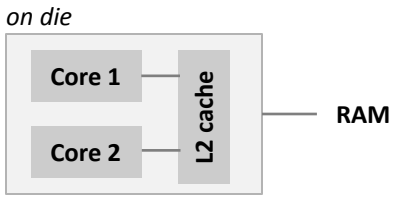
Abstracted Microarchitecture: Example Core (2008)

Throughput is measured in doubles/cycle
Latency in cycles for one double
1 double = 8 bytes
Rectangles not to scale



Core 2 Duo:



Memory hierarchy:

- Registers
- L1 cache
- L2 cache
- Main memory
- Hard disk