Abstracted Microarchitecture: Example Core

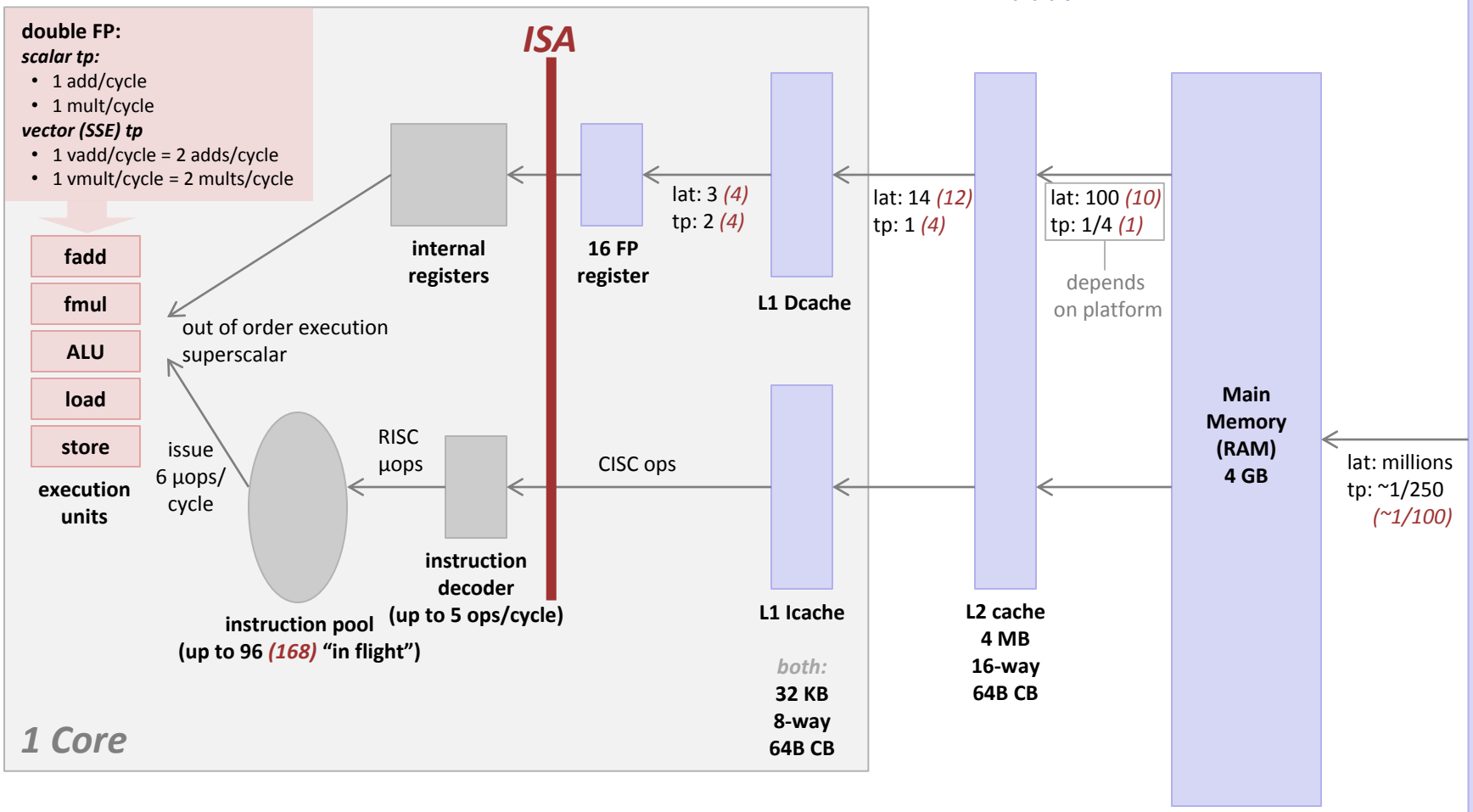
Throughput (tp) is measured in doubles/cycle. For example: 2 *(4)*
Latency (lat) is measured in cycles
1 double floating point (FP) = 8 bytes
Rectangles not to scale

Core 2 (2008)

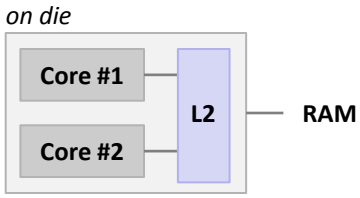
Core i7 Sandy Bridge (2011)

Memory hierarchy:

- Registers
- L1 cache
- L2 cache
- Main memory
- Hard disk



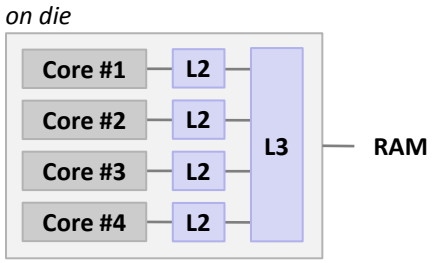
Core 2 Duo:



Core i7 Sandy Bridge:

256 KB L2 cache
2–8MB L3 cache: lat 26-31, tp 4
vector (AVX) tp

- 1 vadd/cycle = 4 adds/cycle
- 1 vmult/cycle = 4 mults/cycle



Source: Intel