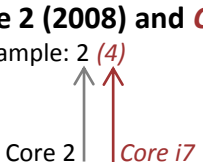


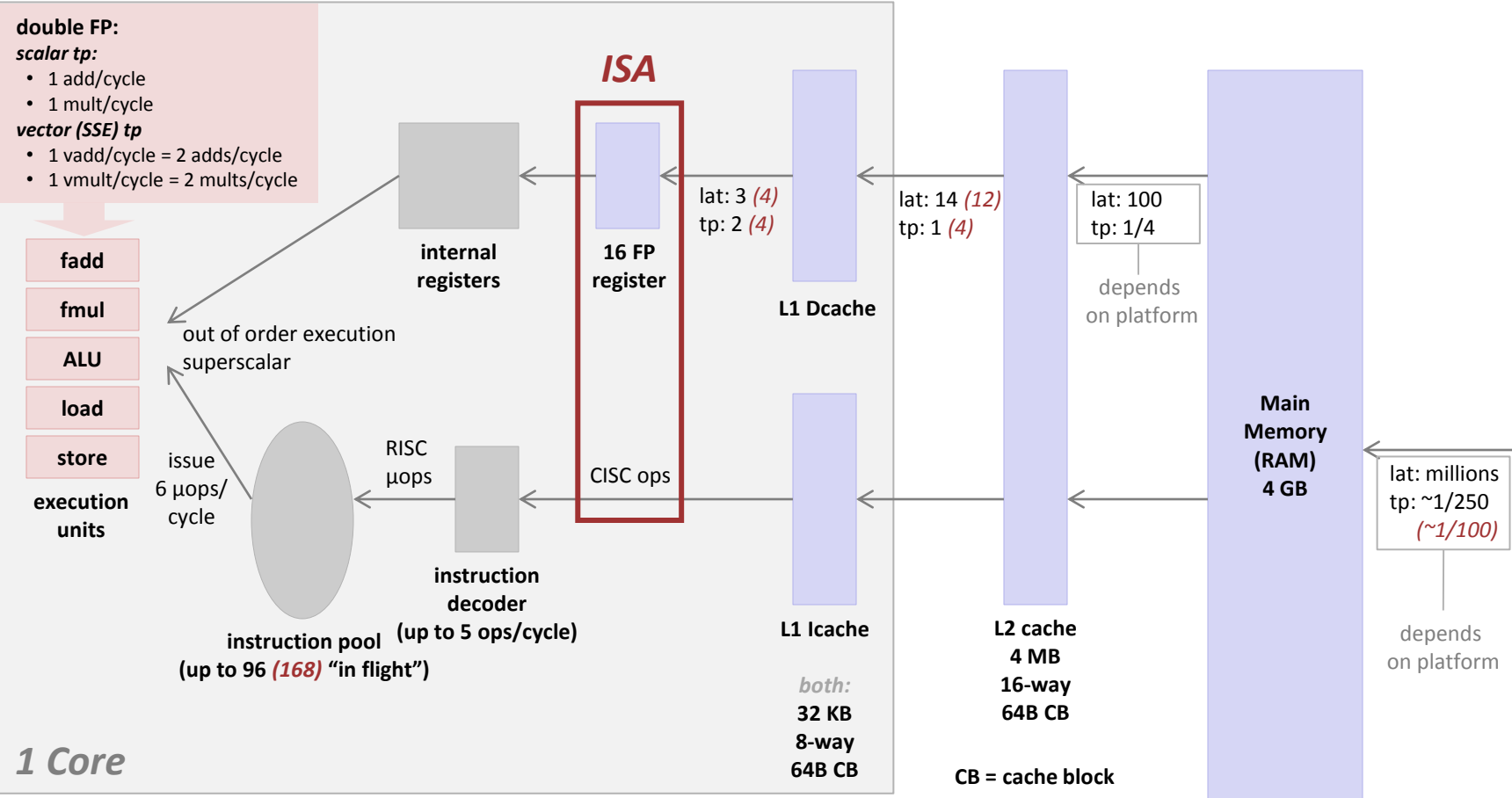
Abstracted Microarchitecture: Example Core 2 (2008) and Core i7 Sandybridge (2011)

Throughput (tp) is measured in doubles/cycle. For example: 2 (4)
 Latency (lat) is measured in cycles
 1 double floating point (FP) = 8 bytes
 Rectangles not to scale

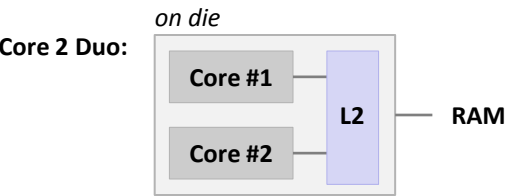


Memory hierarchy:

- Registers
- L1 cache
- L2 cache
- Main memory
- Hard disk

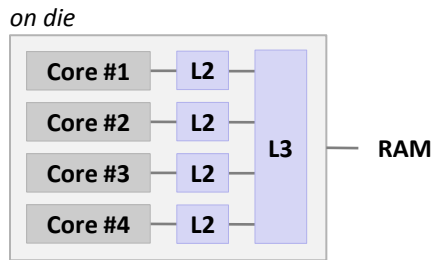


1 Core



Core i7 Sandy Bridge:

256 KB L2 cache
 2-8MB L3 cache: lat 26-31, tp 4
 RAM: tp 1
 vector (AVX) tp
 • 1 vadd/cycle = 4 adds/cycle
 • 1 vmult/cycle = 4 mults/cycle



Source: Intel manual (chapter 2)