MUHSEN OWAIDA

Curriculum Vitae

Post-Doctoral Researcher

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EDUCATION

- *October 2008 –September 2012:* PhD, Department of computer & communication engineering, University of Thessaly, Volos, Greece.

  Dissertation: "Using a Parallel Programming Model for Architectural Synthesis".

- *March 2006 - June 2008:* Master of Science, Department of computer & communication engineering, University of Thessaly, Volos, Greece.

  MSc. Thesis: "Design of High Performance and low power Hardware Architecture for the Transform & Quantization Stages in H.264".

- *September 1999 - July 2004* (5 years program)*:* Electrical Engineering Bachelor, Department of Electrical Engineering, Birzeit University, Birzeit, Palestine.

  Diploma thesis: "Design & Simulation of a Beamforming Array Antenna Applied for Radar Systems".

RESEARCH INTERESTS

My main research area is FPGA-based computing and data processing, covering four topics: CPU-FPGA system integration environments, data processing FPGA kernels design, high level synthesis, and novel FPGA architectures.

- ***CPU-FPGA system integration environment.*** The lack of standard architectural and software interfaces for FPGA processing engines is a serious challenge for efforts toward integrating FPGAs in Datacenters. The architectural and software interfaces will provide a unified model for talking to different processing engines on the FPGA fabric from users application software. In addition to standard interfaces, a middleware that manages FPGA

processing resources through sharing them among multiple tenants, and scheduling different compute-kernels to different processing engines is necessary. Currently, I work on developing and exploring such architectural and software interfaces and middleware for CPU-FPGA shared memory platforms.

- ***Implementation of Data Processing kernels on FPGA.*** An integral part for enabling FPGA computing for a large base of software developers is to provide libraries of FPGA kernels together with programming interfaces much like optimized libraries for GPUs and many-core processors. In my research I am focusing on data analytics, data mining and machine learning kernels. One of my research objectives here is to find out common compute and I/O kernels across a broad range of algorithms in data mining and machine learning and expose them as a library of basic functions for applications developers to embed in their software. One area where I am applying this concept is in developing a FPGA data mining library for MonetDB column store database.

- ***High-Level Synthesis.*** An area where my research started is high-level synthesis. My PhD dissertation described techniques for automatically generating hardware accelerators form OpenCL kernels, which led to the development of the Silicon-OpenCL (SOpenCL) toolset. My research was motivated by the observation that for FPGAs to be seamlessly integrated in a heterogeneous platform, they need to be programmed by parallel programming models already used by software engineers.

  My research addressed a variety of problems in automatic hardware generation:

  - Regular hardware generation by developing templates for hardware accelerators. The use of templates allowed capturing the specific features of the application (like parallelism levels, computation patterns, memory and data dependencies, etc.) and customizing the generated hardware components to meet area/performance requirements.
  - Automatic custom instructions generation to capture regular computation patterns. Such computational patterns allowed customization of the application accelerator and led to improved performance and minimized resources cost.
  - Resources scheduling and binding.

Currently, my interest in high-level synthesis moving toward automatic composition of complex processing engines from a library of coarse grain building blocks starting from higher abstraction level such as domain specific languages for machine learning. This approach is more promising and in line with efforts to develop a CPU-FPGA integrated system and programming environment.

- ***Novel FPGA Architectures.*** Another interesting research topic for me is exploring new novel reconfigurable architectures that will better meet the new demands for performance and ease of programmability. Either inventing new FPGA logic elements at fine granularity or looking into new domain specific coarse grain reconfigurable architectures (CGRAs) is an exciting way to develop innovative architectures for future FPGAs. Looking into different scenarios of how the FPGA and CPU fabrics can come closer and mingle with each other is another nice path to innovate new customizable processors.

PUBLICATIONS

2017

- **Accelerating Pattern Matching Queries in Hybrid CPU-FPGA Architectures**, D. Sidler, Zs. Istvan, M. Owaida, G. Alonso, to appear in SIGMOD 2017.

2016

- **FPRESSO: Enabling Express Transistor-Level Exploration of FPGA Architectures**, G. Zgheib, M. Lortkipanidze, M. Owaida, D. Novo, P. Ienne, Proceedings of ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), February 2016, Monterey, USA.
- **Progressive generation of canonical sum of products using a SAT solver**, A Petkovska, A Mishchenko, D Novo, M Owaida, P Ienne, Proceedings of the 25th International Workshop on Logic and Synthesis (IWLS), June 2016, Austin, USA.
- **Off-chip bus power minimization using serialization with cache-based encoding**, K Mohammad, A Kabeer, TM Taha, M Owaida, M Washha, Microelectronics Journal, Vol. 54, pp. 138-149, August 2016.

2015

- **Improved carry chain mapping for the VTR flow**, A. Petkovska, G. Zgheib, D. Novo, M. Owaida, A. Mishchenko, P. Ienne, International Conference on Field Programmable Technology (FPT), December 2015, Queenstown, New Zealand.
- **FudgeFactor: Syntax-Guided Synthesis for Accurate RTL Error Localization and Correction**, A. Becker, D. Maksimovic, D. Novo, M. Ewaida, A. G Haifa Verification Conference HVC, November 2015, Haifa, Israel.
- **Automatic support for multi-module parallelism from computational patterns**, N. George, H.J. Lee, D. Novo, M. Owaida, D. Andrews, K. Olukotun, P. Ienne, 25th International Conference on Field Programmable Logic and Applications (FPL), September 2015, London, UK.
- **Enhancing design space exploration by extending CPU/GPU specifications onto FPGAs**, M. Owaida, G. Falcao, J. Andrade, C. Antonopoulos, N. Bellas, Madhura Purnaprajna, D. Novo, G. Karakonstantis, A. Burg, P. Ienne, ACM Transactions on Embedded Computing Systems (TECS), Vol. 14(2), 2015.
- **Exploring Automatically Generated Platforms in High Performance FPGAs**, P Skrimponis, G Zindros, I Parnassos, M Owaida, N Bellas, P Ienne, Proceedings of International Conference on Parallel Computing (ParCo), September 2015, Edinburg, Irland.

2014

- **On the characterization of OpenCL dwarfs on fixed and reconfigurable platforms**, K. Krommydas, W. Feng, M. Owaida, C. Antonopoulos, N. Bellas IEEE 25th International Conference on Application-specific Systems, Architectures and Processors (ASAP), June 2014, Zurich, Switzerland.

- **A grammar induction method for clustering of operations in complex FPGA designs**, M. Owaida, C. Antonopoulos, N. Bellas, IEEE 22nd Annual Symbosuim on Field-Programmable Custom Computing Machines (FCCM), May 2014, Boston, USA.

2013

- **On the portability of the OpenCL dwarfs on fixed and reconfigurable parallel platforms**, K. Krommydas, M. Owaida, C. Antonopoulos, N. Bellas, W. Feng, International Conference on Parallel and Distributed Systems (ICPADS), December 2013, Seoul, Korea.

2012

- **Shortening design time through multiplatform simulations with a portable OpenCL golden-model: the LDPC decoder case**, G. Falcao, M. Owaida, D. Novo, M. Purnaprajna, N. Bellas, C. Antonopoulos, IEEE 20th Annual Symposium on Field-Programmable Custom Computing Machines (FCCM), April 2012, Toronto, Canada.

2011

- **Massively parallel programming models used as hardware description languages: the OpenCL case**, M. Owaida, N. Bellas, C. Antonopoulos, K. Daloukas, C. Antoniadis, Proceedings of the International Conference on Computer-Aided Design (ICCAD), September 2011, San jose, USA.
- **Implementation and performance comparison of the motion compensation kernel of the AVS video decoder on FPGA, GPU and multicore processors**, M. Owaida, N. Bellas, C. Antonopoulos, K. Daloukas, C. Antoniadis, IEEE 19th Annual Symposium on Field-Programmable Custom Computing Machines (FCCM), April 2011, Salt Lake City, USA.
- **Synthesis of platform architectures from OpenCL programs**, M. Owaida, N. Bellas, K. Daloukas, C. Antonopoulos IEEE 19th Annual Symposium on Field-Programmable Custom Computing Machines (FCCM), April 2011, Salt Lake City, USA.

2009

- **A high performance and low power hardware architecture for the transform & quantization stages in H. 264**, M. Owaida, M. Koziri, I. Katsavounidis, G. Stamoulis, International Conference on Multimedia and Expo (ICME), June 2009, New York, USA.

ACADEMIC EXPERIENCE

- **ETHZ:** *Post-Doctoral Researcher:*
  - 01/12/2015 – Present: Working at the Systems Group as a Post-doctoral researcher. My research involves developing FPGA architecture and software for integrating FPGAs with a database engine such as MonetDB. In addition, implementing and developing FPGA libraries for data analytics, data mining operators to be integrated in the database engine.

- ***EPFL:*** *Post-Doctoral Researcher:*
  - 01/09/2014 – 30/11/2015: Working at Processor Architecture Laboratory (LAP) as a Post-doctoral researcher involved in the research of current PhD students, and exploring new research venues.
- ***Birzeit University:*** *Assistant Professor*
  - *7/9/2013 – 20/8/2014: Teaching Fall Semester at the Department of Computer Systems Engineering.* Courses include: Digital Systems Design, Advanced Numerical Methods for Computing Science Master program. Real Time Systems Lab, and Digital Electronics Lab.
- ***University of Thessaly:*** *Research Visit*
  - *5/7/2013 – 6/9/2013:* Post Doctoral Research at the SCoRPIO project of IRETETH/CERTH.

    My research activity focused on two aspects:

    a. Developing an FPGA to desktop system interface using the PCI Express (PCIe). The system will be used to plug-and-play applications hardware accelerators.

    b. Designing and implementing algorithms for instruction clustering for FPGA high level synthesis. Here I work on extending my PhD work in generating applications specific instructions clusters, by looking into pattern recognition based techniques searching for regular computation patterns, instead of using a grammar-based algorithm.
- ***Birzeit University:*** *Assistant Professor*
  - *15/1/2013 – 3/6/2013:* Teaching Spring Semester at the Department of Computer Systems Engineering. Courses I taught include:
    - Digital Systems Design. This is a sophomore class with 35 students.
    - Computer Organization. This is a junior class with 54 students.
    - Digital Design Laboratory. This is a junior class with 16 students.
    - Computer Design Laboratory. This is a senior class with 16 students.
    - Mentoring diploma thesis.

    My duties include preparing course outline and lectures, teaching the class, and grading exams.
- ***University of Thessaly:*** *Teaching Assistant*: My duties include: assisting in testing experiments correctness and verifying experiments setup, and assisting students do and understand experiments.
  - *Spring 2011, Spring 2012:* Department of Computer & Communication Engineering
    - Embedded Systems Lab.
- ***Birzeit University:*** *Teaching Assistant*: My duties include: assisting in testing experiments correctness and verifying experiments setup, and assisting students do and understand experiments.
  - *Fall 2004 - Spring 2005:* Department of Mechanical Engineering
    - Control Systems Lab.
    - MATLAB Training Course.
  - *Fall 2005:* Department of Electrical Engineering

- Digital Design Lab.

SKILLS

Technical Skills

- Professional programming skills and fluent in C/C++ (e.g. over 50000 lines of C++ code in the SOpenCL tool).
- Programming in Java, Python, Perl.
- Knowledge and use of scripting languages (Bash scripts, JavaScript, HTML, CSS, PHP).
- Use of HDL languages (Verilog/VHDL) in large hardware designs.
- Familiarity with Unix/Linux and Windows operating systems.

Software and Tools

- Extensive knowledge and use of ModelSim, Altera Quartus, and Xilinx ISE tools for design verification and analysis. Use of Xilinx ChipScope for FPGA design debugging.
- Use of MATLAB tool for mathematical analysis and modeling.
- Use of Synopsys Design Compiler tool for custom design generation, timing and power analysis.

PROJECTS

- Silicon-OpenCL Tool Development: University of Thessaly. 2008-2012.
- Design and Synthesis of high performance Chroma and Luma Pixels Motion Compensation Engine in the AVS Video standard: University of Thessaly. 2011.
- C++-Like language Compiler development. University of Thessaly. 2009.
- Design and Synthesis of high performance, low power H.264 video standard Quantization/Transformation module. University of Thessaly. 2007.
- Design of an ARM-based processor, representation and simulation in VHDL. University of Thessaly 2006.
- Analysis of various Latch circuits power consumption models. University of Thessaly 2006.

HONORS AND AWARDS

- Post Doctoral Research: IRETETH/CERTH. 5/7/2013 – 6/9/2013.
- Doctoral Studies Scholarship: Greek State Scholarships Foundation. 2008 - 2012.
- Postgraduate Studies Scholarship: University of Thessaly. 2006 - 2007.
- Outstanding Academic Performance Honor & Award: Birzeit University. 1999-2000, 2002, 2003. Granted for excellent outstanding student performance in courses.

FOREIGN LANGUAGES

- **Arabic:** Native tongue.
- **English:** Fluent.
- **Greek:** Fluent.