CLR-DRAM: A Low-Cost DRAM Architecture Enabling Dynamic Capacity-Latency Trade-off

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Motivation & Goal

- Workloads and systems have **varying** main memory capacity and latency demands.
- Existing commodity DRAM makes **static** capacity-latency trade-off at **design time**.
- Systems miss opportunities to improve performance by adapting to changes in main memory capacity and latency demands.

**Goal**: Design a low-cost DRAM architecture that can be **dynamically** configured to have high capacity or low latency at a fine granularity (i.e., at the granularity of a row).
**CLR-DRAM (Capacity-Latency-Reconfigurable DRAM):**
- A low cost DRAM architecture that enables a single DRAM row to *dynamically* switch between **max-capacity mode** or **high-performance mode**.

**Key Idea:**
*Dynamically* configure the connections between DRAM cells and sense amplifiers in the density-optimized open-bitline architecture.

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Open-bitline (Baseline) ➔ CLR-DRAM
CLR-DRAM (Capacity-Latency-Reconfigurable DRAM)

- **Max-capacity mode**

  - The same storage capacity as the conventional open-bitline architecture

- **High-performance mode**

  - Reduced latency and refresh overhead via coupled cell/SA operation

  *mimics the cell-to-SA connections as in the open-bitline architecture*
Key Results

- **DRAM Latency Reduction:**
  - Activation latency (tRCD) by 60.1%
  - Restoration latency (tRAS) by 64.2%
  - Precharge latency (tRP) by 46.4%
  - Write-recovery latency (tWR) by 35.2%

- **System-level Benefits:**
  - Performance improvement: 18.6%
  - DRAM energy reduction: 29.7%
  - DRAM refresh energy reduction: 66.1%

We hope that CLR-DRAM can be exploited to develop more flexible systems that can adapt to the diverse and changing DRAM capacity and latency demands of workloads.
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