

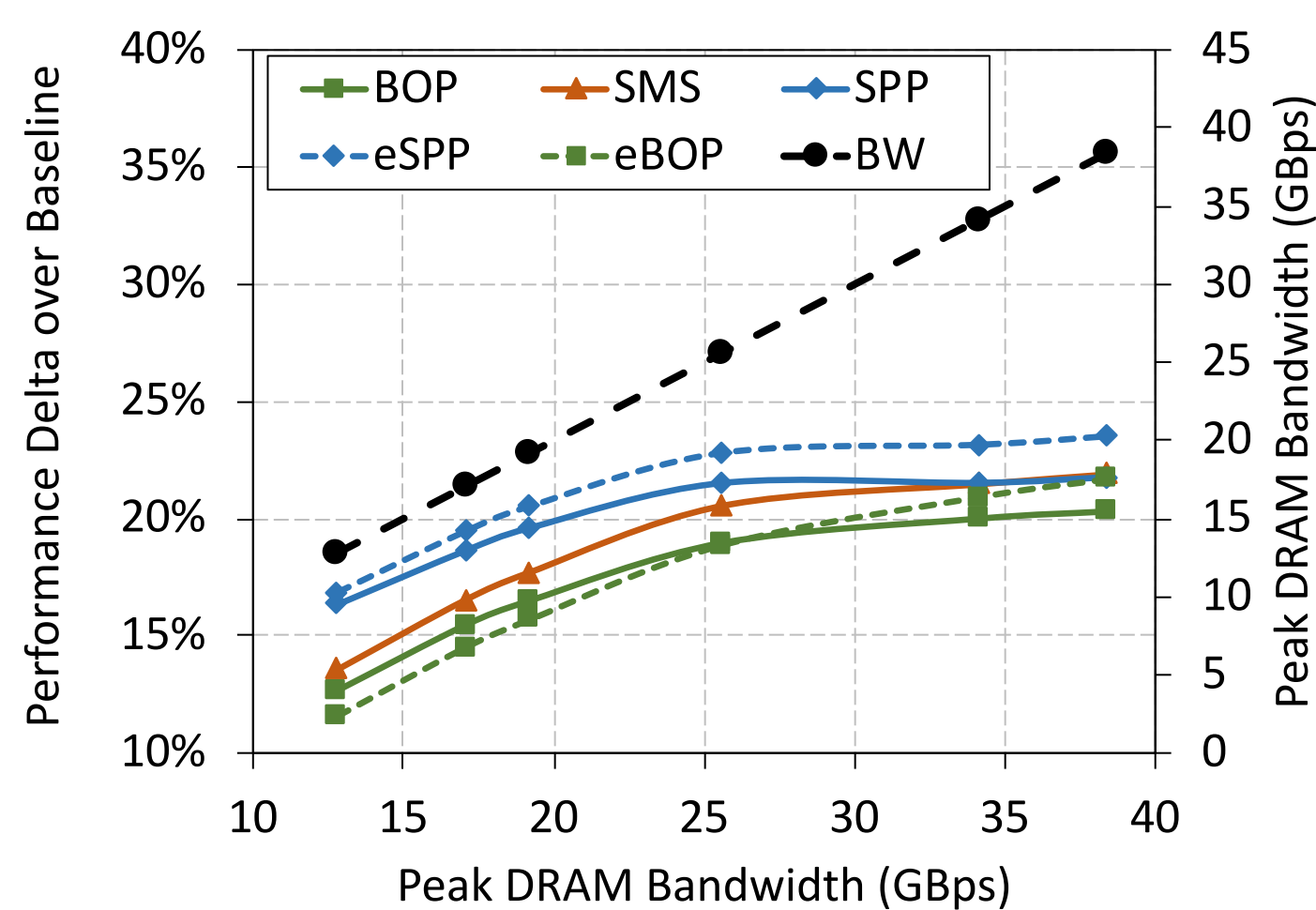
DSPatch: Dual Spatial Pattern Prefetcher

Rahul Bera* Anant V. Nori* Onur Mutlu+ Sreenivas Subramoney*

*Processor Architecture Research Lab (PARL),  Intel Labs +  SAFARI ETH Zürich

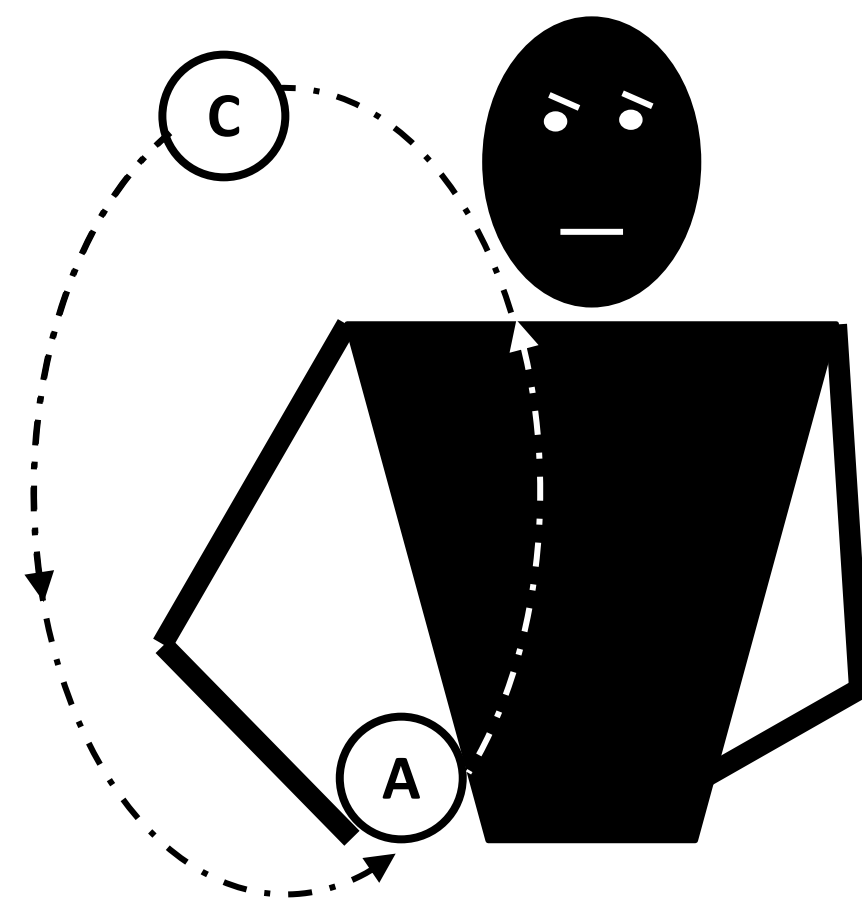
1. Motivation

- Current state-of-the-art spatial prefetcher performance plateaus despite increasing memory bandwidth
- ⇒ Need to boost speculation and coverage to maximize utilization of memory bandwidth resource



2. Challenge

- Fundamental tradeoff in traditional prefetcher design between **Coverage** versus **Accuracy**
- ⇒ Limits ability to dynamically adapt to memory bandwidth headroom and significantly **boost Coverage**



3. Goal

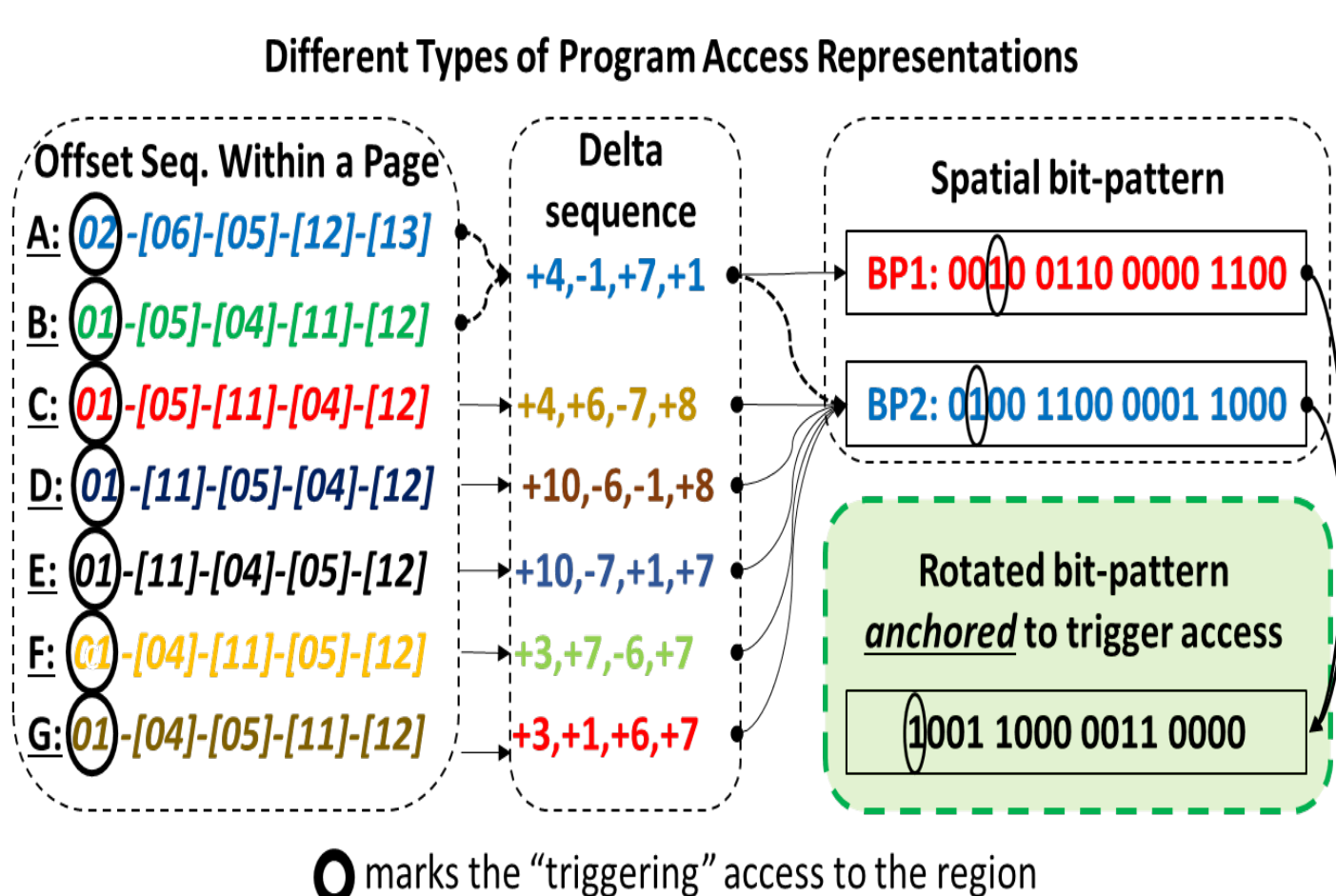
New prefetcher design should include:

- Pattern representations best suited to capture spatially co-located program accesses and **boost Coverage**
- Mechanisms to simultaneously optimize for **both Coverage and Accuracy**
- Ability to dynamically adjust aggressiveness (Coverage vs. Accuracy) based on available DRAM bandwidth

4. DSPatch Key Insights

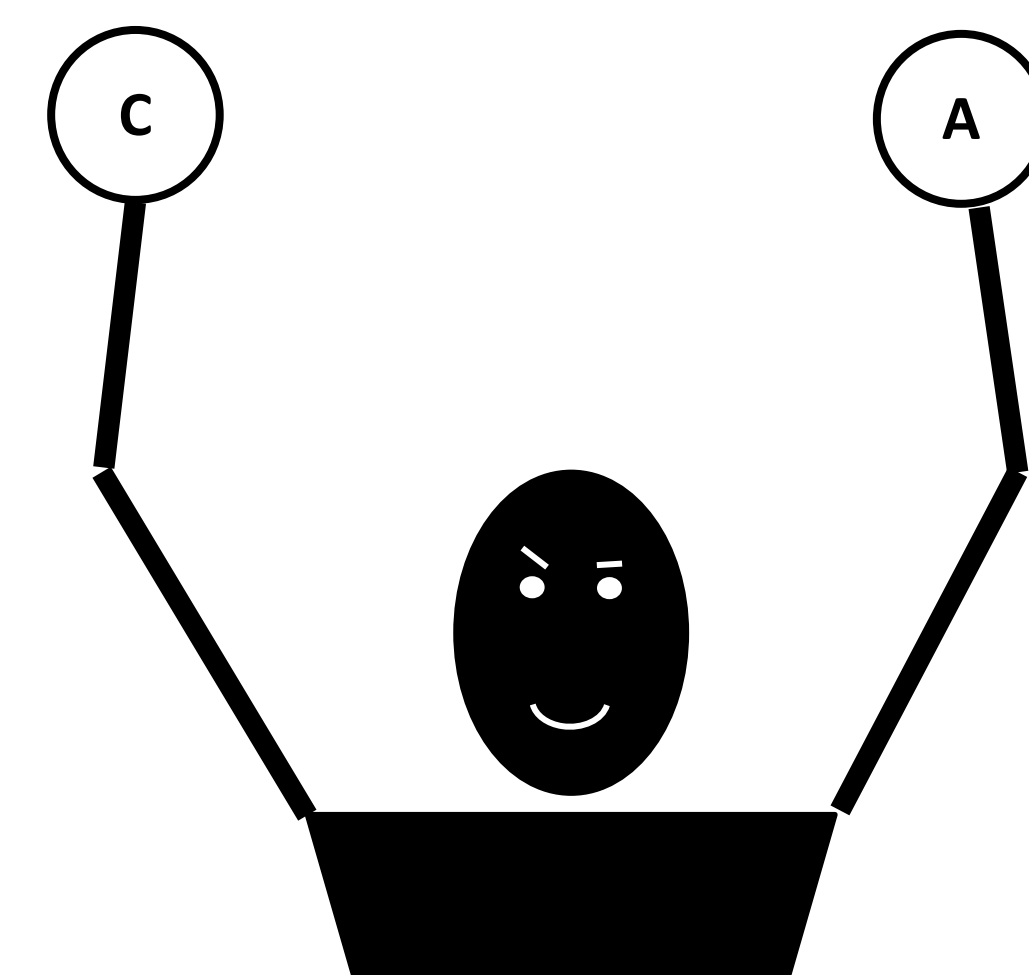
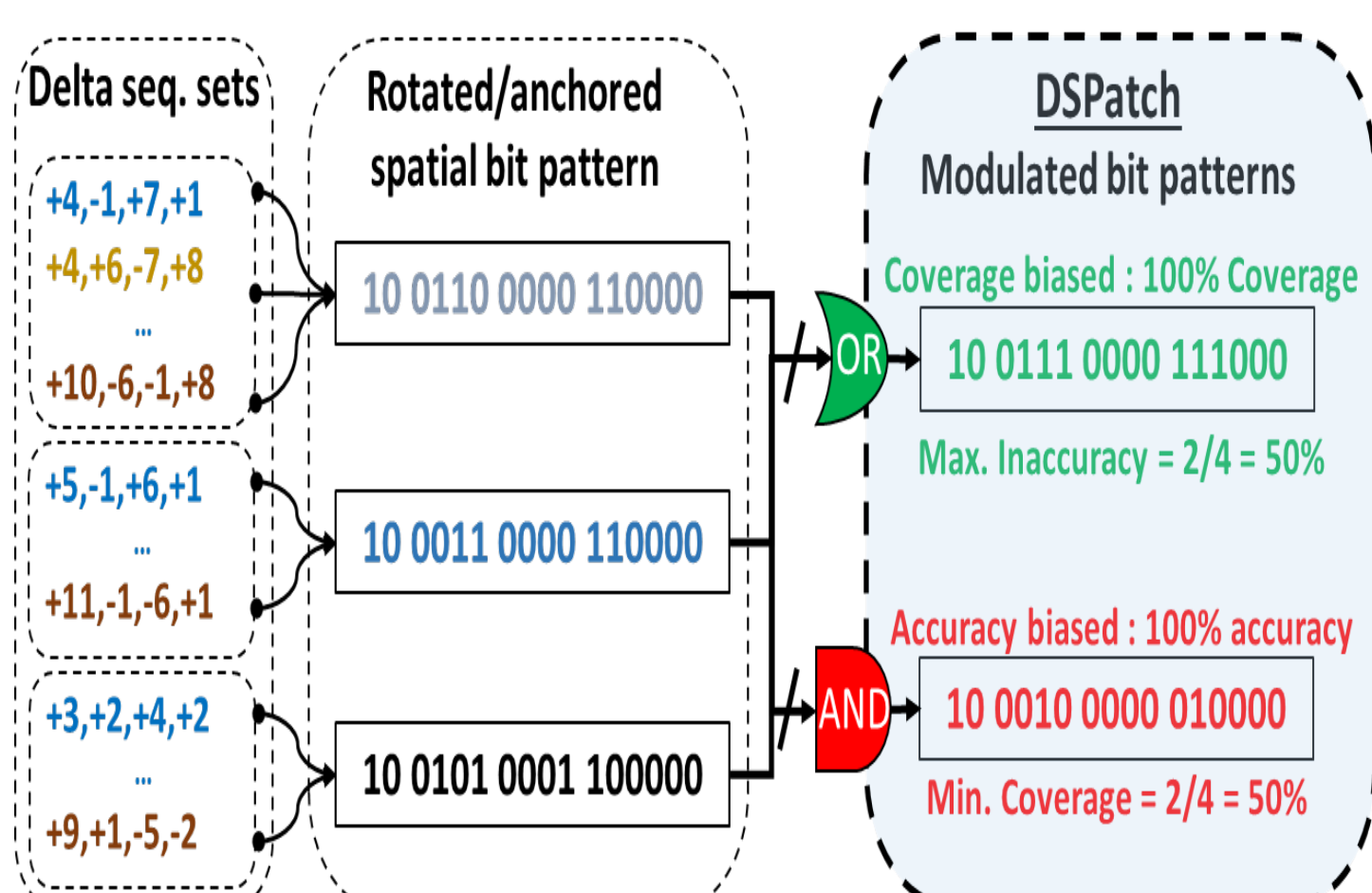
A **bit-pattern** representation, **rotated and anchored** to the first "triggering" access to a page, captures all spatially identical patterns subsuming any temporal variability.

⇒ Captures all "global deltas" from the trigger access



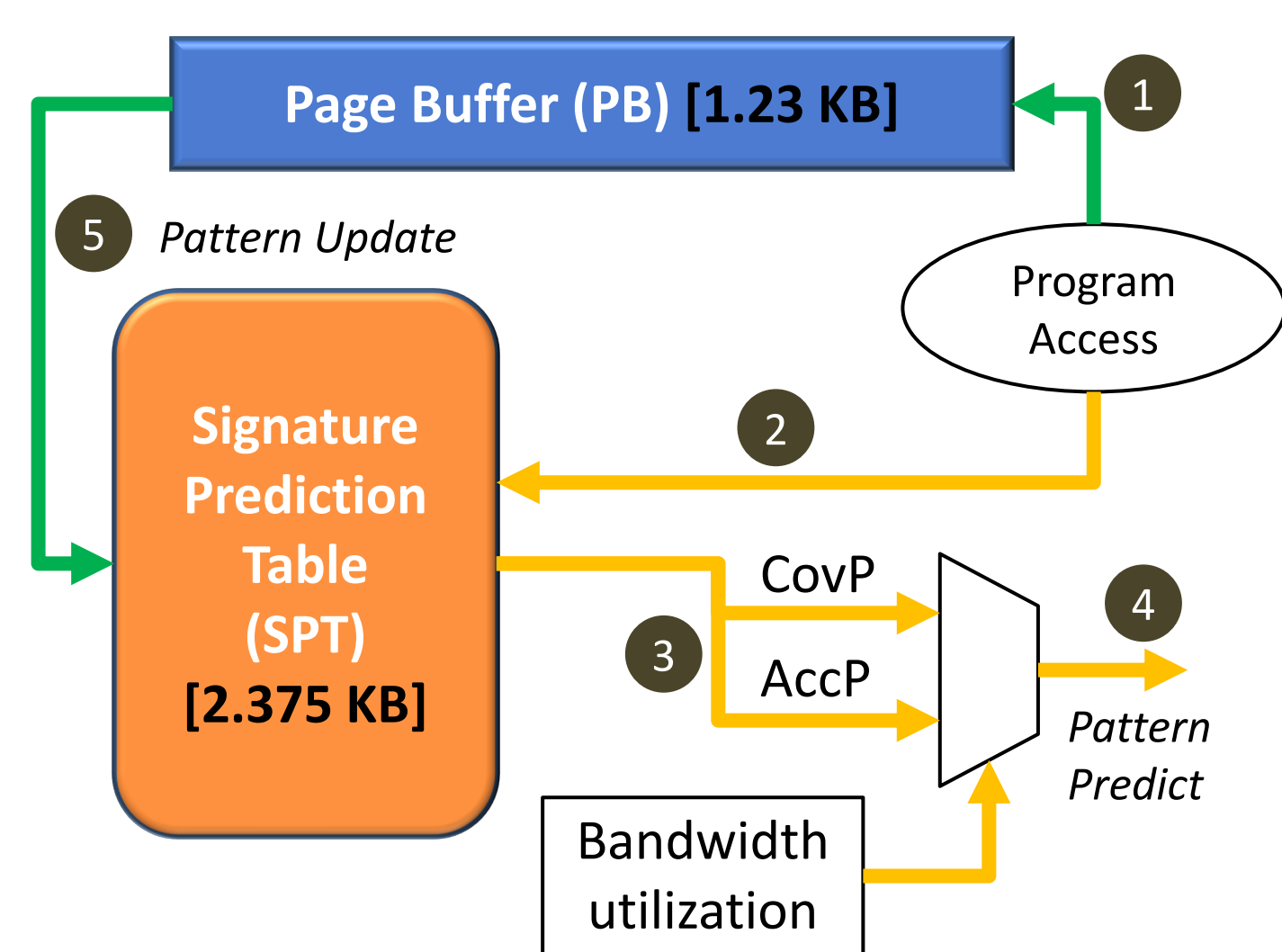
- Bit-wise **OR** of rotated bit-patterns adds missing bits to the pattern, biasing it towards **Coverage**
- Bit-wise **AND** of rotated bit-patterns keeps only repeating bits in the pattern, biasing it for **Accuracy**

Using **dual** modulated bit-patterns allows **DSPatch** to simultaneously optimize for **both Coverage and Accuracy**

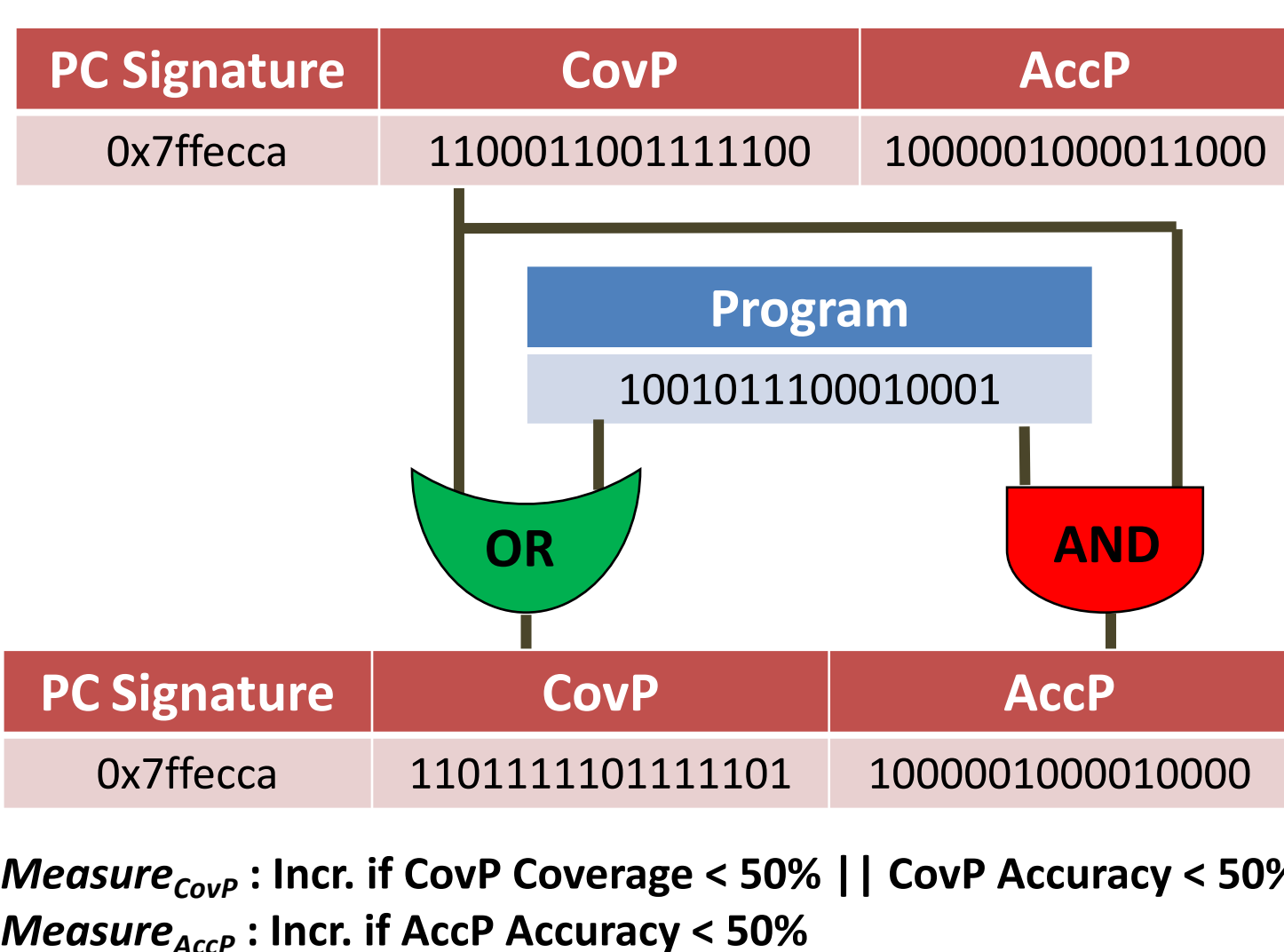


5. DSPatch Design

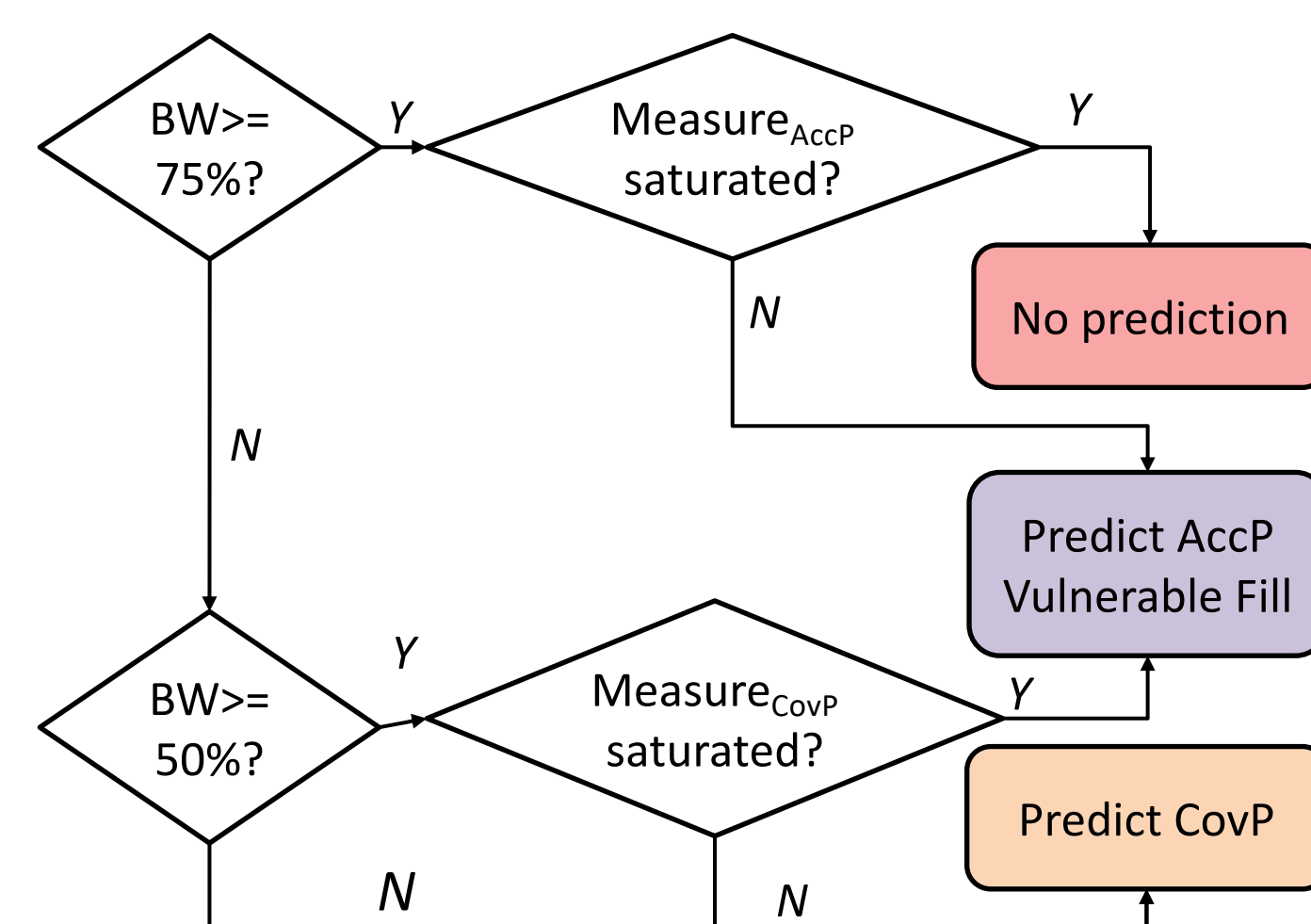
DSPatch: Overall Flow



DSPatch: Pattern Update

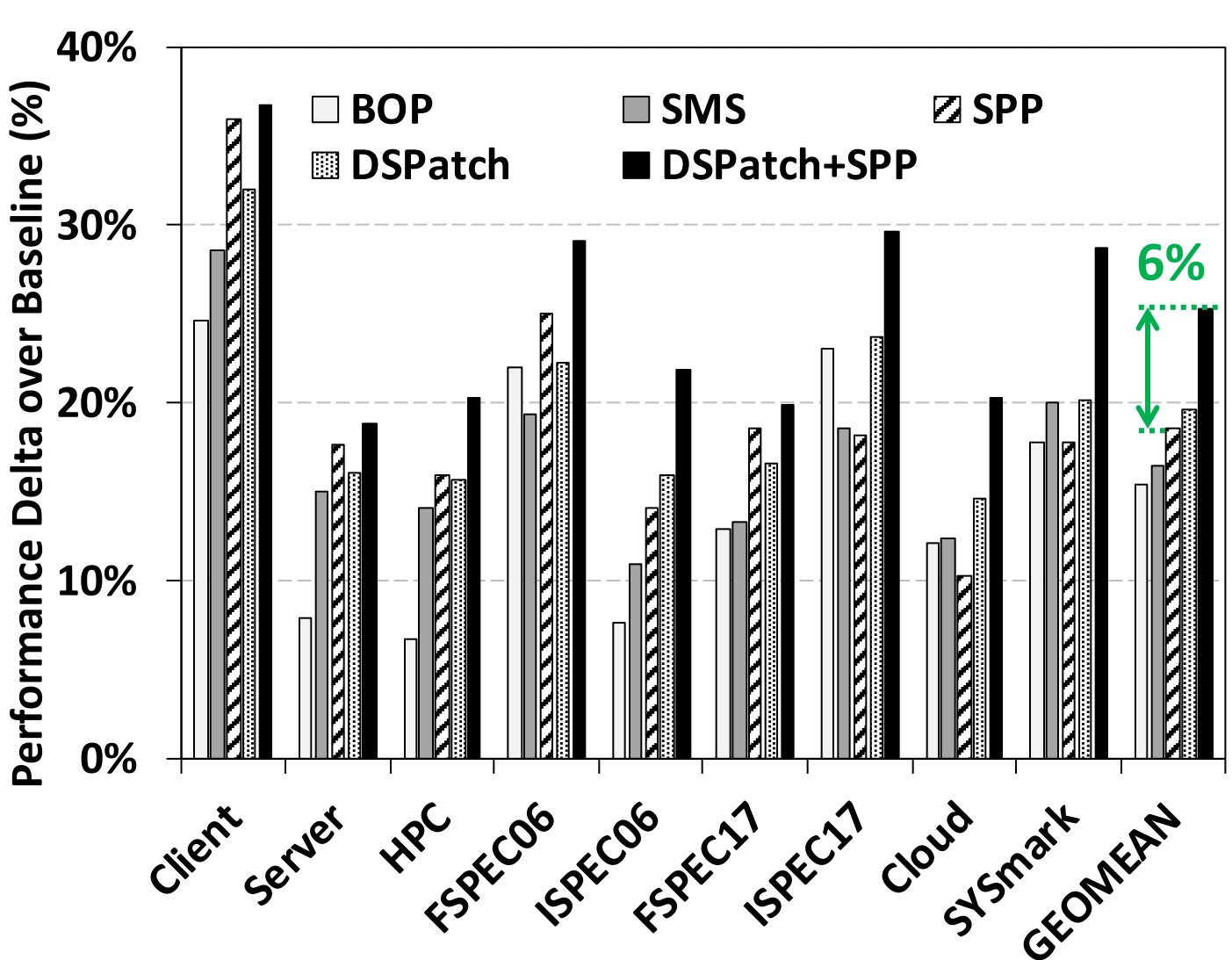


DSPatch: Pattern Predict

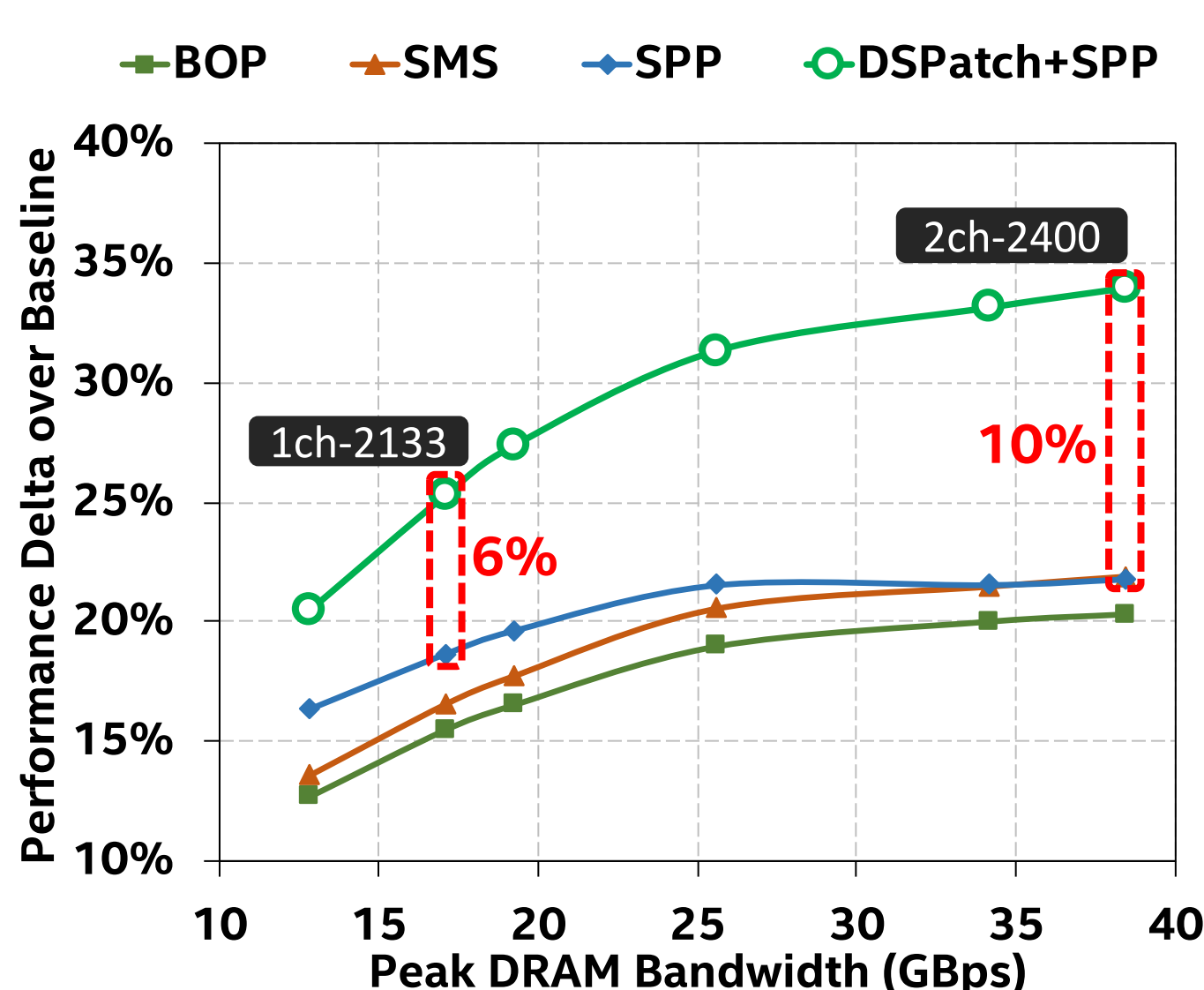


5. DSPatch Results

DSPatch: Single Core Performance



DSPatch: Single Core DRAM B/W Scaling



DSPatch: Multi-Core Performance

