

DarkGates: A Hybrid Power-Gating Architecture to Mitigate the Performance Impact of Dark-Silicon in High Performance Processors

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To reduce the leakage power of inactive (dark) silicon components, modern processor systems shut-off these components' power supply using low-leakage transistors, called power-gates. Unfortunately, power-gates increase the system's power-delivery impedance and voltage guardband, limiting the system's maximum attainable voltage (i.e., V_{max}) and, thus, the CPU core's maximum attainable frequency (i.e., F_{max}). As a result, systems that are performance constrained by the CPU frequency (i.e., F_{max} -constrained), such as high-end desktops, suffer significant performance loss due to power-gates.

To mitigate this performance loss, we propose DarkGates, a hybrid system architecture that increases the performance of F_{max} -constrained systems while fulfilling their power efficiency requirements. DarkGates is based on three key techniques: i) bypassing on-chip power-gates using package-level resources (called bypass mode), ii) extending power management firmware to support operation either in bypass mode or normal mode, and iii) introducing deeper idle power states.

We implement DarkGates on an Intel Skylake microprocessor for client devices and evaluate it using a wide variety of workloads. On a real 4-core Skylake system with integrated graphics, DarkGates improves the average performance of SPEC CPU2006 workloads across all thermal design power (TDP) levels (35W–91W) between 4.2% and 5.3%. DarkGates maintains the performance of 3DMark workloads for desktop systems with TDP greater than 45W while for a 35W-TDP (the lowest TDP) desktop it experiences only a 2% degradation. In addition, DarkGates fulfills the requirements of the ENERGY STAR and the Intel Ready Mode energy efficiency benchmarks of desktop systems.

1. Introduction

Due to the breakdown of Dennard scaling [1], the fraction of a silicon chip that can operate at the maximum attainable frequency (within a fixed power limit) reduces with each process generation [2, 3]. As a result, processor architects need to ensure that, at any point in time, a large fraction of a chip is effectively *dark* (i.e., idle) or *dimmed* (i.e., underclocked), which limits performance. To this end, architects clock-gate idle components to eliminate their dynamic power consumption or *power-gate* components to reduce their leakage power consumption and use the saved precious energy to power-up the necessary resources or increase their frequency.

As opposed to clock-gating, power-gating has a significant effect on a processor's architecture. A power-gate is implemented using area-hungry low-leakage transistors that can

shut off the voltage supply to a target idle circuitry. A power-gate's impedance should be as small as possible to reduce the voltage drop it causes when the target circuit is active, as the impedance has a direct impact on the circuit's supply voltage and power consumption. However, lowering the power-gate's impedance increases the power-gate's area cost. The area of such power gates is non-trivial as it grows as a function of the circuit area that is power-gated. For instance, the area of a low-impedance power-gate for a CPU core can lead to a significant increase (>5%) in the overall chip area [4–9]. Unfortunately, since there is a limited area budget for placing power-gates, it is impractical to minimize a power-gate's impedance and, thus, this impedance causes voltage drops on the power-delivery network. To cope with that, designers increase the voltage guardband, which results in increased power consumption when the system is active [10, 11]. This limits the maximum attainable voltage (i.e., V_{max}) and frequency (i.e., F_{max}) [12, 13], which can result in considerable performance loss for systems that are constrained by the maximum attainable CPU core frequency (i.e., F_{max} -constrained), such as high-end desktops (e.g., Intel Skylake-S [14–16]).

In this paper, we propose *DarkGates*, a hybrid power-gating architecture to increase the performance of F_{max} -constrained systems while satisfying their power efficiency requirements. DarkGates is based on *three* key techniques. First, DarkGates bypasses the power-gates of F_{max} -constrained processors at the *package* level by shorting gated and un-gated CPU core power-delivery domains. This enables the sharing of 1) the decoupling capacitors of the die (i.e., Metal Insulator Metal (MIM) [17]) and the package (i.e., decaps [18]), and 2) the package routing resources among CPU cores, resulting in lower voltage drops, and improving voltage/frequency (i.e., V/F) curves.¹ Second, DarkGates extends the power management firmware (e.g., Pcode [20]) algorithms to operate in two modes: 1) bypass mode, which increases the CPU cores' voltage and frequency, and 2) normal mode, which utilizes the power-gates to reduce leakage power of CPU cores. Third, DarkGates enables deeper system idle power states (i.e., package C-states) to reduce energy consumption once the entire processor is idle. For example, we include support for C8 package C-state [21, 22] to allow turning off most of the processor's components once

¹Intel processors are individually calibrated in the factory to operate on a specific voltage/frequency and operating-condition curve specified for the individual processor [19]. Reducing the voltage guardband increases the effective voltage, which allows the processor to operate at higher frequency for the same voltage level [12].

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the entire processor is idle, which reduces the average power consumption of energy-efficiency benchmarks.

We implement DarkGates on an Intel Skylake microprocessor² for client devices and evaluate it using a wide variety of SPEC CPU2006, graphics (3DMark), and energy efficiency workloads. On a 4-core Skylake processor with integrated graphics engines, DarkGates improves the performance of SPEC CPU2006 workloads by up to 8.1% (4.6% on average)³ for a 91W thermal design power (TDP) desktop system. DarkGates maintains the performance of 3DMark workloads for desktop systems with a TDP higher than 45W. For a 35W TDP (the lowest TDP) desktop, DarkGates degrades performance by only 2%. In addition, DarkGates fulfills the ENERGY STAR (energy efficiency standard [28, 29]), the Intel Ready Mode Technology (RMT [30, 31]) energy efficiency benchmarks' requirements.

This work makes the following **contributions**:

- To our knowledge, DarkGates is the first work that provides a hybrid power-gating architecture to increase the performance of systems that are constrained by the maximum attainable CPU core frequency (i.e., F_{max} -constrained), such as high-end desktops.
- We present the implementation of DarkGates on the Intel Skylake microprocessor for client devices, showing the three key techniques required to realize DarkGates and their overhead.
- We perform an experimental evaluation of DarkGates on a real 4-core Intel Skylake system and clearly establish DarkGates' performance and energy benefits over a baseline system without it.

2. Background

We provide brief background on the architecture, power delivery networks, and design limits in modern client processors such as Intel Skylake [23, 32], Kaby Lake [24], Coffee Lake [25], and Cannon Lake [26].

2.1. Client Processor Architecture

A high-end client processor is a system-on-chip (SoC) that typically integrates three main domains into a single chip: 1) compute (e.g., CPU cores and graphics engines), 2) IO, and 3) memory system. Fig. 1(a) shows the architecture used in recent Intel processors (e.g., Skylake [23, 33, 34], Coffee Lake [25], and Cannon Lake [26]) with a focus on CPU cores.

Power Management. The processor includes one central power management unit (PMU) and one local PMU per CPU core. The central PMU is responsible for several power-management activities, such as dynamic voltage and frequency

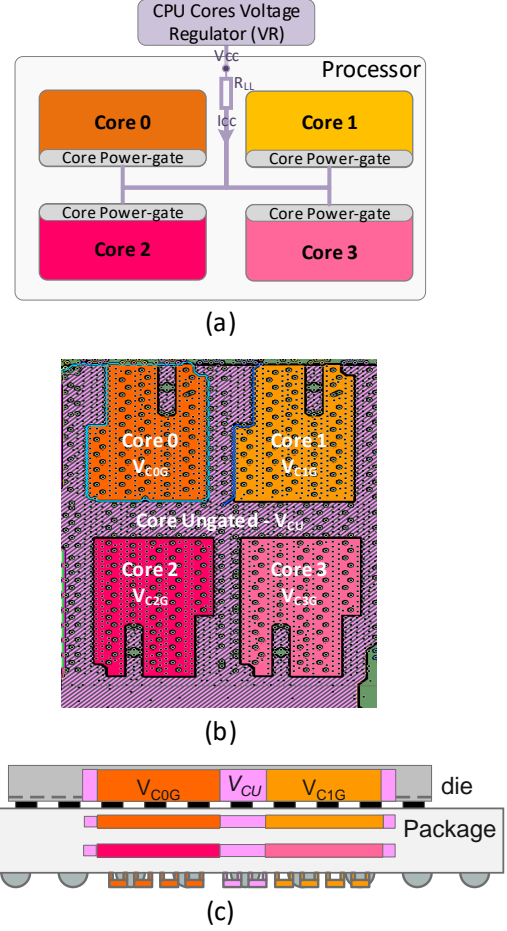


Figure 1: (a) Architecture overview of recent Intel client processors. All cores share the same voltage regulator (VR). Each CPU core has a power-gate (PG) for the entire core. (b) Package layout showing an ungated main voltage domain (V_{CU}) arriving from the CPU core VR that feeds four power-gated voltage domains (one for each CPU core, V_{C0G} , V_{C1G} , V_{C2G} , and V_{C3G}). (c) Side view of die and package showing 1) the ungated main voltage domain (V_{CU}) and two cores' voltage domains (V_{C0G} and V_{C1G}), and 2) the package's decoupling capacitors [18].

scaling (DVFS) [22, 35–37]. The central PMU has several interfaces to on-chip and off-chip components, such as to 1) the motherboard voltage regulator (VR), i.e., serial voltage identification (SVID) [20, 22, 38, 39], to control the voltage level of the VR, 2) the phase-locked-loop, to control the clock frequency, and 3) each core's local PMU, to communicate power management commands and status report. The local PMU inside the CPU core is responsible for core-specific power management, such as clock gating, power gating control, and thermal reporting.

Clocking. A phase-locked loop (PLL) supplies the clock signal to all CPU cores. All CPU cores have the same maximum clock frequency [40–43].⁴

Power Gating. Power gating is a circuit-level technique to significantly reduce the leakage power of an idle circuit [10, 20, 22].

²Intel Skylake [23] shares its microarchitecture with multiple processors in 2015–2020, such as Kaby Lake [24], Coffee Lake [25], Cannon Lake [26].

³The performance gains of DarkGates are significant in highly-optimized systems like the Intel Skylake. It is important to note that all new microarchitectural optimizations (e.g., improvements in pipelining, branch prediction, and memory subsystem) in Skylake generated a 2.4% average performance improvement [27] over Broadwell (one generation older than Skylake) and 5.7% over Haswell (two generations older than Skylake) [27].

⁴Typically, Intel client processors that use fully-integrated voltage regulator (FIVR) power delivery, including Haswell and Ice Lake processors, have the same clock frequency domain for all cores [41, 44].

A power-gate is implemented using low-leakage transistors that shut off the input voltage to the target circuit and comes with a *power-area tradeoff*. A power-gate needs to be large enough to help reduce 1) the power delivery impedance (R), 2) the voltage drop (i.e., IR drop), and 3) the operating voltage and power consumption of the target circuit when it is active. However, a power-gate for a large circuit (e.g., a CPU core) can consume significant chip area [4–9]. A power-gate may involve an additional trade-off between leakage power consumption reduction and performance loss due to the latency to ungate the circuit (i.e., to open the power gate). Typically, the wake-up latency from the power-gated state can take a handful to tens of cycles [20, 45]. However, to reduce the worst-case peak in-rush current [46–49] and voltage noise of power-delivery (e.g., di/dt noise [20, 22, 50]) when waking up a power-gate, the power-gate controller applies a *staggered* wake-up technique [48] that takes tens of nanoseconds (typically, 10–20ns) [45, 51, 52].

Power Budget Management (PBM). To keep the system running below a thermal design power (TDP) limit, the SoC PMU employs a *power budget management (PBM)* algorithm to dynamically distribute the total power budget to each SoC domain [36–38, 53–60]. This allows each domain to operate within its allocated power budget. For instance, CPU cores and graphics engines in the compute domain share the same power budget. When a graphics-intensive workload is executed, the graphics engines consume most of the compute domain’s power budget.

To keep the power consumption of the compute domain within its allocated power budget, the PMU applies DVFS to 1) reduce the CPU cores’ power consumption and 2) increase the graphics engines’ performance [38, 39, 54, 61].

System Idle Power States (C-states). The Advanced Configuration and Power Interface (ACPI)⁵ defines a processor’s *idle power states*, commonly called *C-states* [62]. C-states are defined in two primary levels: 1) the component level, such as thread (TCi), core (CCi), and graphics (RCi) C-states, and 2) the system level, known as *package C-states* (PCi or Ci) [21, 22].

A package C-state defines an idle power state of the system (consisting of the processor, chipset, and external memory devices). A system enters a specific package C-state depending on each system component’s idle power state (*component C-state*). Various levels of package C-states exist to provide a range of power consumption levels with various techniques, such as clock gating at the uncore level or a nearly complete shutdown of the system. The ACPI standard includes recommendations on the C-states, but manufacturers are free to define their C-states and the corresponding system behavior at each C-state. In this work, we focus on the package C-states of the Intel Skylake architecture [21], but similar idle power state definitions exist in other architectures (e.g., AMD [63] and ARM [64]). Table 1 shows all package C-states of the Intel Skylake architecture and the major conditions under which the

Table 1: Package C-states in the Intel Skylake mobile SoC.

Package C-state	Major conditions to enter the package C-state
C0	One or more cores or graphics engine executing instructions
C2	All cores in CC3 (clocks off) or deeper and graphics engine in RC6 (power-gated). DRAM is active .
C3	All cores in CC3 or deeper and graphics engine in RC6. Last-Level-Cache (LLC) may be flushed and turned off, DRAM in self-refresh , most IO and memory domain clocks are gated, some IPs and IOs can be active (e.g., DC and Display IO).
C6	All cores in CC6 (power-gated) or deeper and graphics engine in RC6. LLC may be flushed and turned off, DRAM in self-refresh , IO and memory domain clocks generators are turned off. Some IPs and IOs can be active (e.g., video decoder (VD) and display controller (DC)).
C7	Same as Package C6 while some of the IO and memory domain voltages are power-gated . CPU core VR is ON .
C8	Same as Package C7 with additional power-gating in the IO and memory domains. CPU core VR is OFF .
C9	Same as Package C8 while all IPs must be off. Most voltage regulators’ voltages are reduced. The display panel can be in panel self-refresh (PSR) [65, 66].
C10	Same as Package C9 while all SoC VRs (except state always-on VR) are off. The display panel is off.

power management unit (PMU) places the system into each package C-state (a similar table exists in the Intel manual [21]).

Typical *desktop* systems based on processors prior to Intel Skylake (e.g., Haswell [31, 67] or Broadwell [68]) support up to *package C7*, while mobile systems (e.g., Haswell-ULT [69] or Broadwell-ULX [70]) support up to *C10*.

2.2. Client Processor Packages and Die Sharing

Architects of modern client processors typically build a *single* CPU core (with a built-in power-gate) architecture⁶ that supports *all* dies of a client processor family, and some of the dies are used to build different processor packages targeting different segments. For example, the Intel Skylake processor for high-end *mobile* (i.e., Skylake-H [72]) and high-end *desktop* (i.e., Skylake-S [14]) processors uses a single processor die [55, 73, 74] for all TDP ranges (from 35W [75] to 91W [76]). Recent AMD client processors use a similar strategy [77–82]. This design reuse is adopted for two major reasons. First, doing so allows system manufacturers to configure a processor for a specific segment using two main methods: 1) by configuring processor’s TDP (known as configurable TDP [83–85] or cTDP) to enable the processor to operate at higher or lower performance levels, depending on the available cooling capacity and desired power consumption of the system and 2) by integrating one or more dies (e.g., CPU dies, chipset, and embedded-DRAM) into a single package that is optimized for a specific market segment. For example, a land grid array (LGA [86]) package is used for desktops while a ball grid array (BGA [87]) package is used for laptops. Second, it reduces non-recurring engineering (NRE [88]) cost and design complexity to allow competitive

⁵ACPI is an industry standard that is widely used for OS-directed configuration, power management, and thermal management of computing systems.

⁶An Intel CPU core has nearly the same microarchitecture for client and server processors. Intel CPU core design is a single development project, leading to a master superset core. Each project has two derivatives, one for server and one for client processors [71].

product prices and enable the meeting of strict time-to-market requirements.

2.3. Power Delivery Network (PDN)

There are three commonly-used PDNs in recent high-end client processors [60, 89]: motherboard voltage regulators (MBVR) [33, 37, 90, 91], integrated voltage regulators (IVR) [77–80, 92, 93], and low dropout voltage regulators (LDO) [17, 41, 74, 94]. We describe aspects of the MBVR PDN here due to its simplicity. As shown in Fig. 1(a), the MBVR PDN of a high-end client processor includes 1) one motherboard voltage regulator (VR) for all CPU cores, 2) a load-line impedance (R_{LL}), and 3) power-gates for each individual core.⁷ All CPU cores share the same VR [33, 37, 43, 90, 91]. For more details on state-of-the-art PDNs, we refer the reader to our recent prior work [60].

Load-line. Load-line or *adaptive voltage positioning* [97–100] is a model that describes the voltage and current relationship⁸ under a given system impedance, denoted by R_{LL} . Fig. 2(a) describes a simplified power delivery network (PDN) model with a voltage regulator (VR), load-line (R_{LL}), and load (CPU Cores). R_{LL} is typically $1.6m\Omega$ – $2.4m\Omega$ for recent client processors [40, 60]. The voltage at the load is defined as $V_{CCload} = V_{CC} - R_{LL} \times I_{CC}$, where V_{CC} and I_{CC} are the voltage and current at the VR output, respectively, as shown in Fig. 2(b). From this equation, we can observe that the voltage at the load input (V_{CCload}) decreases when the load’s current (I_{CC}) increases. Due to this phenomenon, the PMU increases the input voltage (V_{CC}), i.e., applies a *voltage guardband*, to a level that keeps the voltage at the load (V_{CCload}) above the minimum functional voltage (i.e., V_{CCmin}) under even the most intensive load (i.e., when all active cores are running a workload that exercises the highest possible dynamic capacitance (C_{dyn})). This workload is known as a *power-virus* [60, 104, 105] and results in the maximum possible current ($I_{CCvirus}$). A typical application consumes a lower current $I_{CCtypical}$ than $I_{CCvirus}$. The minimal current that the processor can consume is the leakage current (I_{CClk}) once the clocks are gated (while the supply voltage is *not* power-gated). In all cases where the current is lower than $I_{CCvirus}$, the voltage drop (i.e., $R_{LL} \times I_{CC}$) is smaller than when running a power-virus, which results in a higher load voltage V_{CCload} than necessary (as shown in Fig. 2(b)), leading to a power loss that increases quadratically with the voltage level.

Adaptive Voltage Guardband, I_{CCmax} , and V_{CCmax} . To reduce the power loss resulting from a high voltage guardband when *not* running a power-virus, due to the load-line effect, modern processors define *multiple levels* of power-viruses depending on the maximum dynamic capacitance (C_{dyn}) that a system state (e.g., number of active cores and the computational intensity of running instructions) can draw. For each power-virus level, the processor applies a *differ-*

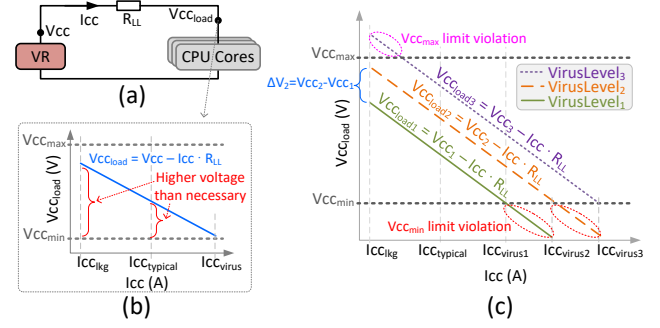


Figure 2: Adaptive voltage guardband on modern processors. (a) Simplified Power Delivery Network (PDN) model with a load-line. (b) Voltage at the load is defined as: $V_{CCload} = V_{CC} - R_{LL} \times I_{CC}$, where V_{CC} and I_{CC} are the voltage and current at the VR output, respectively. (c) Multi-level load-line with three power-virus levels. The voltage guardband is adjusted based on the power-virus level corresponding to the system state of the processor (e.g., number of active cores and instructions’ computational intensity).

ent voltage guardband. Fig. 2(c) illustrates the load-line model behavior of a processor with three power-virus levels denoted by $VirusLevel_1$, $VirusLevel_2$, and $VirusLevel_3$ (where $VirusLevel_1 < VirusLevel_2 < VirusLevel_3$). The three power-virus levels represent multiple scenarios. For example, $VirusLevel_1$, $VirusLevel_2$, and $VirusLevel_3$ can represent one, two, and four active cores, respectively, for a processor with four cores. When the processor moves from one power-virus level to a higher/lower level, the processor increases/decreases the voltage by a voltage guardband (ΔV). For example, when moving from $VirusLevel_1$ to $VirusLevel_2$, the processor increases the voltage by ΔV_2 as shown (in blue text) in Fig. 2(c).

2.4. Processor Design Limits

2.4.1. Thermal Limits. We describe the most important thermal limits that constrain the performance of modern processors.

Junction Temperature (T_{jmax}) Limit. As the processor dissipates power, the temperature of the silicon junction (T_j) increases. T_j should be kept below the maximum junction temperature (T_{jmax}) as overheating may cause permanent damage to the processor. The processor measures the temperature and applies multiple techniques (e.g., PBM [53], thermal throttling [22], and catastrophic trip temperature [20]) to ensure that the temperature remains under the T_{jmax} limit. In the worst case, the processor automatically shuts down when the silicon junction temperature reaches its operating limit [22, 39, 43, 98, 106].

Thermal Design Power (TDP). TDP (in watts) is the maximum sustainable power consumption under the maximum theoretical load (e.g., common applications, but not a power-virus) that the cooling solution of the system needs to be designed for [22, 58, 83, 84, 107, 108].

2.4.2. Power Delivery Network (PDN) Limits. There are multiple PDN limits in a modern processor. We describe the most important ones.

⁷Fine-grained power-gates exist in a CPU core. For example, a power-gate is implemented in each AVX unit (e.g., AVX512 [95, 96]) inside a CPU core.

⁸In this model, short current bursts result in voltage droops [12, 101, 102], which are filtered out by the decoupling capacitors [103], while long current bursts are detected by the motherboard VR.

VR Thermal Design Current (TDC). TDC is the the continuous load current, also known as maximum continuous current, thermal current, or second power limit (i.e., PL2 [39]). TDC is the sustained current that the processor is capable of drawing indefinitely and defines the current to use for VR temperature assessment. In other words, TDC is the maximum amount of electrical current the VR must be able to supply while being thermally viable [19, 79, 109].

Power Supply and Battery Maximum Current Limit. The power supply unit (e.g., ATX power supply [110] or power brick [39]) and/or device battery that supply current to the system VRs also have current limits. For example, the third power limit (i.e., PL3) is used for battery over-current protection [39].

VR Electrical Design Current (EDC) Limit. The power delivery of a modern processor is limited by EDC, also known as the maximum instantaneous current, peak current, $I_{cc_{max}}$, or fourth power limit (i.e., PL4 [39]). EDC is the maximum amount of current at any instantaneous short period of time that can be delivered by a motherboard VR or an integrated VR (e.g., FIVR [17]). EDC limit is typically imposed by the limited maximum current that the VRs can supply [17, 20, 22, 98, 111, 112]. Exceeding the EDC limit can result in irreversible damage to the VR or the processor chip, or tripping the VR’s protection mechanism for excessive current that shuts down the system. Therefore, a combination of *proactive* enforcement and platform design constraints must be used to prevent system failure [17, 20, 22, 98, 109, 111–115].

Maximum Current per Bump/Pin. The amount of current that a processor’s die/package can consume per voltage domain is limited by the maximum current a bump/pin can support [113–115]. For example, while integrated VRs mitigate the EDC limit by enabling a reduced input current for the processor [60], the maximum current of the processor can be limited by the maximum current for a bump/pin.

Minimum Operating Voltage Limit (V_{min}). Operating below the V_{min} limit can cause a processor to malfunction. Therefore, modern processors implement multiple techniques to prevent the voltage from dropping below $V_{cc_{min}}$ due to, for example, di/dt voltage fluctuations [20, 22, 101, 102, 116–118].

Maximum Operational Voltage Limit (V_{max}). Technology scaling has made modern integrated circuits more susceptible to reliability degradation phenomena such as Negative Bias Temperature Instability (NBTI), Electromigration (EM), and Time Dependent Dielectric Breakdown (TDDB) [119]. Degradation depends on many processes and environmental factors, but can be controlled by managing the circuit’s temperature and voltage levels [120]. Processor manufacturers define a maximum operational voltage limit (V_{max}) that should not be exceeded to ensure the guaranteed processor lifespan and reliability. For example, Intel allows exceeding V_{max} when overclocking a system (e.g., via the BIOS [121] or the XTU tool [106]). This process is out of the processor’s reliability specification and can shorten the processor’s lifespan [98, 106, 121].

Voltage Droop Effect on Maximum Frequency (F_{max}). In an active CPU core, simultaneous operations in memory and/or

logic circuits demand high current flow, which creates fast transient voltage droops from the nominal voltage (V_{nom}). The worst-case voltage droop can degrade the maximum attainable frequency at a given voltage since this requires additional voltage (droop) guardband (V_{gb}) above the nominal voltage to enable the CPU core to run at the target frequency. If the core voltage with the voltage guardband becomes higher than V_{max} (i.e., $V_{nom} + V_{gb} > V_{max}$), the power management unit reduces F_{max} , thereby reducing V_{nom} to keep the CPU core voltage below V_{max} . Therefore, voltage guardband (V_{gb}) has a direct effect on the CPU core F_{max} .

3. Motivation

We conduct experiments on two different system setups to clearly motivate the productization of DarkGates.

Our first setup is a real Intel Broadwell processor [94], the previous generation of our target Skylake processor [55]. We configure the Broadwell processor to four Thermal Design Power (TDP) levels and frequencies using post-silicon configuration tools (see Sec. 6). In this experiment, we reduce the voltage guardband of the CPU cores by 100mV, allowing the power budget management algorithm (PBM, see Sec. 2.1) to increase the CPU cores’ frequency for a given voltage while keeping the system power consumption below TDP and the voltage below the maximum operating voltage limit (V_{max}). The goal of this experiment is to evaluate the potential performance benefits of increasing CPU core clock frequency as we increase the effective voltage by reducing the voltage guardband. In this experiment, we run the SPEC CPU2006 benchmarks, both floating-point (fp) and integer (int) with base (single-core) and rate (all cores) modes [122].

Our second experimental setup is based on an in-house power delivery network simulator (see Sec. 6) that aims to evaluate the maximum possible reduction in system impedance when we bypass the power-gates.

We make two key observations from these experiments:

Observation 1. Reducing the voltage guardband (e.g., IR drop compensation) increases the effective voltage, which allows increasing the processor frequency with a negligible increase in power consumption.

Fig. 3 plots the performance impact of increasing the CPU core frequency of an Intel Broadwell system, which is enabled by increasing the effective voltage as a result of reducing the voltage guardband by 100mV. We gather our results using SPEC CPU2006 benchmarks for four TDP levels.

We make five key observations from Fig. 3. First, the average performance of SPECfp and SPECint benchmarks increases (by 6–10%) as the frequency of the system increases for each given TDP level. Second, the system can run at a higher frequency with the same CPU core voltage level *without* exceeding the TDP limit since the effective voltage increases once we reduce the voltage guardband. Third, the performance of high-TDP (i.e., 95W) configurations increases even though these systems are typically limited by V_{max} (i.e., F_{max} -constrained) since the effective V_{max} voltage increases once we reduce the voltage guardband. Fourth, the lower the TDP, the higher the

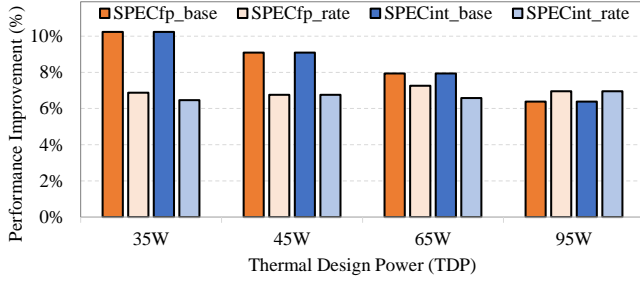


Figure 3: Average performance improvement of floating-point SPEC CPU2006 (floating-point (fp) and integer (int) benchmarks with base (single-core) and rate (all-cores) modes) when we increase the CPU core frequency, which is enabled by increasing the effective voltage as a result of reducing the voltage guardband by 100mV.

performance gain of the SPEC benchmarks in the base (i.e., single-core) mode. This is because the relative increase of frequency in steps of 100MHz granularity until reaching the TDP limit is higher as the TDP (and baseline frequency) level is lower. Fifth, the high TDP (i.e., 95W) performance gain of the SPEC benchmarks in the rate (i.e., all-cores) mode is higher than that in the base mode. This is because we can increase the frequency of all cores to the maximum attainable frequency corresponding to the improved V_{max} (due to the reduced the voltage guardband) without exceeding the TDP level since these systems are typically V_{max} limited.

We conclude that reducing the voltage guardband can significantly improve the performance of both thermally-limited systems (e.g., 35W TDP) and F_{max} -constrained systems (e.g., 95W TDP), based on experiments on real Intel Broadwell systems.

Observation 2. While power-gating is an effective technique to reduce leakage power of idle CPU cores, we observe that power-gates can significantly increase system impedance, which increases voltage drop (e.g., resistive voltage drop, IR drop), thereby requiring higher voltage guardbands to compensate for the higher voltage drop. Fig. 4 shows the impedance-frequency profile [123–125] of two simulated Intel Skylake systems: 1) one that uses power-gates (red) and 2) another that bypasses the power-gates (blue). The system that uses the power-gates has approximately 2× the impedance of a system that bypasses the power-gates. Therefore, a system that uses the power-gates requires approximately 2× the voltage guardband of a system that bypasses the power-gates.

We conclude that bypassing the power-gates can reduce system impedance by approximately 2×, which allows reducing the voltage drop guardband by approximately 2×.

Summary. Our experimental results clearly demonstrate that modern desktop systems face a significant challenge against achieving their potential performance and TDP utilization due to the voltage drops on power gates. Even though these voltage drops are completely preventable (e.g., if power-gates are removed), they still exist in real desktop processors. This is because reusing the same processor die for a wide variety of systems (e.g., from mobile to desktop to server) with built-in

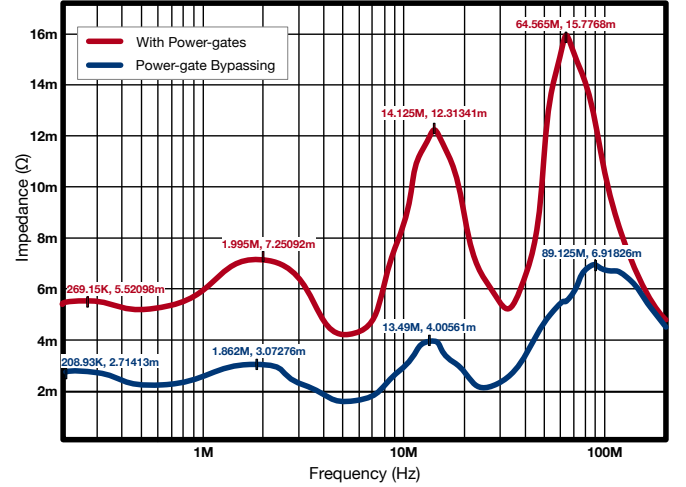


Figure 4: The impedance-frequency profile of a Skylake system that 1) uses power-gates (red) and 2) bypasses the power-gates (blue). The system that uses the power-gates has approximately 2× the impedance of a system that bypasses the power-gates.

power-gates configuration is economically preferable.

Based on our key observations, we conclude that a *hybrid power-gating approach* is necessary to mitigate the power-gating inefficiencies in current client processors. Our **goal** is to provide such an approach that 1) reduces the voltage guardband overhead of power-gates in high-performance systems (e.g., high-end desktops), 2) utilizes the reduced voltage guardband to increase the frequency of the CPU cores without increasing the baseline voltage or exceeding the TDP, and 3) provides low energy consumption for battery-operated systems (e.g., laptops) and meets the energy-efficiency benchmarks' requirements for desktop systems by reducing the leakage power consumption of idle cores.

4. DarkGates Architecture

Based on our experimental analyses, we propose *DarkGates*, a hybrid system architecture that increases the performance of F_{max} -constrained systems while fulfilling their power efficiency requirements.

We design DarkGates with two design goals in mind: 1) reduce CPU cores' power-delivery impedance, and, thus, voltage drop, to improve the V/F curve of high-end desktops, and 2) meet the energy efficiency requirements of desktop devices by enabling deeper package C-states.

DarkGates achieves these two goals with *three* key components. The *first component* of DarkGates is a *Power-gates Bypassing* technique that effectively bypasses the power-gates of F_{max} -constrained processors at the *package* level by shorting gated and un-gated CPU core power domains. This leads to 1) sharing of the decoupling capacitors of the die and package between CPU core, and 2) sharing of package routing resources between CPU cores, resulting in lower voltage drops. The result is improved voltage/frequency (i.e., V/F) curves.

The *second component* of DarkGates is the improved *power management firmware* that is responsible for extending the

power management algorithms to operate in two modes: 1) bypass mode, which increases the CPU core voltage and frequency by utilizing the improved V/F curves, and 2) normal mode, which utilizes the power-gates to reduce the leakage power of CPU cores.

The *third component* of DarkGates is a *new deep package C-state* for desktop systems that reduces energy consumption once the entire processor is idle. This leads to improved average power consumption for desktop energy-efficiency benchmarks.

The three components of DarkGates work together to increase the performance of F_{max} -constrained systems while fulfilling the energy efficiency requirements. We describe them in detail in the next three subsections.

4.1. Power-gate Bypassing

The DarkGates Power-gate Bypassing technique is responsible for reducing CPU cores' voltage drop in F_{max} -constrained systems (e.g., high-end desktops) by reducing system impedance. To do so, the technique uses the same Intel Skylake die to build 1) a dedicated package for Skylake-H (used for high-end mobile systems) with the power-gates enabled and 2) a dedicated package for Skylake-S (used for high-end desktop systems) that bypasses the power-gates, as shown in Fig. 5. This architecture is feasible since client processors typically share the same die between multiple mobile and desktop products. Specifically, the same die is used for both Intel Skylake high-end mobile systems (Skylake-H) and Skylake desktop systems (Skylake-S).⁹

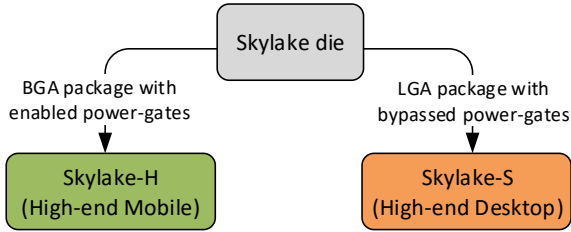


Figure 5: The DarkGates hybrid power-gating architecture uses the same Skylake die to build 1) a dedicated package for Skylake-H (used for high-end mobile systems) with the power-gates enabled and 2) a dedicated package for Skylake-S (used for high-end desktop systems) that bypasses the power-gates.

As shown in Fig. 6, the desktop package combines into a single voltage domain the five voltages used in the mobile package shown in Fig. 1 (i.e., the core ungated voltage domain (V_{CU}) and the per-core gated voltage domains, V_{C0G} , V_{C1G} , V_{C2G} , and V_{C3G}). To do so, the desktop package effectively shorts the *four* gated CPU cores' voltage domains and the ungated voltage domain into a single domain.

The single voltage domain architecture leads to 1) sharing of the decoupling capacitors of the die (i.e., Metal Insulator Metal (MIM) [17]) and package (i.e., decaps [18]) between CPU cores, and 2) sharing of package routing resources between CPU cores. This architecture results in reducing both resistive and inductive voltage drops [102, 126–128]. As discussed

in Sec. 2.4.2, reducing the voltage drop reduces the voltage guardband, which improves the voltage/frequency (i.e., V/F) curves. Improved V/F curves lead to a higher frequency (and, thus, performance) for F_{max} -constrained systems.

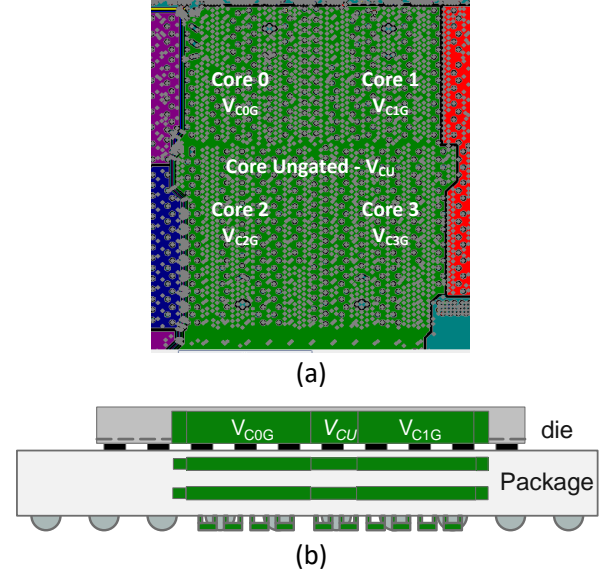


Figure 6: (a) Package layout of Skylake-S (high-end desktop) showing a single voltage domain for the cores (green), which combines the Core Ungated voltage domain (V_{CU}) and each of CPU core voltage domains, V_{C0G} , V_{C1G} , V_{C2G} , V_{C3G} . (b) Side view of die and package showing combined voltage domain in die, package's substrate, and package's decoupling capacitors.

4.2. Improved Power Management Algorithms

DarkGates architecture requires the adjustment of three main components inside the power management unit (PMU) firmware (i.e., Pcode [20]).

First, DarkGates requires the adjustment of DVFS firmware power management algorithms (e.g., P-state, Turbo) that enables the transition from one frequency/voltage operating point to another [36, 43]. Since Power-gate Bypassing (Sec. 4.1) improves the V/F curves (i.e., for a given voltage level, it increases the maximum attainable frequency), the DVFS algorithms should be adjusted to take into account the new V/F curves for desktop system¹⁰ by allowing the appropriate higher frequency at any given voltage level. In particular, these changes allow increasing the maximum attainable frequency (i.e., F_{max}) for systems that are limited by the maximum reliable voltage (i.e., V_{max}). An additional advantage of the improved V/F curves is that a CPU core can run at a given frequency with a lower voltage level, which reduces the processor power consumption in the active state.

Second, DarkGates requires adjustments in the power budget management algorithm (PBM) [37, 38, 53–58] (discussed in Sec. 2). In particular, in the DarkGates architecture, the PBM algorithm needs to take into account the additional power consumption due to the leakage of inactive cores (i.e., ungated

⁹Some of Skylake products even integrates an additional embedded DRAM die into the same processor package [55].

¹⁰The firmware (i.e., Pcode [20]) can recognize the target system (i.e., mobile vs. desktop) based on fuses available to the firmware.

idle CPU core), which can decrease the effective power budget that is allocated to the active cores and/or graphics engines. The reduced power budget can decrease the frequency of a thermally-limited compute domain.

Third, DarkGates can change the processor’s lifetime reliability [129–131] due to the additional power and temperature resulting from bypassing the power gates. On the one hand, DarkGates’s Power-gate Bypassing that combines cores’ otherwise separated voltage domains into a single voltage domain can improve the maximum current provided to each core since, with DarkGates, all bumps are shared between the cores, which alleviates the electromigration (EM) issues [131]. On the other hand, Power-gate Bypassing keeps cores powered-on in workloads where one or more cores are idle since these cores are normally power-gated in the baseline system (i.e., without DarkGates). Therefore, Power-gate Bypassing 1) increases the stress time of the CPU cores and 2) increases the junction temperature compared to baseline. As a result, DarkGates requires the adjustment of the reliability voltage guardband. Our reliability model shows that less than $5mV/20mV$ of *additional reliability voltage guardband* is required to compensate for the additional stress and temperature for $91W/35W$ (additional $\sim 5^\circ C$), respectively.

4.3. New Package C-state for Desktops

As discussed in Sec. 2.1, *desktop* systems in previous processor generations of Skylake support up to the *package C7* (defined in Table 1). For example, the deepest package C-state that Haswell [31, 67] and Broadwell [68] desktop systems support is package *C7*, while Haswell [69] and Broadwell [70] for mobile systems support up to *C10*. The difference in package C-state support between desktop and mobile is due to two major reasons. First, reducing energy consumption is critical for mobile systems to meet battery life requirements for representative benchmarks (e.g., video playback, web browsing, video conferencing, light gaming [132]), while it is less critical for a desktop system. Therefore, the main desktop energy-efficiency benchmarks, such as ENERGY STAR [28, 29] and Intel Ready Mode Technology [30, 31] efficiency benchmarks, are related to reducing energy consumption once the processor is fully idle. The average power consumption needs of such benchmarks can be met with package *C7* state. Therefore, to reduce motherboard component cost and validation¹¹ effort, desktop systems are designed to support only up to package *C7* state. Second, supporting different features for different market segments is essential for product specialization and cost efficiency. For example, such differentiation prevents laptop manufacturers from using a processor that is dedicated to the desktop market segment, which is significantly cheaper than a mobile processor with equivalent TDP, to build laptop devices.

¹¹Package *C10*, for example, requires 1) dedicated components on the motherboard to turn off IO signals, 2) a special flow to move the CPU cores’ context to a dedicated area in DRAM, and 3) migrating the processor wake-up timers to the chipset to enable turning off the processor’s crystal clock [133].

Since the CPU core’s voltage regulator is turned on in the package *C7* state (as shown in Table 1) and the power-gates are bypassed in DarkGates, the power consumption of package *C7* is significantly (more than $3\times$) higher in DarkGates than in the baseline due to the additional leakage power of the ungated CPU cores. To mitigate this issue, we extend the desktop systems with the package *C8* state [21, 22, 60]: a deeper (lower power but with higher entry/exit latency) package C-state in which the voltage regulator of the CPU cores is off, as shown in Table 1. This reduces the CPU cores’ leakage power and saves even more power in the uncore compared to the package *C7* state.

5. Implementation and Hardware Cost

DarkGates’ three key components are implemented within the Intel Skylake SoC [23, 33, 34].

First, DarkGates requires the implementation of different packages for the processor segment with power-gates (i.e., Skylake-H, used for high-end mobile system) and the processor segment that bypasses the power-gates (i.e., Skylake-S, used for high-end desktop systems). Typically, these two processor segments already have different packages: a land grid array (LGA [86]) package for Skylake-S and a ball grid array (BGA [87]) package for Skylake-H.

Second, we implement DarkGates’s power management flows in firmware¹² to enable the *hybrid* architecture on the processor die. DarkGates operates in one of two modes based on a silicon fuse [134] value: 1) *bypass mode*, which bypasses the power-gates to increase the voltage and frequency of the CPU cores, and 2) *normal mode*, which uses the power-gates to reduce the leakage power of the CPU cores. The additional firmware code to support this flow is approximately $0.3KB$, which is less than 0.004% of Intel Skylake’s die area [55].

Third, DarkGates requires the implementation of a deeper package C-state (i.e., package *C8*) for desktop systems (i.e., Skylake-S). The package C-state power-management hardware and firmware flows are already implemented in the baseline used for mobile systems [21, 133]. Therefore, we expect no additional cost for this third component.

Like many other architectural optimizations, DarkGates also has **tradeoffs** and **drawbacks**. First, as explained in Sec. 4.2, DarkGates can affect the lifetime reliability of the processor. Second, the proposed mechanisms of DarkGates can degrade the performance of power-limited processor scenarios where few cores are active (e.g., computer graphics). This is because the additional leakage of the inactive cores reduces the power budget allocated to the graphics engines (as shown in Fig. 9). Third, DarkGates requires separate designs for the target segments. Although our baseline system have two separate packages for the target processor (i.e., Skylake-H and Skylake-S, discussed in Sec. 4.1), processor vendors that do not have

¹²A fully-hardware implementation is also possible. However, such power management flows are normally error-prone and require post-silicon tuning. As such, most of the power management flows are implemented within the power-management firmware (e.g., Pcode [20]).

two packages in the baseline architecture need to build two packages to implement DarkGates.

6. Evaluation Methodology

We use two distinct methodologies to 1) collect motivational data, demonstrating DarkGates’s potential benefits on our target processor’s (Skylake) predecessor (Broadwell) and 2) evaluate DarkGates on Skylake. The reason is that we would like to demonstrate the potential benefits of DarkGates on the previous generation processor (i.e., Broadwell) of our target Skylake processor, before we implement it in the Skylake processor.

Methodology for Collecting Motivational Data. We use a Broadwell-based system [94] to collect motivational data that shows the potential performance benefits of increasing CPU core frequency when we increase the effective voltage (i.e., by reducing the voltage guardband).

To collect the motivational data of the potential impedance improvement with Power-gate Bypassing, we model both the baseline (i.e., with power-gates enabled) and DarkGates (i.e., with Power-gate Bypassing) using an in-house power delivery network simulator (similar to [135, 136]). We create the model directly from the layout files of the package and the motherboard. We use a voltage regulator (VR) model, attached to the motherboard to allow time domain simulations. Each processor die is configured as a dynamic current load.

Methodology for Evaluating DarkGates. We implement DarkGates on the Intel Skylake [55] die that targets high-end desktop (i.e., Skylake-S [14]) and high-end mobile (i.e., Skylake-H [72]) processors. Table 2 shows the major system parameters. For our baseline and DarkGates measurements we use the Skylake-H (mobile) and Skylake-S (desktop), respectively.

Table 2: Parameters of Evaluated Systems

Processors	i7-6700K [137] Skylake-S
	i7-6920HQ [138] Skylake-H
	CPU Core Frequencies: 0.8–4.2GHz
	Graphics Engine Frequencies: 300–1150MHz
	L3 cache (LLC): 8MB
	Thermal Design Point (TDP): 35–91W
Memory	Process technology node: 14nm
	DDR4-2133 [139], no ECC, dual-channel, 32GB capacity

Configuring the Processor. We use Intel’s In-Target Probe (ITP) [140] silicon debugger tool that connects to an Intel processor through the JTAG port [141]. We use ITP to configure processor control and status registers (CSRs) and model specific registers (MSRs). For example, we use the ITP to configure the TDP to multiple values between 35W to 91W. For more detail, we refer the reader to the Intel ITP manual [142, 143] and to our recent prior work [36].

Power Measurements. We measure power consumption when running energy-efficiency benchmarks by using a National Instruments Data Acquisition (NI-DAQ) card (NI-PCIe-6376 [144]), whose sampling rate is up to 3.5 Mega-samples-per-second (MS/s). Differential cables transfer multiple signals from the power supply lines on the motherboard to the

NI-DAQ card in the host computer that collects the power measurements. By using NI-DAQ, we measure power on up to 8 channels simultaneously. We connect each measurement channel to one voltage regulator of the processor. The power measurement accuracy of the NI-PCIe-6376 is 99.94%. Our prior works [36, 89] provide more detail on this experimental setup.

Workloads. We evaluate DarkGates with three classes of workloads that are widely used for evaluating client processors. First, to evaluate CPU core performance, we use the SPEC CPU2006 benchmarks [122] and use the SPEC CPU2006 benchmark score as the performance metric. Second, to evaluate computer graphics performance, we use the 3DMARK benchmarks [145] and use frames per second (FPS) as the performance metric. Third, to evaluate the effect of DarkGates on energy efficiency, we measure the average power consumption of two workloads that are typically used to evaluate energy consumption of desktop systems (e.g., the Skylake-S): 1) *ENERGY STAR* is a program that promotes energy efficiency [28, 29]. An important criterion of ENERGY STAR is that a system must automatically enter into a low power mode, defined as off, sleep, long_idle, short_idle, when it is idle. The depth of the low power mode is determined based on the idle period of the system. The energy consumption limit values are calculated using a formula that is based on the residency in each power state and the power consumption of each state. 2) An idle platform workload that places the platform into *Ready Mode* enabled by Intel’s *Ready Mode Technology* (RMT [30, 31, 146]).¹³ A modern desktop system enters into Ready Mode during idle periods, in which it operates at a low power state (e.g., package C7 [151]) to reduce energy consumption while remaining connected to a communication network for usability (e.g., for email notifications and phone calls). Typically, ~99% of the time, the platform is idle (e.g., in package C7 state) and consumes few hundreds of milliwatts [66, 70, 146]. In the remaining ~1% of the time, the platform is active (in package C0 state) and consumes a few watts [30, 31, 133].

7. Evaluation

We present performance and average power benefits obtained with DarkGates when it is implemented in the Intel Skylake-S [14] processor compared to Skylake-H [72] baseline that has power-gates enabled. We evaluate three workload categories: CPU (Sec. 7.1), graphics (Sec. 7.2), and energy efficiency workloads (Sec. 7.3).

7.1. Evaluation of CPU Workloads

Fig. 7 reports the performance improvement of DarkGates when it is implemented in the Intel Skylake-S processor on SPEC CPU2006 base (single core) workloads over the baseline Skylake-H processor with enabled power-gates when both pro-

¹³Intel Ready Mode Technology (RMT) provides an alternative to the traditional desktop sleep state, such as suspend states S3 (suspend to RAM) and S4 (suspend to disk) [22, 147, 148]. A similar feature exists in mobile devices, called Connected-Standby [133, 149, 150].

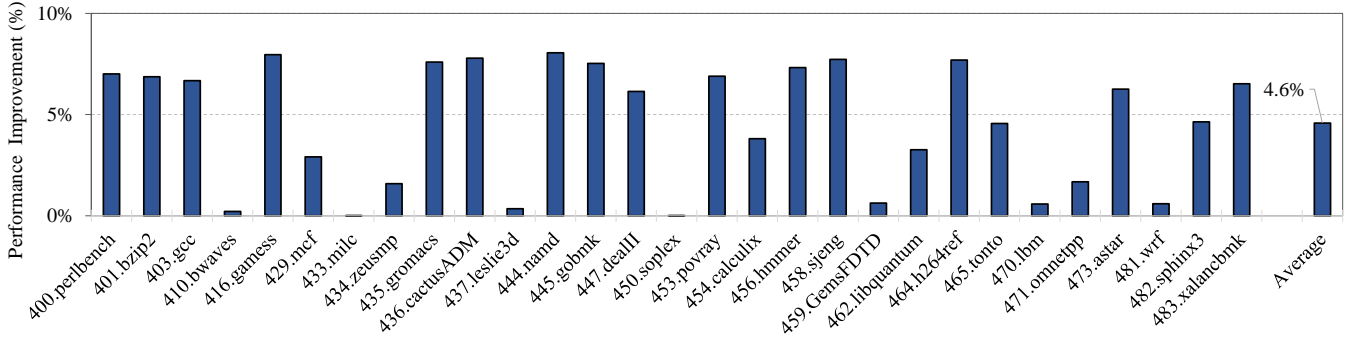


Figure 7: Performance improvement of DarkGates when it is implemented in the Intel Skylake-S processor on SPEC CPU2006 workloads compared to the baseline Intel Skylake-H processor with enabled power-gates; both processors have a TDP of 91W.

processors operate at their highest attainable CPU core frequencies within a TDP of 91W. We make two key observations.

First, DarkGates improves real system performance by up to 8.1% (4.6% on average). This result is significant as it is obtained on a real Intel Skylake-S system.

Second, the performance benefit of DarkGates is positively correlated with the *performance scalability*¹⁴ of the running workload with CPU frequency. Highly-scalable workloads (i.e., those bottlenecked by CPU core frequency, such as *416.gamess* and *444.namd*) experience the highest performance gains. In contrast, workloads that are heavily bottlenecked by main memory, such as *410.bwaves* and *433.milc*, have almost no performance gain.

We conclude that DarkGates significantly improves CPU core performance by reducing the voltage guardband with Power-gate Bypassing, which improves the V/F curve and leads to higher CPU core frequency.

Fig. 8 reports the average performance improvement of DarkGates when it is implemented in the Intel Skylake-S processor on SPEC CPU2006 base (single core) and rate (all cores) workloads over the baseline Skylake-H processor with enabled power-gates when both processors operate at the highest attainable CPU core frequencies at multiple TDP levels (35W, 45W, 65W, and 91W). We make three key observations.

First, DarkGates improves the average real system performance of SPEC base/rate benchmarks by 5.3%/4.2%, 5.2%/4.7%, 5.0%/4.8%, and 4.6%/5.0% for 35W, 45W, 65W, and 91W TDP, respectively. This result is also significant as it is obtained on a real Intel Skylake-S system.

Second, the average performance improvement of SPEC_base benchmarks decreases as the TDP level increases. The reason is that at a low TDP (e.g., 35W), the processor is more thermally constrained and runs at a lower frequency than at a higher TDP (e.g., 91W). Therefore, the relative increase in frequency, at steps of 100MHz granularity until reaching the TDP limit, is higher at a lower TDP.

Third, the average performance improvements of SPEC_rate benchmarks increases as the TDP level increases. The reason is

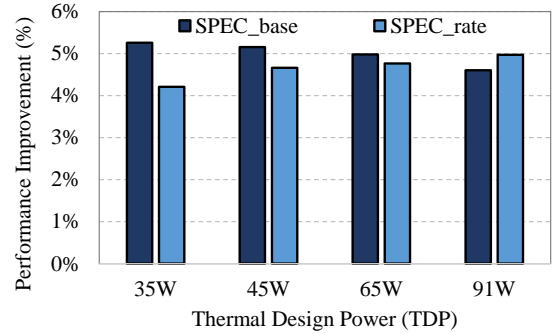


Figure 8: Average performance improvement of DarkGates when it is implemented in the Intel Skylake-S processor on SPEC CPU2006 (base and rate) workloads compared to the baseline Intel Skylake-H processor with enabled power-gates for multiple TDP levels.

that a high TDP is V_{max} -constrained while a low TDP is thermally constrained. Therefore, a low TDP processor exceeds the TDP limit faster once all cores operate at an increased frequency compared to a high TDP processor (e.g., 91W) that can increase the frequency of all cores to the maximum attainable frequency with the improved V_{max} (due to the reduced voltage guardband) without exceeding the thermal limit.

We conclude that DarkGates significantly improves CPU core performance by reducing the voltage guardband with Power-gate bypassing, which improves the V/F curves and leads to higher CPU core frequency for both thermally-constrained and V_{max} -constrained systems.

7.2. Evaluation of Graphics Workloads

Typically, the performance of a graphics workload is highly scalable with the graphics engine frequency. When running graphics workloads, the power budget management algorithm (PBM [39, 53]) of the PMU normally allocates only 10% to 20% of the compute domain power budget to the CPU cores, while the graphics engine consumes the rest of the power budget [37, 38, 54]. For a client system, while running a graphics workload, one of the CPU cores normally runs (e.g., runs the graphics driver) at the most energy-efficient frequency P_n [22] (i.e., the maximum possible frequency at the minimum functional voltage (V_{min})) while the other cores are idle and power-gated. Since the power-gates are bypassed in a system

¹⁴We define performance scalability of a workload with respect to CPU frequency as the performance improvement the workload experiences with unit increase in frequency, as described in [152, 153].

with DarkGates, the additional leakage of the inactive cores (i.e., three CPU cores in a four-core processor) reduces the effective power budget allocated to graphics engines, which can reduce the graphics performance of a thermally-constrained system.

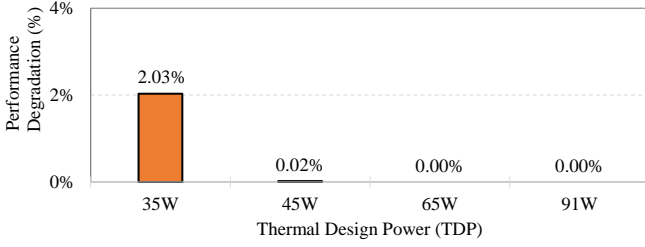


Figure 9: Average performance degradation of DarkGates over the baseline system across different TDP levels when running 3DMark graphics workloads.

Fig. 9 shows the average performance degradation of DarkGates compared to the baseline system across different TDP levels when running the 3DMark [145] graphics workloads. We make two key observations.

First, DarkGates provides the same system performance for 3DMark for TDP levels equal to or higher than 45W. Graphics performance is not affected with the additional power spent on the leakage of idle cores since graphics workloads in these systems are not limited by thermal constraints.

Second, for a TDP level of 35W, DarkGates leads to only 2% performance degradation in graphics workloads. DarkGates reduces the graphics performance for a system with 35W TDP because this system is thermally limited. Hence, the additional leakage power of the idle CPU cores forces the PBM to reduce the frequency of the graphics engine to keep the system within the TDP limit.

We conclude that the reduced graphics engine power budget due to the additional leakage power of idle CPU cores can slightly degrade the performance of graphics workloads in thermally-limited systems, but it is not a main concern in many real systems that are not thermally-limited.

7.3. Evaluation of Energy Efficiency Workloads

Unlike CPU and graphics workloads that always benefit from higher performance, energy efficiency workloads, such as *ENERGY STAR* [28, 29] and *Intel Ready Mode Technology* (RMT [30, 31]), have long idle phases where the system enters into idle power states (i.e., C-states [20, 22, 62, 133]). For example, in the RMT workload (discussed in Sec. 6) of the baseline system (i.e., with power-gates) the package C0 (i.e., active) power state residency is only $\sim 1\%$ of the total time and the package C7 (i.e., idle) power state residency is $\sim 99\%$ of the total time. Since DarkGates bypasses the power-gates, package C7 power would significantly increase due to leakage power consumed by the idle cores. Therefore, DarkGates uses package C8 instead of C7 to keep the average power of these workloads within the target limits.

Fig. 10 shows the Intel Skylake-S average processor power reduction when running the two energy-efficiency workloads,

ENERGY STAR and RMT, on two systems: 1) the DarkGates system, where power-gates are bypassed, and the deepest package C-state is C8 (denoted by DarkGates+C8), and 2) a system without DarkGates, and the deepest package C-state is C7 (denoted by Non-DarkGates+C7), when compared to the baseline system that includes DarkGates but limits the deepest package C-state to C7 (denoted by DarkGates+C7).

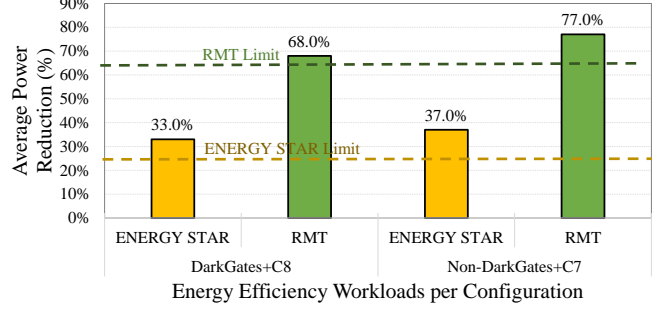


Figure 10: Average processor power reduction when running two energy efficiency workloads, ENERGY STAR and RMT on 1) the DarkGates system at package C8 power state (DarkGates+C8), and 2) a system without DarkGates at package C7 power state (Non-DarkGates+C7) compared to the baseline system that includes DarkGates at C7 (DarkGates+C7).

We make three key observations. First, our proposed DarkGates system (i.e., DarkGates+C8) reduces the average power consumption of ENERGY STAR and RMT by 33% and 68%, respectively, on the real Intel Skylake-S system, compared to the baseline where we limit the deepest package C-state to C7 (i.e., DarkGates+C7).

Second, the baseline system (i.e., DarkGates+C7) does not meet the target average power limit for both workloads. Applying package C8 is essential to meet the target average power limit since C8 turns off the CPU core's voltage regulator, which greatly reduces the leakage power of the ungated CPU cores.

Third, the system without DarkGates at the deepest package C-state of C7 (i.e., Non-DarkGates+C7) shows lower average power consumption compared to the system with DarkGates at the deepest package C-state of C8 (i.e., DarkGates+C8). The higher average power of DarkGates+C8 compared to Non-DarkGates+C7 is mainly because DarkGates+C8 has higher power consumption at the power states in which some of the cores are idle, such as C0. These cores consume leakage power in DarkGates+C8, but they are power-gated in Non-DarkGates+C7.

We conclude that for energy efficiency workloads, which have fixed performance requirements, applying DarkGates with package C8 state significantly reduces the average processor power consumption, thereby meeting the target average power requirements of the energy efficiency standards.

8. Related Work

To our knowledge, DarkGates is the first hybrid power-gating architecture for different processor market segments that increases the performance of systems constrained by the maximum attainable CPU core frequency (i.e., $F_{max-constrained}$),

such as high-end desktop systems. There are many prior works that discuss the reduction [12, 117, 118, 154–165] and characterization [116, 163, 166, 167] of various design voltage guardbands. Other works focus on system impedance characterization and optimization [136, 168]. All these works are either orthogonal to DarkGates (i.e., can be applied with DarkGates) or they do not propose a practical and hybrid mitigation approach to reduce power-gates’ impedance.

Voltage Guardband Reduction. Many prior works propose multiple techniques to reduce voltage guardband [12, 118, 154–165, 169, 170]. These works can be categorized into two types. The first category reduces the voltage guardband while the processors continue to function correctly [104, 118, 164], whereas the second category tolerates timing speculation errors with the aid of an error detection and recovery mechanism [165, 169, 170]. These mechanisms optimize voltage guardband using hardware and/or software sensors to reduce the operating margin for energy savings. Multiple of these guardband reduction mechanisms are already applied in the Skylake processor [14, 23, 34, 72, 74]. DarkGates can be applied orthogonally to these mechanisms since it physically optimizes the system impedance by bypassing the power-gates and sharing the power delivery resources on the package.

Voltage Guardband Characterization. Several prior works use simulation to study voltage noise in single-core [116, 117, 166] and multi-core [163, 167] CPUs. Other prior works conduct measurement-based studies of voltage noise in CPUs [101, 102, 118, 160, 171]. In our work, we use an in-house power delivery network simulator [125, 135] to characterize the system impedance and the voltage guardband. Our model is created directly from the layout files of the package and the motherboard as well as measured data from the previous Intel processor generation (Intel Broadwell [94]).

System Impedance Characterization and Optimization. Shekher *et al.* [136] discuss different microprocessor power gating architectures and their impact on system impedance. Engin *et al.* [168] present efficient algorithms for sensitivity calculations of power delivery network impedance to minimize the maximum deviation from the target impedance. Compared to DarkGates, these works do not propose practical mitigation techniques, such as Power-gate Bypassing.

9. Conclusion

We propose DarkGates, the first hybrid power-gating architecture for different processor market segments that increases the performance of systems constrained by the maximum attainable CPU core frequency (i.e., $F_{max-constrained}$), such as high-end desktop systems. DarkGates enables optimizing and customizing the processor package, firmware, and features based on the target processor market segment needs by overcoming the limitations introduced by power gates. DarkGates is implemented in the Intel Skylake processor for high-end desktops and mobile processors (i.e., Skylake-S and Skylake-H). On a real 4-core Skylake system with integrated graphics, DarkGates improves the performance of SPEC CPU2006 workloads by up to 8.1% (4.6% on average) for the highest thermal

design power (TDP) desktop system (i.e., 91W). DarkGates maintains the performance 3DMark graphics workloads for a desktop system with TDP higher than 45W while a 35W-TDP (the lowest TDP) desktop experiences only 2% performance degradation. DarkGates fulfills the ENERGY STAR (energy efficiency standard) and the Intel Ready Mode energy efficiency benchmark requirements. We conclude that DarkGates is an effective approach to improving energy consumption and performance demands across high-end heterogeneous client processors.

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