Understanding Power Consumption and Reliability of High-Bandwidth Memory with Voltage Underscaling

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Executive Summary

- **DRAM** has problems and one of them is **Bandwidth**.
 - **HBM** puts DRAM chips inside a package with GPU, FPGA, etc.
- **HBM** uses the package's **power** budget
 - ✓ Undervolting reduces power WITHOUT losing bandwidth.
- Push undervolting too far, it will result unwanted bit-flips
 - ✓ This Work: power, bit flips and trade-offs
- Evaluation Setup
 - ✓ Xilinx FPGA with **2 Stacks**
 - ✓ HBM voltage rail
- <u>Main Results</u>
 - ✓ 19% voltage guardband
 - ✓ 2.3X power savings
 - Fault-map to aid users to take advantage of undervolting

- Why HBM?
- What is HBM?
- Undervolting
- Methodology
- Results
 - Power
 - Reliability
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Why HBM?

• DRAM Limitations: Power, Latency, Bandwidth, etc.

✓ Specially in data-intensive applications

• Replace DRAM: PCM, MRAM, etc.

✓ Have their own limitations

• Improve DRAM:

✓ Reduced Latency DRAM (RLDRAM)

✓ Graphics DDR (GDDR)

✓ Low-Power DDR (LPDDR)

✓ <u>High Bandwidth Memory (HBM) -> Bandwidth</u>

• HBM Use cases

✓ NVIDIA A100, Xilinx Virtex Ultrascale+ HBM, AMD Radeon Pro

 \checkmark The Summit Supercomputer

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What is HBM?

• IDEA: Integrate stacks DRAM chips into the computing package

 \checkmark Use TSVs, µBumps and Silicon Interposer to connect everything

✓ **Eight 128bits** wide channels per stack

• Benefits:

✓ An order of magnitude Higher Bandwidth

✓ Smaller form factor

Lower energy per bit (7pJ vs 25pJ in DDRx)

• Challenge:

✓ Uses the package's **power** budget

✓ Save power but **NOT** lose bandwidth: **Undervolting**



Xilinx VCU128



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Undervolting

• IDEA: Reduce supply voltage but keep Frequency

✓ We can do this because of **Voltage Guardband**

✓ Save power WITHOUT losing bandwidth

• Catch:

✓ Pushed beyond guardband, bit flips will appear!

 \checkmark But we can save even more power at the cost of these faults!

• <u>Our Work:</u>

✓ Undervolt HBM

✓ Then push in too far!

✓ Report power saving and bit flips

✓ Trade-off among memory capacity, power and fault-rate

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Methodology

• Undervolting Mechanism

- \checkmark HBM supply voltage is driven by an on-board regulator
- \checkmark We control it from the host
- ✓ 10mV voltage steps

• Power Measurements:

 \checkmark Change bandwidth utilization by enabling/disabling AXI ports

- ✓ Measure power at all voltage steps
- ✓ Measure idle power by disabling all AXI ports

• Reliability Test

- \checkmark Test the entire memory vs. pseudo-channel
- Write all 1s (to detect 1-to-0 bit flips)
- Write all 0s (to detect 0-to-1 bit flips)

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Power: Active and Idle

• Active Power = $\alpha \times C_L \times f \times V_{dd}^2$



Power: α

- Active Load Capacitance = $\alpha \times C_L \times f$
- Unit: *farads per second*
- **f** and **C**_Lare constant



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Reliability: the Regions

Exponential No Bit Flips Guardband: HBM0, 0-to-1 bit flips ✓ Below nominal level ($V_{nom} = 1.2V$) % Cells in Stack 05 00 % •• HBM1, 0-to-1 bit flips ✓ No faults ··· ·· HBM1, 1-to-0 bit flips **Unsafe**: **GUARBAND** \checkmark Below guardband ($V_{min} = 0.98V$) ✓ **Exponential** growth in bit-flips min ✓ Max out at **0.84V** 0 **Failure**: 800 .95 20 8 0.8508. 0.7 \checkmark HBM crash point ($V_{critical} = 0.81V$) HBM Supply Voltage (V) ✓ Restart with nominal voltage

Reliability: the Variations

	HBM0												HBM1																					
	AXI#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	
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