SlimNoC: A Low-Diameter On-Chip Network Topology for High-Energy Efficiency and Scalability

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(1) Key motivation
Massively parallel chips require energy-efficient, cost-effective, and high-performance topologies

(2) Inspiration: Slim Fly
Slim Fly [1] ensures the lowest radix (port count) for a given node count and for a fixed diameter (we use two). Sounds ideal for an on-chip setting?

Key idea:
Lower diameter and thus average path length: fewer routers and wires required, resulting in lower cost and power consumption.

Key method:
Optimize towards the Moore Bound: the upper bound on the number of vertices in a graph with diameter \( D \) and radix \( k \).

MB(D,k) = 1 + k + k(k - 1) + k(k - 1)^2 + ...

(3) Slim Fly on a chip?

So how does it fare?

Why?

Problem with large buffers:
Short wire: small input buffers.

New-best radial-size-diameter tradeoff, but...

Long wire: traversing the whole die requires large input buffers for full link utilization.

(4) Slim NoC: Extending Slim Fly to the on-chip setting

(4.1) Generic layout models:

(4.2) Efficient layouts:

(4.3) Layout advantages:

(4.4) NoC configurations with non-prime finite fields:

(4.5) Slim NoC Router microarchitecture:

(5) Key Slim NoC results

Another problem: a lack of configurations satisfying various NoC technological constraints

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AN AREA- AND ENERGY-EFFICIENT TOPOLOGY

Slim NoC is more efficient than high-radix designs

A LOW-LATENCY TOPOLOGY

A POWER-PERFORMANCE-SWEETSPOT TOPOLOGY

A HIGHLY-SCALABLE TOPOLOGY

1296 nodes

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SLIM NOC ADVANTAGES