

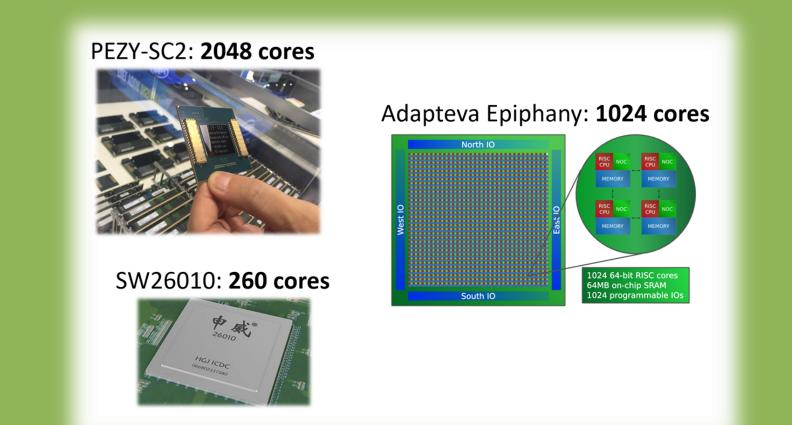
# **SlimNoC: A Low-Diameter On-Chip Network Topology** for High-Energy Efficiency and Scalability

Maciej Besta, Syen Minhaj Hassan, Sudhakar Yalamanchili, Rachata Ausavarungnirun, Onur Mutlu, Torsten Hoefler

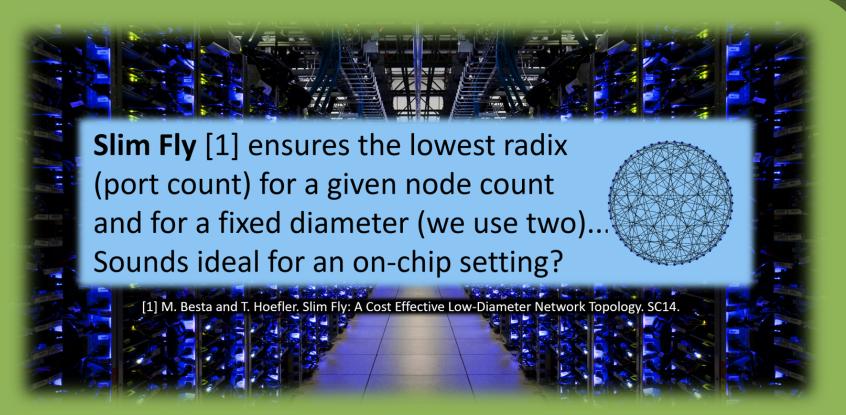


## (1) Key motivation

Massively parallel chips require energy-efficient, cost-effective, and high-performance topologies

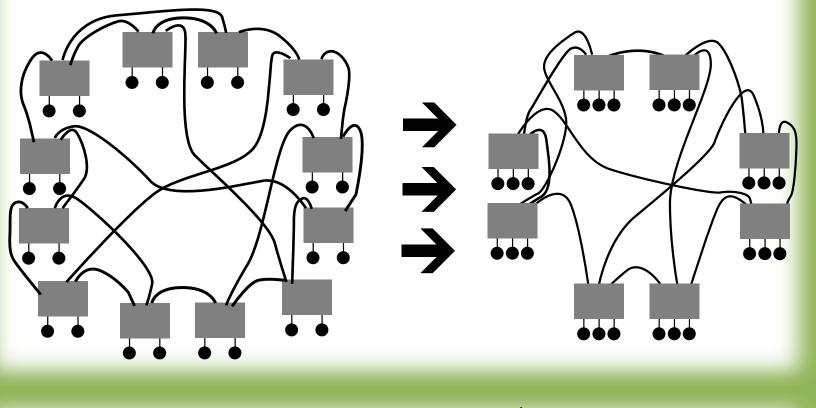


# (2) Inspiration: Slim Fly



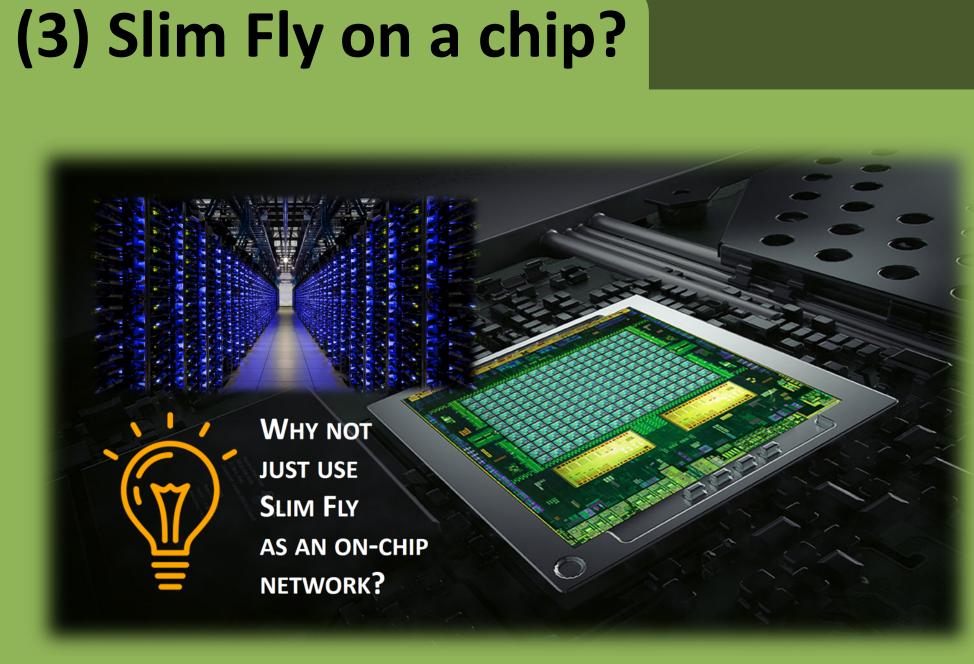
### Key idea:

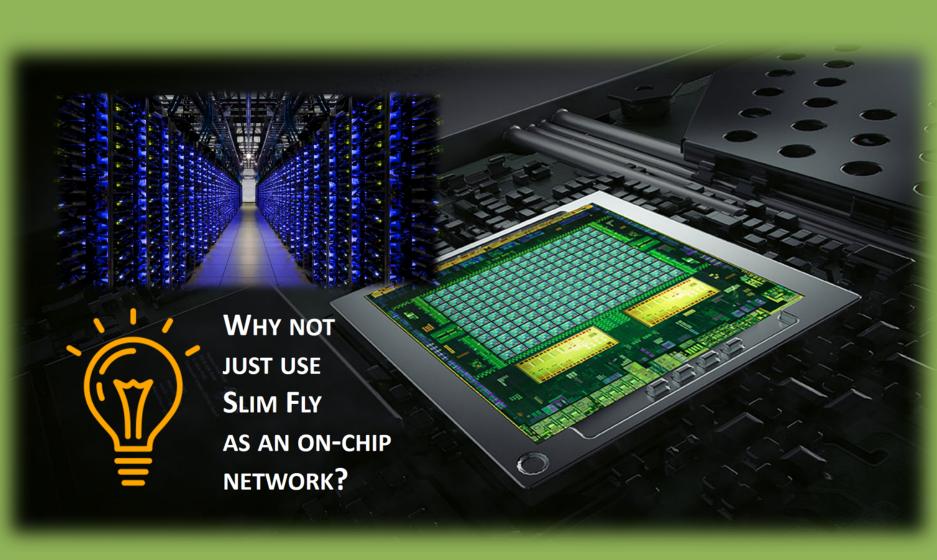
Lower diameter and thus average path length: fewer routers and wires required, resulting in lower cost and power consumption.

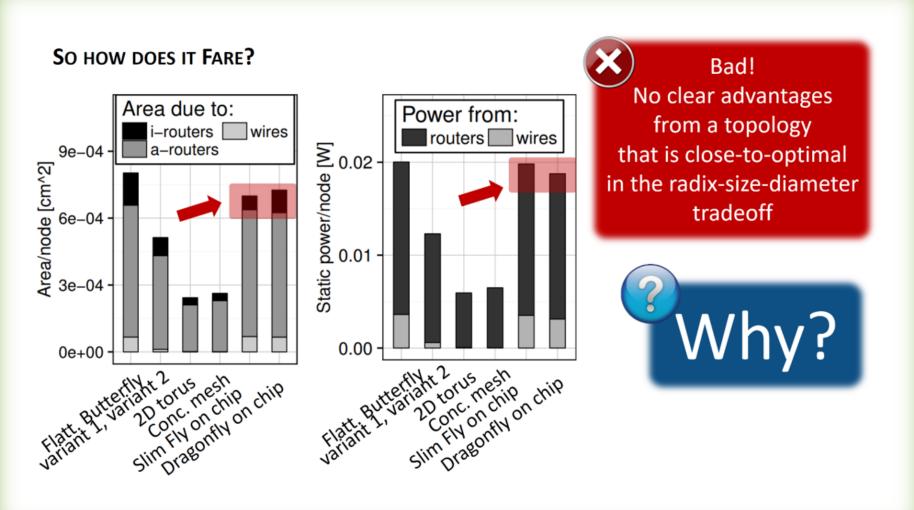


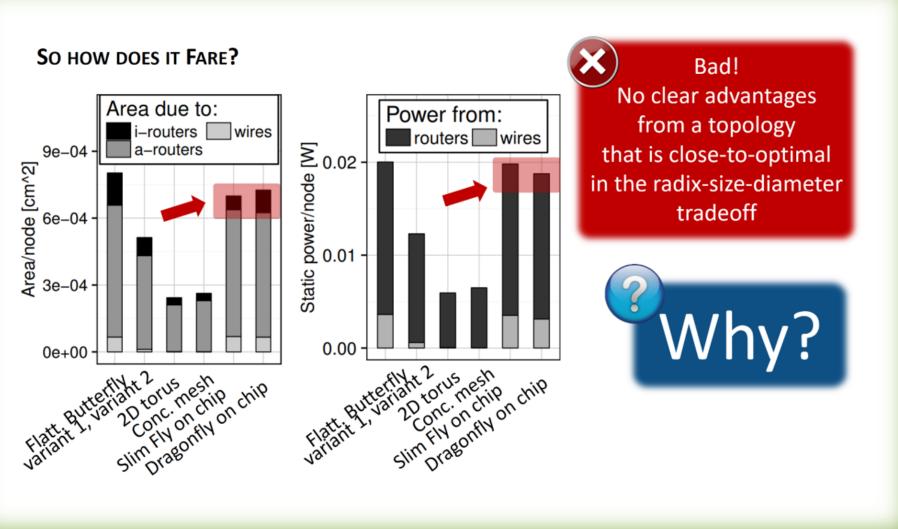


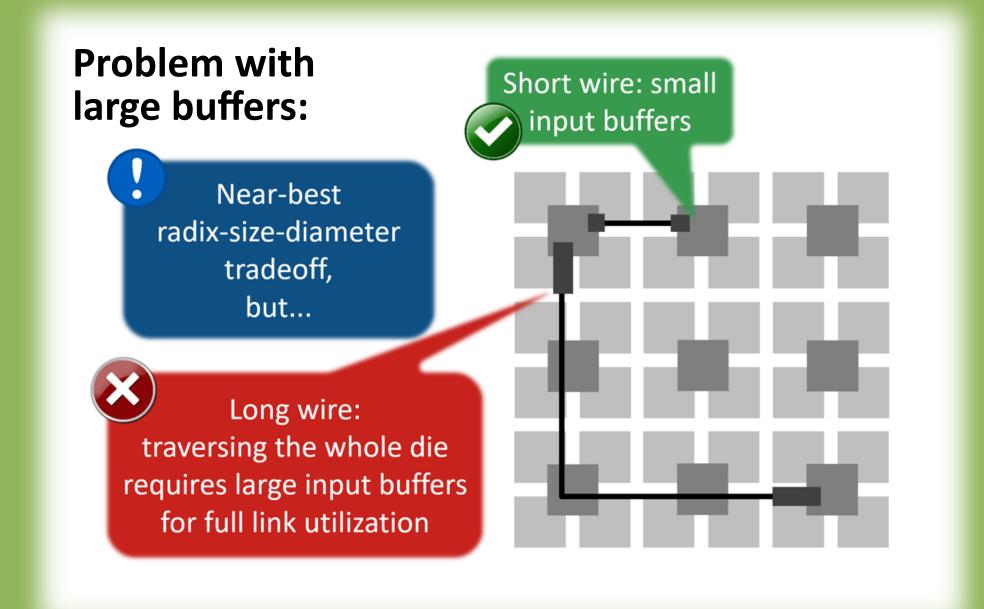
 $MB(D,k) = 1 + k + k(k - 1) + k(k - 1)^{2} + \dots$ 







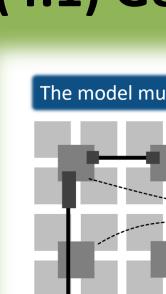




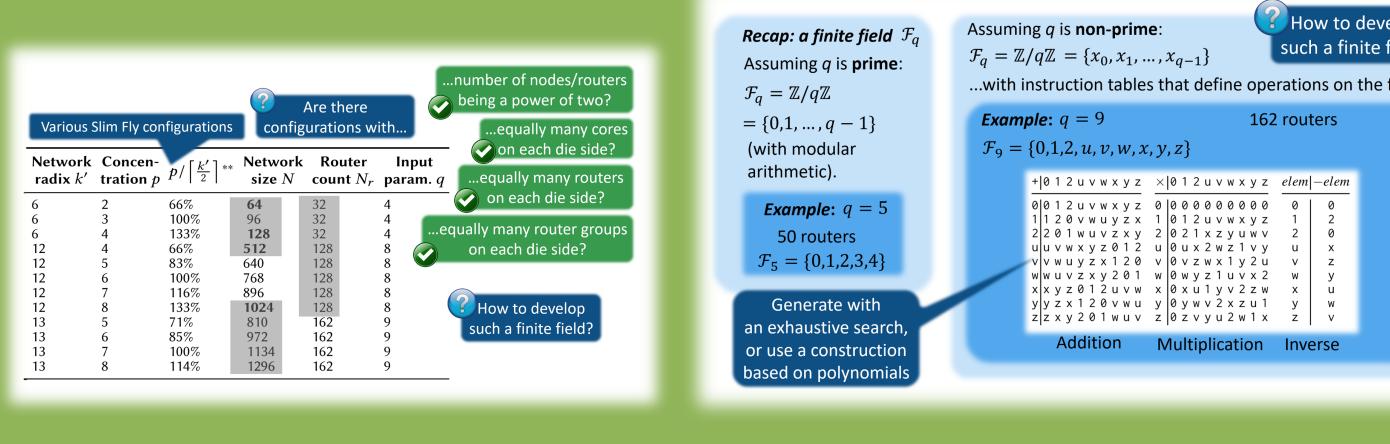
Another problem: a lack of configurations satisfying various NoC technological constraints









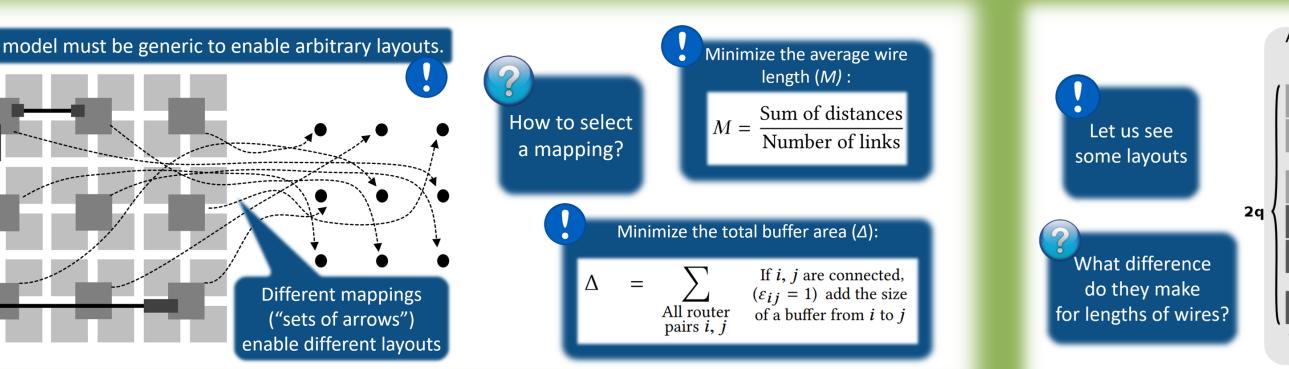






### (4) Slim NoC: Extending Slim Fly to the on-chip setting

### (4.1) Generic layout models:

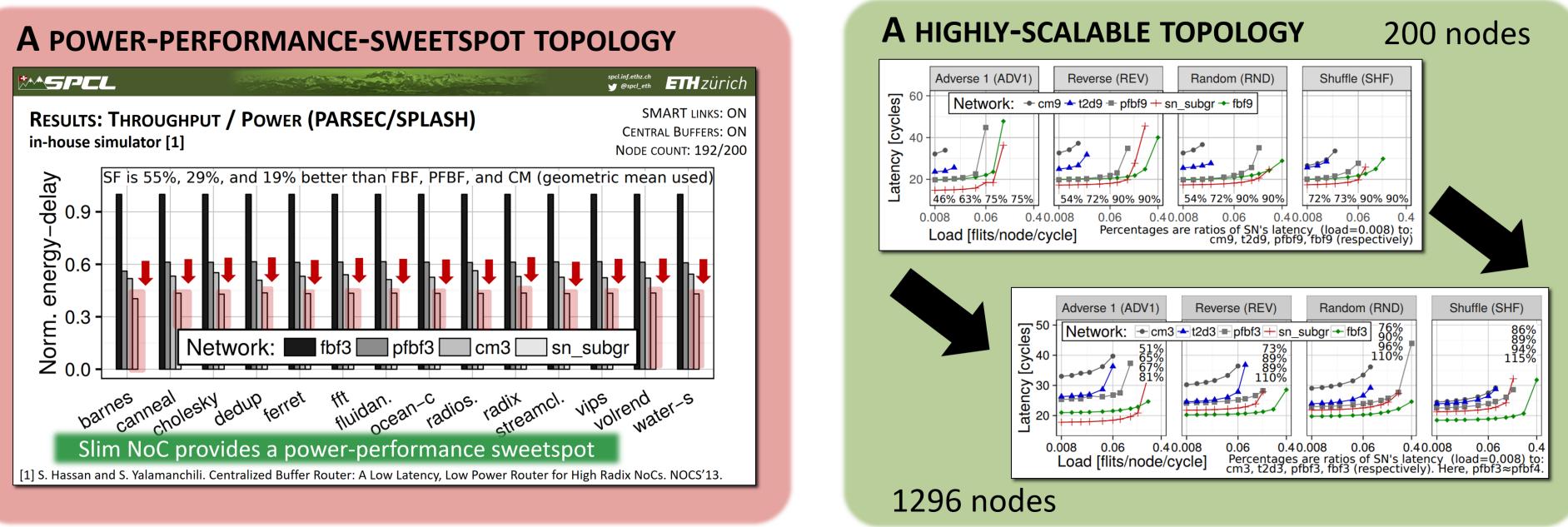


### (4.4) NoC configurations with non-prime finite fields:

### (5) Key Slim NoC results

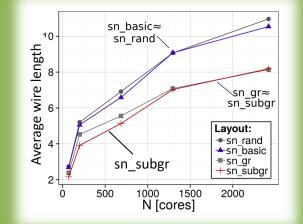
### **A** LOW-LATENCY TOPOLOGY spcl.inf.ethz.ch y @spcl\_eth **IIH**ZÜRICH \*\*\*SPCL \*\*\*SPCL cm3: concentrated mesh, t2d3: torus, SMART LINKS: ON **RESULTS: PERFORMANCE** pfbf3, pfbf4, fbf3: variants of Flattened Butterfly, CENTRAL BUFFERS: ON in-house simulator [1] NODE COUNT: 192/200 DSENT power simulator [1] **n** subgr: Slim NoC (the subgroup layout) Reverse (REV) Network: -cm3 + t2d3 = pfbf3 + pfbf4 + sn\_subgr + fbf3 ਹ 0.004 fi-router ပ္ 40 -0.003 -0.002 -0.001 -0.000 -0.06 0.40.008 0.06 0.4 0.008 0.06 0.40.008 Load [flits/node/cycle] Slim NoC provides the lowest latency [1] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.

# **SLIM NOC ADVANTAGES**



# (4.2) Efficient layouts:

### (4.3) Layout advantages:



The subgroup layout (sn\_subgr) is best for 200 nodes. The group layout reduces wiring complexity for 1296 nodes

### (4.5) Slim NoC Router microarchitecture:

velop field?	Let's leave the details for the paper and just focus on the core aspects 🙂
field.	ENHANCEMENT 1: ELASTIC BUFFER LINKS [1] + ELASTISTORE [2]
	ENHANCEMENT 2: SMART LINKS [3] Drive links asynchronously and use repeaters for single-cycle wires
	ENHANCEMENT 3: CENTRAL BUFFERS [4] Replace multi-flit input buffers with single-flit stating input buffers and add a central buffer
	<ul> <li>[1] G. Michelogiannakis et al. Elastic-Buffer Flow Control for On-Chip Networks. HPCA'09.</li> <li>[2] I. Seitanidis et al. ElastiStore: An Elastic Buffer Architecture for Network-on-Chip Routers. DATE'14.</li> <li>[3] CH. O. Chen et al. SMART: A Single-Cycle Reconfigurable NoC for SoC Applications. DATE'13.</li> <li>[4] S. Hassan and S. Yalamanchili. Centralized Buffer Router: A Low Latency, Low Power Router for High Radix NoCs. NOCS'13.</li> </ul>

**AN AREA- AND ENERGY-EFFICIENT TOPOLOGY** spcl.inf.ethz.ch ᢖ@spcl\_eth ETHZÜRICh SMART LINKS: ON CENTRAL BUFFERS: ON **RESULTS: AREA AND POWER CONSUMPTION** NODE COUNT: 192/200, TECHNOLOGY NODE: 45NM Slim NoC is more efficient than high-radix designs a-routers RRa-wires |/ RNg-wires RRg-wires: router-router wires (global layer), RNg-wires: router-node wires (global layer). [1] C. Sun et al. DSENT - A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling. NOCS'12.