Venice

Improving Solid-State Drive Parallelism at Low Cost via Conflict-Free Accesses

Session 3B: Monday 19 June, 4:00 PM EDT

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Key Problem: Path Conflicts in Modern SSDs

Multiple flash memory chips are connected to the SSD Controller using a shared channel

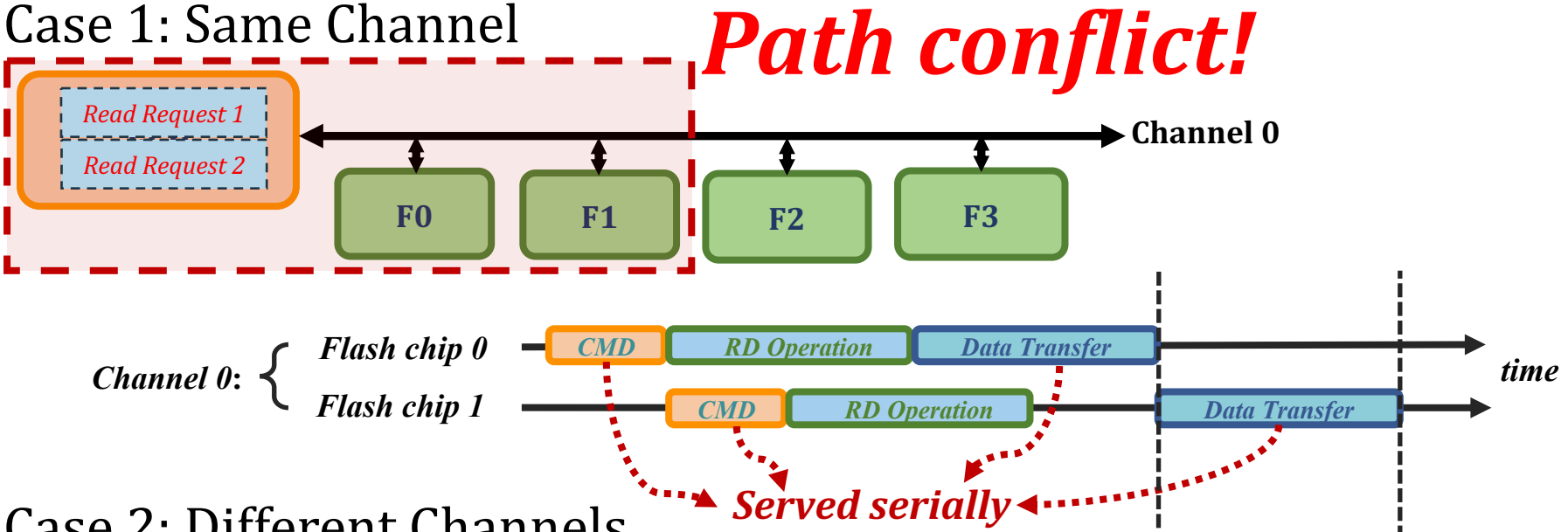
I/O requests attempt to simultaneously access the flash chips using a single path ➡ *Path Conflict*

Path Conflicts cause I/O requests to be transferred serially on the shared channel

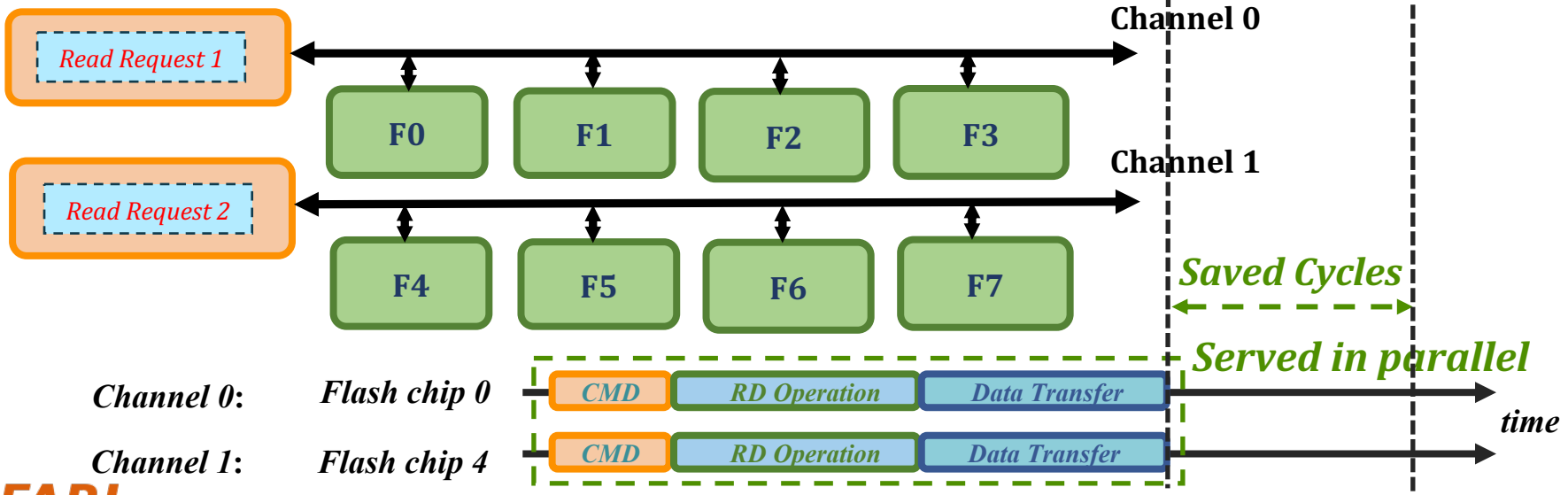
Limits SSD parallelism and overall performance

Delay Caused by Path Conflicts

- Case 1: Same Channel



- Case 2: Different Channels



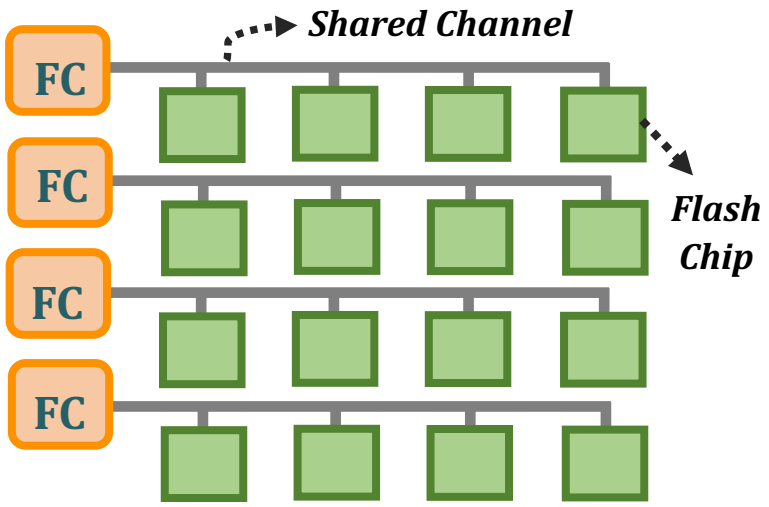
Performance Impact of Path Conflicts

Path conflicts increase the average I/O latency by 57% in our experiments on a performance-optimized SSD

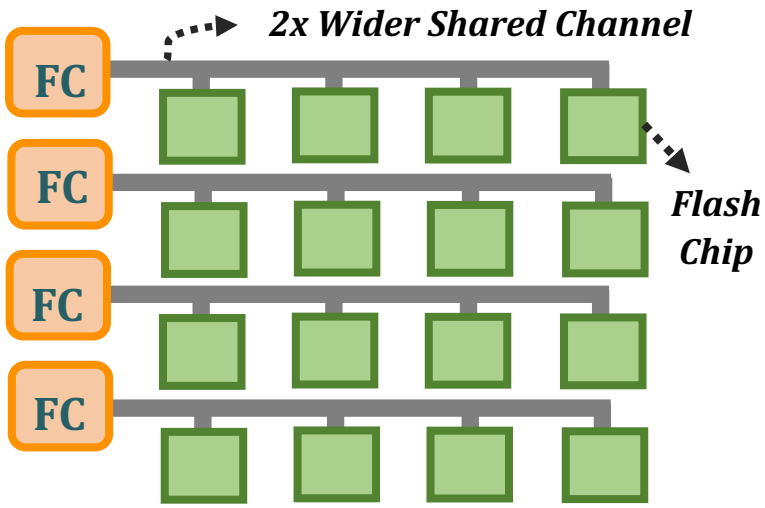
The performance overhead of path conflicts increases by 1.6x in our experiments for high-I/O-intensity workloads

Prior Approaches

Baseline SSD

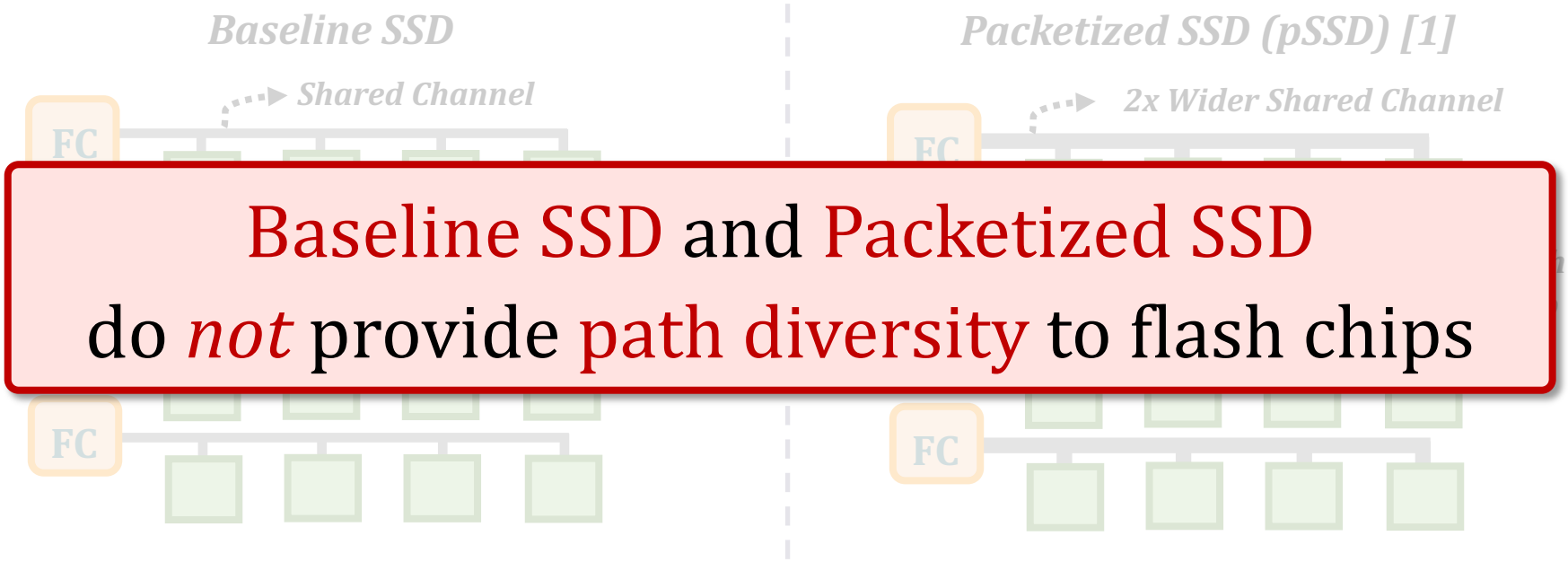


Packetized SSD (pSSD) [1]



[1] Kim+, "Networked SSD: Flash Memory Interconnection Network for High-Bandwidth SSD", MICRO 2022
[2] Tavakkol+, "Network-on-SSD: A Scalable and High-Performance Communication Design Paradigm for SSDs", IEEE CAL 2012

Prior Approaches



Baseline SSD and Packetized SSD
do *not* provide path diversity to flash chips

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Prior Approaches

Baseline SSD and Packetized SSD
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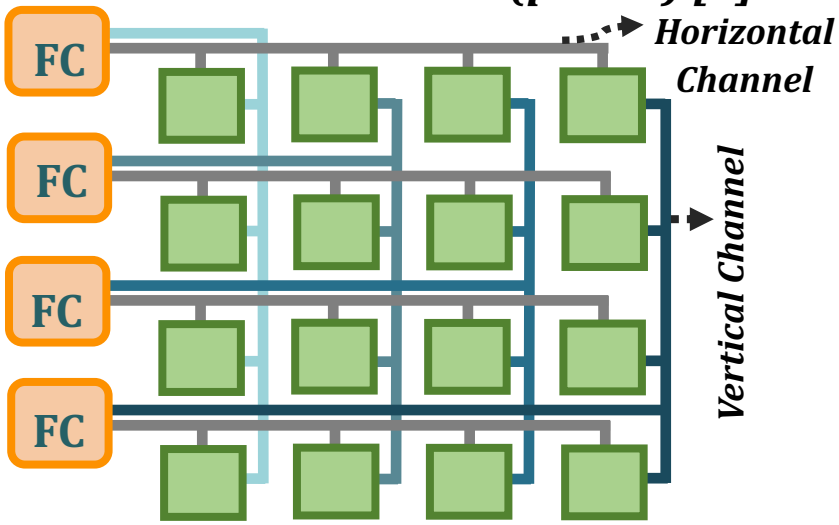
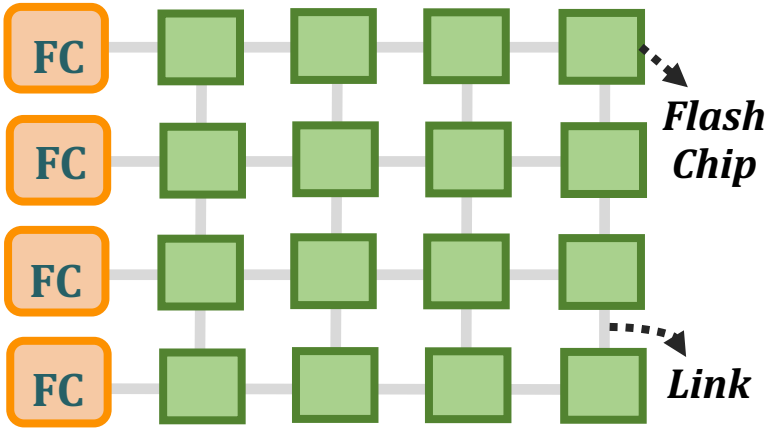
Packetized Network SSD (pnSSD) [1]



Network-on-SSD (NoSSD) [2]



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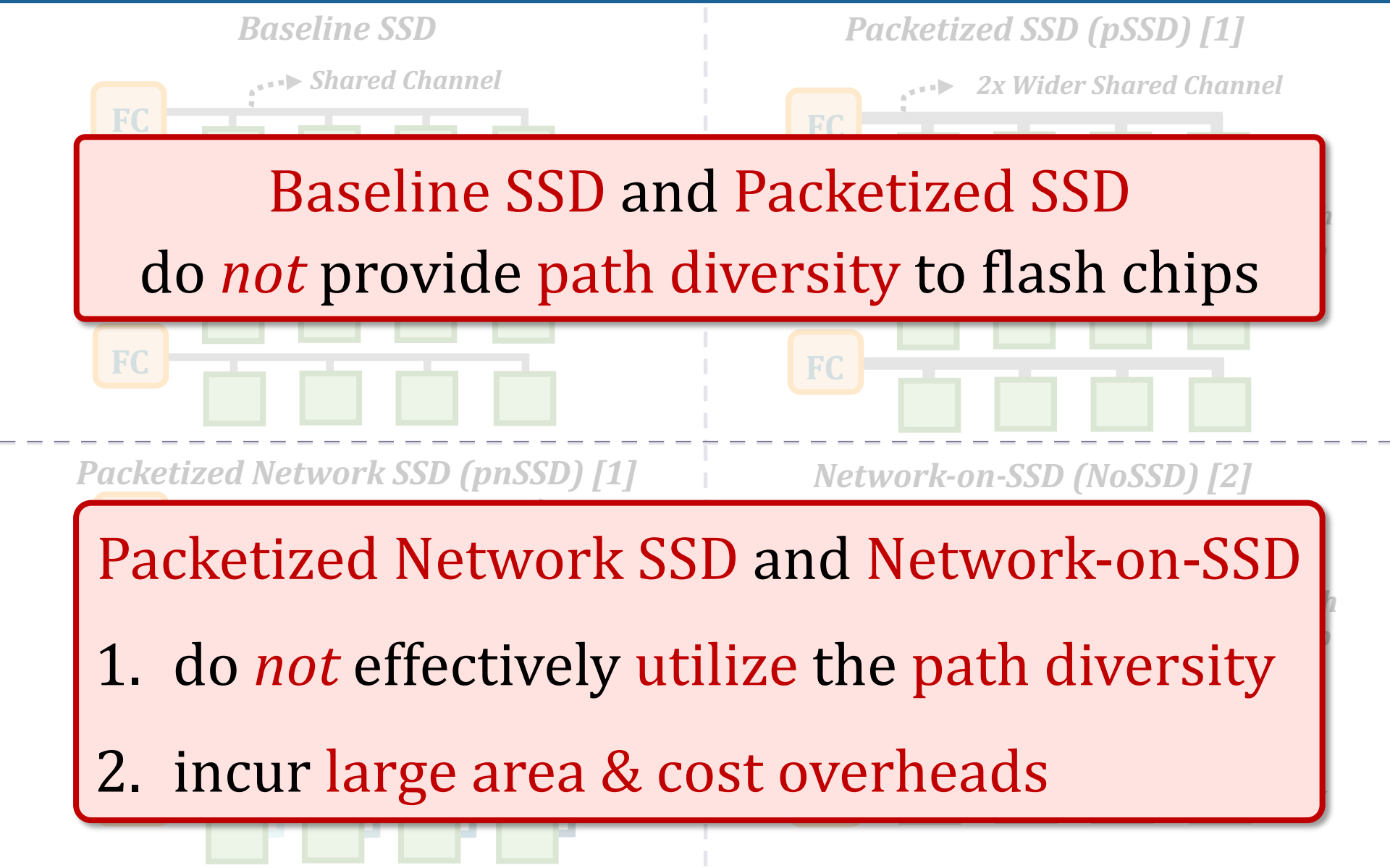
Prior Approaches



Baseline SSD and Packetized SSD do *not* provide path diversity to flash chips

Packetized Network SSD and Network-on-SSD

1. do *not* effectively utilize the path diversity
2. incur large area & cost overheads

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Our Goal

To fundamentally address the path conflict problem in SSDs by

1. increasing the number of paths to each flash chip (i.e., path diversity) at low cost

2. effectively utilizing the increased path diversity for communication between the SSD controller and flash chips

Our Proposal

Venice

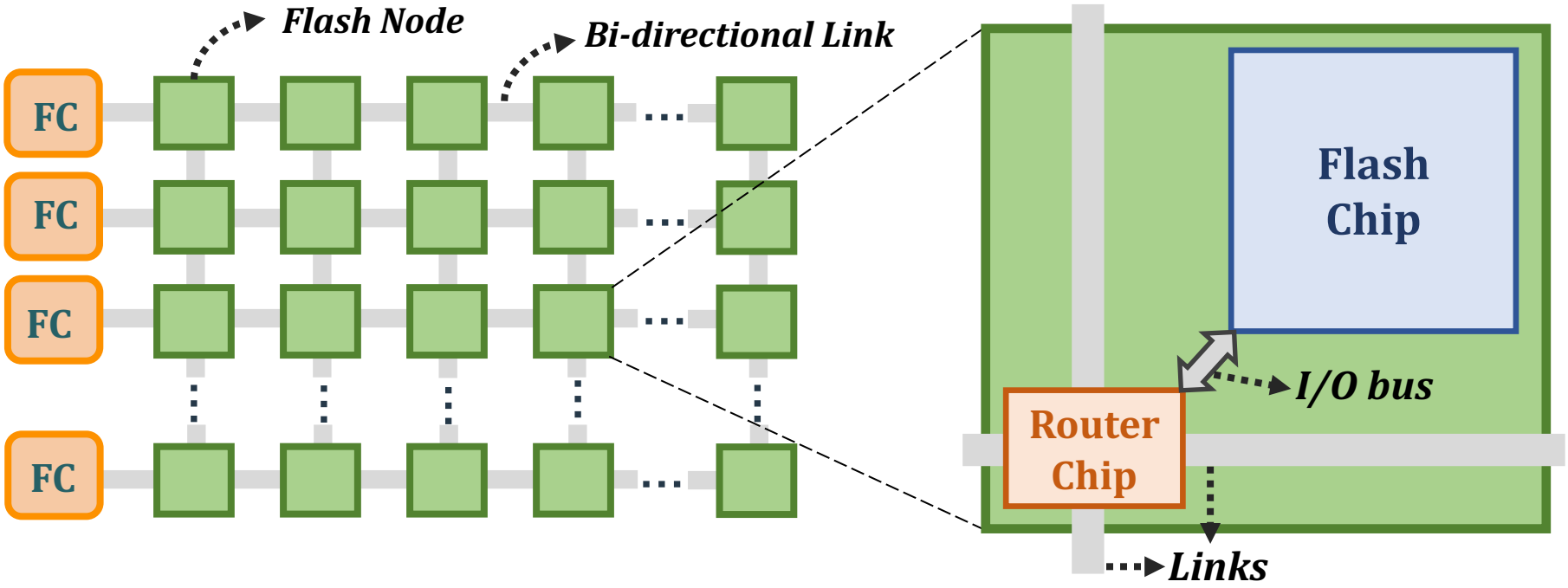
A low-cost interconnection network of flash chips in the SSD

Conflict-free path reservation for each I/O request

A non-minimal fully-adaptive routing algorithm for path identification

Named after the network of canals in the city of Venice
https://en.wikipedia.org/wiki/Venice

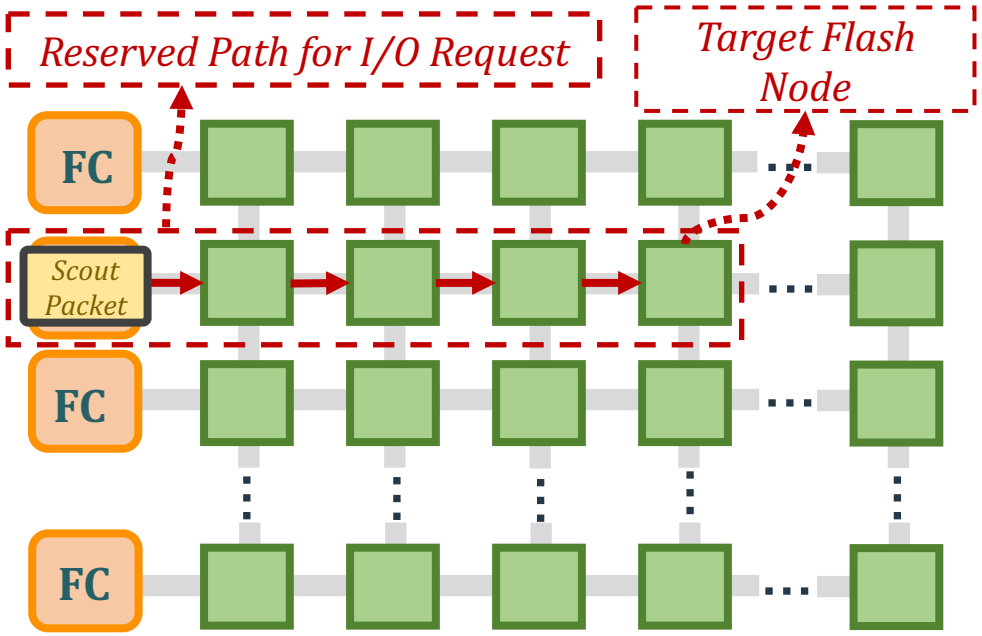
Venice: Architecture (I)



Venice provides increased path diversity at low cost

No modifications to existing flash chips in Venice

Venice: Architecture (II)



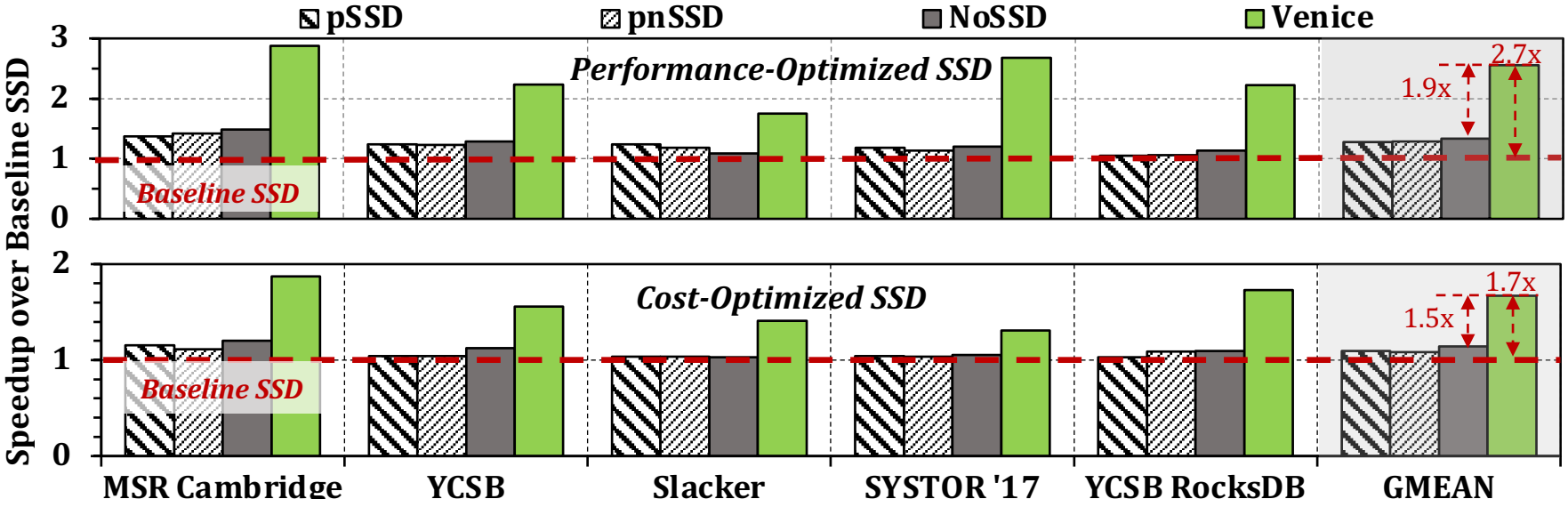
Venice uses a small scout packet
to reserve a conflict-free path for each I/O request

Path reservation eliminates path conflicts
by enabling conflict-free I/O transfer

Venice: Summary

Mitigates path conflicts by efficiently utilizing the path diversity of the SSD interconnection network

Improves performance by 1.9x/1.5x over the best-performing prior work on performance-optimized/cost-optimized SSD



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Reduces energy consumption
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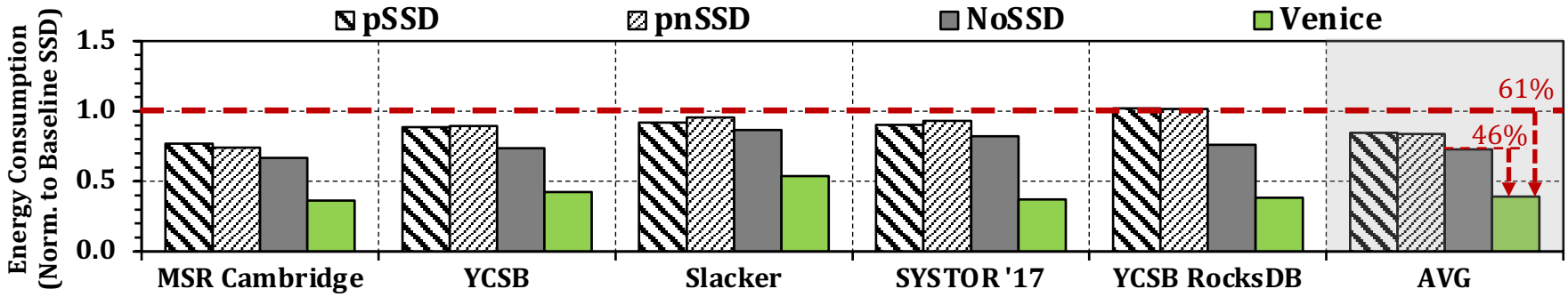

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by 1.9x/1.5x over the best-performing prior work
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Low-cost and requires
no changes to commodity flash chips

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https://arxiv.org/abs/2305.07768

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