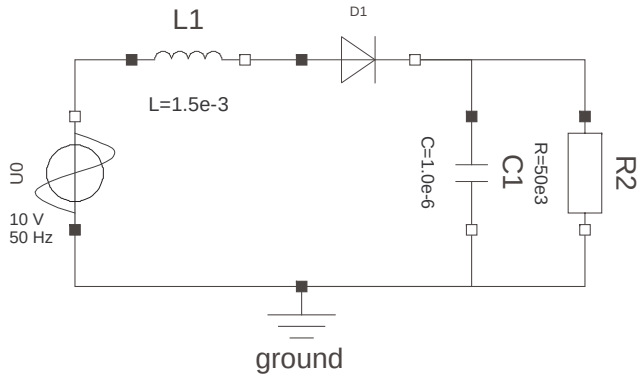
Numerical Simulation of Dynamic Systems: Hw12 - Problem

Prof. Dr. François E. Cellier
Department of Computer Science
ETH Zurich

May 21, 2013

[H9.14] Leaky Diode

Given the electrical circuit:

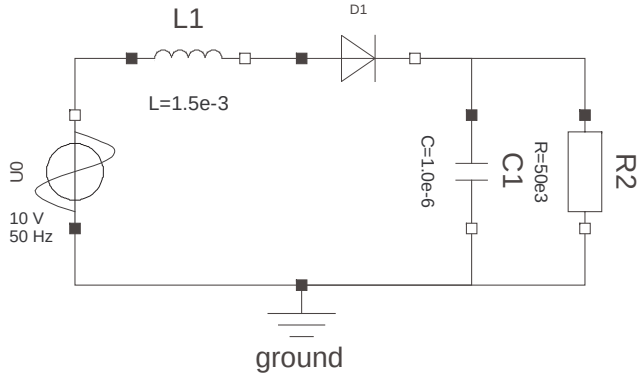


[H9.14] Leaky Diode II

- We wish to simulate the circuit using the rkf45rt routine developed in homework problem [H9.1].
- Since the diode is in series with an inductor, the causality on the switch equation is fixed, and consequently, we are dealing here with a *variable structure system*.
- We shall be using the *leaky diode* approach to avoid the division by zero.
- Choose $R_{on} = 10^{-4}\Omega$ and $G_{off} = 10^{-4} mho$, and simulate the circuit across 0.05 seconds of simulated time.
- Repeat the simulation, but this time around, choose $R_{on} = 10^{-5}\Omega$ and $G_{off} = 10^{-5} mho$.
- Split the screen into two subgraphs, and plot in the top subgraph the voltages across the capacitor together from the two simulation runs, and on the bottom subgraph the step sizes used by the two simulation runs.
- What do you conclude?

[H9.15] Mixed-mode Integration

Given the electrical circuit:



[H9.15] Mixed-mode Integration II

- We wish to simulate the circuit using the rkf45rt routine developed in homework problem [H9.1].
- Since the diode is in series with an inductor, the causality on the switch equation is fixed, and consequently, we are dealing here with a *variable structure system*.
- We shall be using the *mixed-mode integration* approach to avoid the division by zero.
- Inline the inductor using backward Euler. Step-size control will now be limited to controlling the single *continuous state variable* defined by the voltage across the capacitor. The current through the inductor is now a *discrete state variable*. The step size of the backward Euler integrator will simply be in sync with that of the RKF4/5 algorithm.
- Simulate the circuit across 0.05 seconds of simulated time.

Numerical Simulation of Dynamic Systems: Hw12 - Problem
Homework 12 - Problem
Variable Structure System

[H9.15] Mixed-mode Integration III

- Split the screen into two subgraphs, and plot in the top subgraph the voltages across the capacitor together from the current simulation run and from the more precise run of homework problem [H9.14], and on the bottom subgraph the step sizes used by the current simulation run and the more precise run of homework problem [H9.14].
- What do you conclude?