A BOND GRAPH MODEL OF THE BIPOLAR JUNCTION TRANSISTOR

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ABSTRACT

The conventional model of the bipolar junction transistor (BJT) uses two current sources to model the flow of current through a transistor. The question arises: where does the power come from that these current sources seem to inject into the circuit? A model may contain sources representing physical power supplies that are somewhere plugged into a wall socket. Such source elements are perfectly reasonable components to use in a model. Yet, an internally modulated source element somewhere within a circuit is a dubious modeling element, as it is not clear where it takes its power from.

The result of this article is a new bond graph model for the BJT that transforms the modulated current sources into a non-linear resistor. Treating these current sources as a non-linear resistor is indeed correct, since they always dissipate power and never generate it, i.e., they really represent sinks rather than sources. Additionally, RS elements are added to the BJT bond graph, so that the entropy generation by means of power dissipation is modeled correctly. The so produced heat causes a feedback in the electrical performance of the BJT, since the current flow through a transistor is temperature dependent.

Keywords

Bipolar junction transistor; Controlled source modeling; Ebers-Moll equations.

1. INTRODUCTION

The topic discussed in this article is the modeling of a bipolar junction transistor (BJT) using bond graphs. Morel *et al.* published several articles showing how a *pn*-junction can be formulated as a bond graph model [Morel *et al.* 1995, Morel *et al.* 1997]. These models are based on a low-level description of the physics governing the junction, but because they look at a single junction, their bond graphs still contain *SF*-elements describing the generation of current.

The BJT bond graph model, presented here, makes use of the standard high-level Gummel-Poon equations, as they are being used in Spice [Massobrio and Antognetti 1993, Muller *et al.* 1986]. In fact, a particular Spice dialect, BBSpice [Cellier 1991], is used as reference model. The bond graph model matches accurately the model proposed in BBSpice. The model is implemented in Dymola [Dynasim 1998], a high-level object-oriented physical system modeling language. The model was derived starting out from an earlier model that had not yet been based on a bond graph interpretation, and that represented the injected currents by means of modulated current sources [Hild 1993]. Details of the new bond graph model can be found in [Schweisguth 1997].

The main contribution of this article is that it demonstrates that the current sources, that show up in the constructed circuit model, are in fact sinks rather than sources. They can be described accurately and appropriately through a non-linear (modulated) resistor. To this end, the circuit model is reformulated as a bond graph model that explicitly balances the power flows through the BJT's junctions. Physical phenomena that belong together are concentrated into individual bond graph elements. In this way, the unnatural and suspect internally modulated current sources can be avoided.

Whereas the circuit model only represents the electrical properties of the BJT, the bond graph equivalent also models its thermal properties. This is accomplished by adding *RS*-elements to the model. These *RS*-elements transform the energy that the electrical side of the BJT dissipates into heat.

Circuit simulators, such as PSpice, simply throw away this power. Hence the BJT does not heat up. The bond graph model that is presented in this article, in contrast, accounts for the thermal effects of power dissipation by current flowing through the transistor. This causes thermal feedback from the thermal side to the electrical side of the model, since the Ebers-Moll (Gummel-Poon) equations are temperature dependent.

The article is laid out in three sections. Section 1 describes the electrical circuit model, Section 2 discusses

the BJT bond graph, and Section 3 presents some results. The BJT bond graph, as presented here, was implemented and simulated in the Dymola modeling environment [Cellier 1991, Dynasim 1998].

2. THE BJT CIRCUIT MODEL

2.1. INTRODUCTION

The BJT model that is described in this section was taken from Hild [Hild 1993, Hild and Cellier 1994]. Specifically, Hild developed a Dymola model for the BJT transistor, which he then simulated. The results of these simulations were subsequently compared to those obtained by means of conventional circuit simulators such as Spice. The BJT model that was presented in [Hild 1993, Hild and Cellier 1994] is summarized here.

2.2. THE BJT MODEL

Figure 1 shows the BJT circuit equivalent model that was used as the basis for the BJT bond graph model. The model is derived from the conventional Ebers-Moll equations for a laterally diffused *npn*-transistor. Corresponding models were derived for the vertically diffused *npn*-transistor, as well as for the two types of *pnp*-transistors.

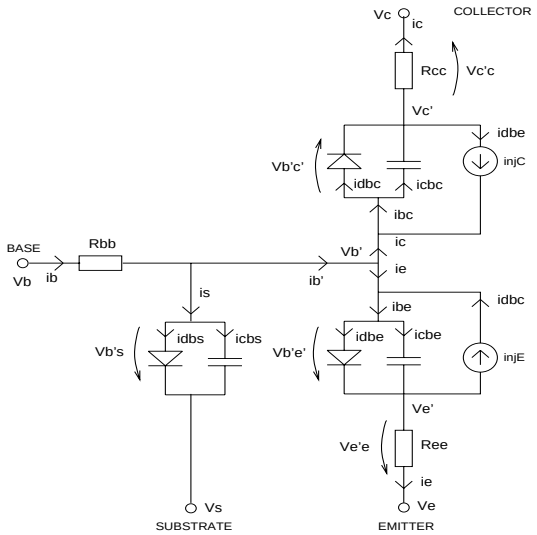

Figure 1: BJT Electric Circuit Model of Lateral NPN

For simplicity, the recombination currents, usually represented by resistors placed in parallel with the junction diodes and the junction capacitors were left out from the circuit diagram of Figure 1.

The substrate diode can be incorporated into the model in two different ways. If the substrate junction diode is formed between substrate material and the collector material, the transistor is called a *Vertical BJT*. If the substrate junction diode is formed between the base material and the substrate material, then the transistor is called a *Lateral BJT*. Figure 2 shows a lateral and a vertical BJT.

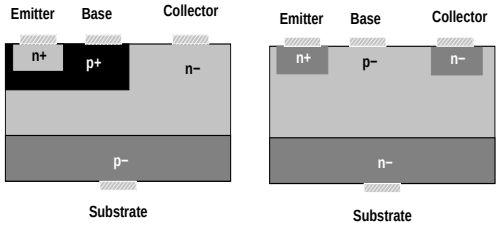

Figure 2: Vertical and Lateral NPN Transistors

The circuit model of Figure 1 contains two non-linear (modulated) current sources. The current source labeled *injC* produces current according to the model:

$$injC = J_s \left[exp\left(\frac{qV_{B'E'}}{kT}\right) \Leftrightarrow 1 \right] = i_{DBE} \tag{1}$$

whereas the current source labeled *injE* produces current according to the model:

$$injE = J_s \left[exp\left(\frac{qV_{B'C'}}{kT}\right) \Leftrightarrow 1 \right] = i_{DBC} \tag{2}$$

i.e., each of the sources is responsible for generating the current that the diode at the other side of the base needs. When the two currents are superposed (Eq. 3), they define the transistor's *linking current*:

$$J_l = J_s \left[exp\left(\frac{qV_{B'C'}}{kT}\right) \Leftrightarrow exp\left(\frac{qV_{B'E'}}{kT}\right) \right] \tag{3}$$

The linking current is the current that flows from the collector, through the base, and finally into the emitter.

2.3. THE JUNCTION DIODE MODEL

Figure 3 shows any one of the three junction diodes that represent a diffusion gradient in the semiconductor material. An equivalent electrical circuit diagram is also given. The diode indicates that current usually only flows "down-hill," not "up-hill." The capacitor symbolizes the separation of electrons from holes in the vicinity of the junction, building up electrical charge, and the resistor signifies the statistical recombination of electrons with holes, resulting in a slow discharge of the capacitor.

All three circuit elements are highly non-linear and temperature dependent. The available Spice dialects and transistor model "levels" differ in the amount of realism that

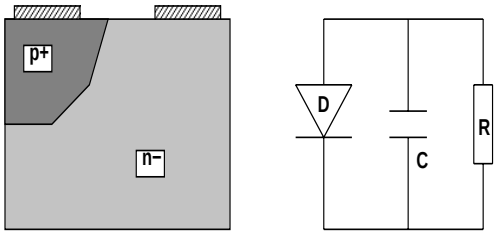

Figure 3: Junction Diode Model

they put into modeling accurately what happens inside the junction [Morel *et al.* 1997].

In figure 3, the diode circuit element is labeled D. It produces a non-linear current that is essentially exponential in nature:

$$J_d = J_s \left[exp\left(\frac{qV}{kT}\right) \Leftrightarrow 1 \right] \tag{4}$$

The regular diode is a non-linear resistor, as its constitutive equation relates voltage across and current through the diode to each other, an *e-f relationship* in bond graph terminology. The diode characteristic is shown in Figure 4. As true for all resistors, the voltage-current characteristic operates in the first and third quadrants exclusively, denoting the strictly dissipative nature of the element. At sufficiently large reverse bias (negative voltage), the diode breaks down, and current now flows "up-hill". This phenomenon is called *avalanche breakdown.*

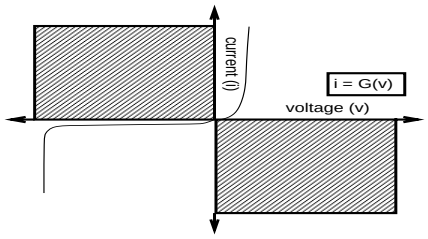

Figure 4: Junction Diode Characteristic

Also the space charge capacitor is a highly non-linear element. It is modeled by a static characteristic linking the voltage across the capacitor to the electrical charge stored in the capacitor, an *e-q relationship* in bond graph terms. Van Halen [Van Halen 1988] described the particular dialect of a space charge capacitor characteristic that is implemented in BBSpice.

3. THE BJT BOND GRAPH MODEL

3.1. INTRODUCTION

Two bond graphs are discussed in this section. The first was declared useless since it did not provide more insight into the power flows throw the BJT than the formerly used circuit model. The second bond graph model fixes this problem by concentrating each individual physical phenomenon into a single bond graph element. It shows explicitly how the power flows are balanced in the base of the BJT.

3.2 THE BOND GRAPH MODEL OF THE BJT

The BJT electric circuit model shown in Figure 1 is easily converted to the bond graph shown in Figure 5. The base of the transistor is labeled **B**, the collector is labeled **C**, the emitter is labeled **E**, and the substrate is labeled **S**. The conversion process is straightforward. The diamond property of bond graphs [Thoma 1990] was used in the conversion, in order to slightly simplify the resulting bond graph.

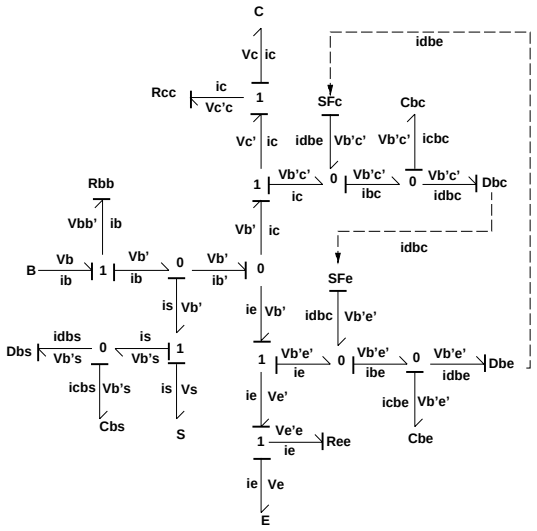

Figure 5: BJT Electric Circuit Bond Graph

The three D-elements, D_{BC}, D_{BE}, and D_{BS}, are the three junction diodes. In bond graph terms, these are non-linear resistors using the *e-f* characteristic provided in Figure 4.

Assigning causality strokes to a subcircuit is somewhat problematic, because the correct assignment depends on assumptions made about the embedding circuit. In the bond graph of Figure 5, it was assumed that all four terminals are *voltage-driven*, i.e., the four potentials V_B, V_C, V_E, and V_S are given, whereas the currents are determined by the subcircuit. However, causality strokes were only added for the convenience and better understanding of the reader. Luckily, Dymola doesn't need them, since it will determine automatically the correct causalities from the given bond graph topology.

The major problem with using this straightforward conversion technique is that the resulting bond graph still uses current sources to describe the transistor's injection currents. Hence the resulting bond graph does not provide any deeper intuition as to where these current sources draw their power

from. Therefore, the bond graph model is not more useful than the circuit equivalent model it replaces.

4. REFORMULATING THE BOND GRAPH

In order to make the BJT bond graph shown in Figure 5 more useful, it is modified in the following way. Looking at the current balance in the base-collector 0-junction, one can write:

$$\begin{aligned} & i_C + i_{DBE} = i_{BC} = i_{CBC} + i_{DBC} \\ \Rightarrow\ & i_C + (i_{DBE} \Leftrightarrow i_{DBC}) = i_{CBC} \end{aligned} \tag{5}$$

and similarly for the base-emitter 0-junction:

$$\begin{aligned} & i_E + i_{DBC} = i_{BE} = i_{CBE} + i_{DBE} \\ \Rightarrow\ & i_E = (i_{DBE} \Leftrightarrow i_{DBC}) + i_{CBE} \end{aligned} \tag{6}$$

It can be noted further that:

$$V_{C'E'} = V_{C'B'} + V_{B'E'} = V_{B'E'} \Leftrightarrow V_{B'C'} \tag{7}$$

These equivalences lead to the bond graph shown in Figure 6.

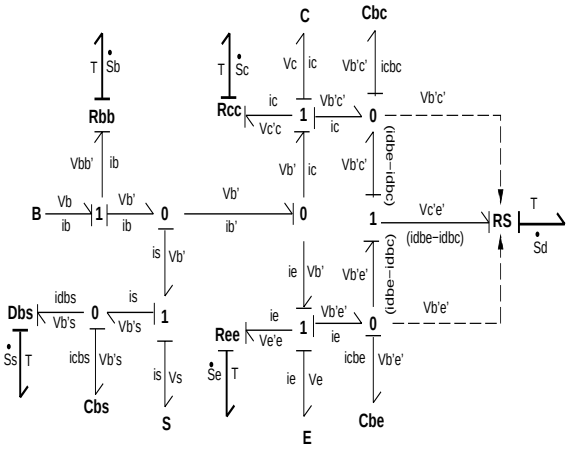

Figure 6: BJT Bond Graph Using Partial Power Flows

From Figure 6, it becomes evident that the net power dissipated by the base-collector and base-emitter diodes is:

$$P_{BJT} = V_{C'E'} \cdot i_{CE} = (V_{B'E'} \Leftrightarrow V_{B'C'}) \cdot (i_{DBE} \Leftrightarrow i_{DBC}) \tag{8}$$

The *RS*-element denotes the power dissipation across the transistor, i.e.:

$$P_{BJT} = V_{C'E'} \cdot i_{CE} = T \cdot \dot{S}_D \tag{9}$$

The *RS*-element contains the former D_{BC} and D_{BE} diodes. It computes the current, i_{CE}, flowing across the transistor from the collector through the base into the emitter.

$$\begin{aligned} i_{DBE} &= J_s \left[\exp\left(\frac{q \cdot V_{B'E'}}{k \cdot T} \right) \Leftrightarrow 1 \right] \\ i_{DBC} &= J_s \left[\exp\left(\frac{q \cdot V_{B'C'}}{k \cdot T} \right) \Leftrightarrow 1 \right] \\ \Rightarrow i_{CE} &= i_{DBE} \Leftrightarrow i_{DBC} \end{aligned} \tag{10}$$

In order to do so, the *RS*-element needs to be modulated by the two nearest 0-junctions. The modulation could have been avoided by amalgamating the *RS*-element with the neighboring 1-junction, but it was decided that the bond graph, as presented, is more instructive, since it shows explicitly the power balance at the base of the transistor.

All dissipative elements are now *resistive sources*, although the S was dropped from the notation in the bond graph of Figure 6 for compactness. If the recombination currents would have been included in the circuit diagram, two additional resistive sources would have appeared in the bond graph placed in parallel with the C_{BC} and C_{BE} space charge capacitors.

The bond graph BJT model shown in Figure 6 has been augmented with *RS*-components, so that the entropy flow can be collected from the dissipative bond graph elements. This allows the environment in which the BJT operates to heat up. As the circuit heats up, the temperature, which is a measure of heat accumulation, causes the currents flowing through the transistor to change, since the amount of current that flows through a diode is a function of its temperature.

5. SIMULATION RESULTS

The bond graph shown in Figure 6 was implemented and simulated using the Dymola modeling language and the Dymola modeling environment, respectively. A test circuit is shown in Figure 7. The BJT bond graph is represented here as a hierarchical five-port bond graph element, showing the four electrical ports (**B**ase, **C**ollector, **E**mitter, and **S**ubstrate), as well as a single **T**hermal port, through which the sum of dissipated energies is injected into the thermal model as a source of entropy [Cellier 1991, Thoma 1990].

The input to the test circuit was a narrow six volt pulse applied at the *Vin*-port. The inverted collector voltage, and the power that is dissipated across the *RS*-element for the given test circuit are plotted in Figure 8.

While the transistor is in its *OFF*-state, no current is flowing through the transistor, and consequently, no power is

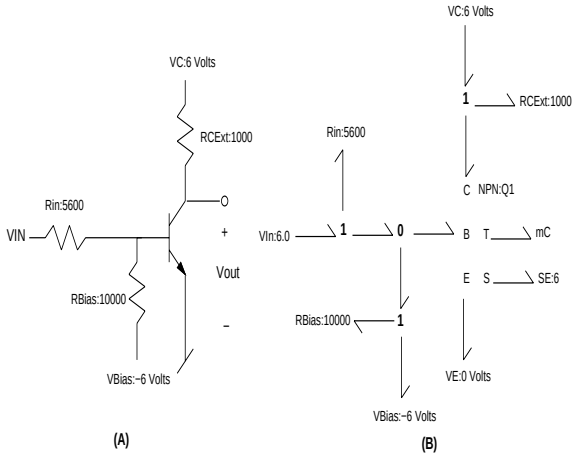

Figure 7: TestCircuit

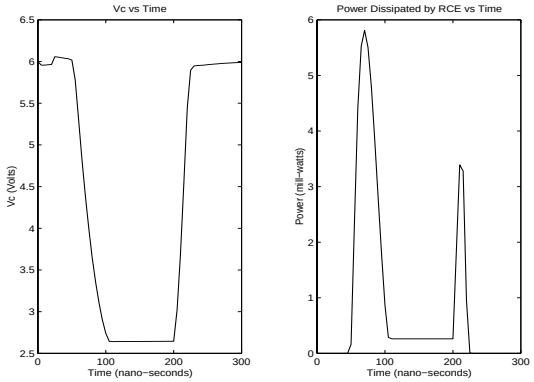

Figure 8: Inverted Collector Voltage and Dissipated Power

being dissipated. While the transistor is in its *ON*-state, current flows from the collector through the base into the emitter. During this period, a constant positive amount of power is being dissipated per time unit. However, the amount of dissipated power is comparatively small. During the switching events, considerably more power is temporarily being dissipated, both while the transistor is being turned *ON*, and while it is being turned *OFF*. As expected, the dissipated power is never negative.

It is easy to show that the physicality of this model cannot be violated. In order to violate the physicality, the signs of $V_{C'E'}$ and i_{CE} would have to be opposite. However from Eq.7, it follows that:

$$V_{C'E'} > 0 \quad \Leftrightarrow \quad V_{B'E'} > V_{B'C'} \tag{11}$$

Thence from Eq.10, it follows that:

$$i_{DBE} > i_{DBC} \tag{12}$$

and therefore:

$$i_{CE} > 0 \tag{13}$$

The simulation results obtained using the new bond graph model match perfectly those obtained using the circuit equivalent model previously developed by [Hild 1993].

6. CONCLUSIONS

The conclusion that can be reached from the exercise of developing a bond graph model for the BJT is that the consideration of power flows should be at the basis of any physical system modeling exercise, rather than being considered only as an afterthought. The initial BJT bond graph, while trivial to implement, did not provide any physical insight into the power flows across the base of the transistor over and beyond that obtainable from the circuit equivalent model. By using power flows as the basis for modeling the transistor, a second BJT bond graph was then developed. This bond graph did away with the current sources, and instead, introduced an *RS*-element to balance the transistor's power flows at the base. By using this technique, a bond graph was derived that was able to explain in a physically appealing and intuitive fashion the power flow balances that take place in the transistor.

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Michael C. Schweisguth grew up in Swiftwater, Pennsylvania. He received his B.S. degree in Electrical Engineering from the University of Scranton in 1993. He continued with his education at the University of Arizona where he received a M.S. degree in Electrical Engineering in 1997 with a thesis concerning the design and simulation of semiconductor bond graphs using the Dymola modeling environment, written under the guidance of Prof. Cellier. He is currently pursuing additional classes in computer science to strengthen his minor area of study. During his free time, he works as a software engineer at the University of Arizona's Optical Sciences Center under Prof. Tom Milster and enjoys biking and hiking around Tucson. Michael's current research interests include: computer simulation; operating systems; web technologies; embedded applications, and compilers.

Dr. Francois E. Cellier received his B.S. degree in Electrical Engineering from the Swiss Federal Institute of Technology (ETH) Zürich in 1972, his M.S. degree in Automatic Control in 1973, and his Ph.D. degree in Technical Sciences in 1979, all from the same university. Dr. Cellier joined the University of Arizona in 1984. He is currently Head of its Computer Engineering Program within the Department of Electrical and Computer Engineering. Dr. Cellier's main scientific interests concern modeling and simulation methodologies, and the design of advanced software systems for simulation, computer–aided modeling, and computer–aided design. Dr. Cellier has authored or co–authored more than 100 technical publications, and he has edited four books. He recently published his first textbook on *Continuous System Modeling* (Springer–Verlag New York, 1991). He served as General Chairman or Program Chairman of many international conferences, most recently ICBGM'93 (SCS International Conference on Bond Graph Modeling, San Diego, January 1993), CACSD'94 (IEEE/IFAC Symposium on Computer–Aided Control System Design, Tucson, March 1994), ICQFN'94 (SCS International Conference on Qualitative Information, Fuzzy Techniques, and Neural Networks in Simulation, Barcelona, June 1994), ICBGM'95 (Las Vegas, January 1995), WMC'96 (SCS Western Simulation MultiConference, San Diego, January 1996), ICQFN'96 (Budapest, June 1996), WMC'97 (Phoenix, January 1997), WMC'98 (San Diego, January 1998), WMC'99 (San Francisco, January 1999), ICBGM'99 (San Francisco, January 1999) and ICQFN'99 (Warsaw, June 1999). He is currently Vice President of Conferences of the Society of Computer Simulation International. Dr. Cellier is Associate Editor of several simulation related journals, and he served as vice–chairman on two committees for standardization of simulation and modeling software.