THE EFFECTS OF IONIZING RADIATION ON THE BREAKDOWN VOLTAGE OF P-CHANNEL POWER MOSFETS†

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ABSTRACT

The effects of ionizing radiation on the breakdown voltage of p-channel power MOSFETs were examined through two-dimensional simulation. Breakdown-voltage performance of p-channel power MOSFETs was found to be very different from corresponding n-channel power MOSFETs. In p-channel devices, simulation showed breakdown-voltage enhancement for low values of positive oxide-trapped charge, N_{ot}, whereas for high values of N_{ot}, the breakdown voltage may or may not continue to increase, and may actually decrease in some topologies. For comparison, in n-channel devices, increases in N_{ot} always cause breakdown-voltage degradation. The uncertainties stem from the interaction of the depletion region of the device (which is a function of its termination method) with its isolation technology, making it difficult to predict breakdown voltage for large N_{ot}. However, insights gained through analysis of depletion-region spreading in p-channel devices suggest a termination/isolation scheme, the VLD-FRR, that will enhance p-channel device reliability in radiation environments.

I. INTRODUCTION

P-channel power MOSFETs are of potential value for applications in radiation environments. It has been suggested that p-channel DMOS devices typically are less sensitive to gamma-dot [1] and single-event burnout [2], and may have a smaller threshold-voltage shift than n-channel devices under typical bias conditions [3]. When either an n- or a p-channel device can be used in a circuit, these advantages may offset the disadvantage of higher on-resistance of the p-channel device. For applications that require complementary drivers [4], such as power amplifiers with complementary output stages, rad-hard p-channel devices would be extremely useful, since complementary devices greatly simplify gate-drive circuit design.

One parameter that is not yet well understood for p-channel power MOSFETs, and thus makes design of rad-hard p-channel devices difficult, is the dependence of drain-source breakdown voltage on ionizing radiation. It is often tacitly assumed that p-channel device breakdown voltage will increase, and surely not degrade, in an ionizing radiation environment. Earlier research has supported this assumption [5].

P-channel devices usually employ the same termination topology, and, if integrated, the same isolation technology, as n-channel devices of similar voltage rating. Thus, their pre-rad breakdown voltages are practically identical for complementary doping and topology. As will be demonstrated in this paper, using identical termination structure topology and isolation technology for n- and p-channel devices is not always warranted. This is because of the fundamentally different effects ionizing radiation has on the spreading of the drain-body depletion region of the two device types.

II. SIMULATION METHOD

Computer code designed to simulate the effects of ionizing radiation on the breakdown voltage of power semiconductor devices has been developed at the University of Arizona [6, 7]. The code, entitled ASEPS (Arizona SEmiconductor Power device Simulator), solves Poisson's equation in two dimensions. Breakdown voltage is then determined by computing the ionization integral through the locus of highest-field points at every potential. ASEPS has proven to be an accurate and efficient simulator of highly reverse-biased junctions with arbitrary termination topologies and varying amounts of radiation-induced oxide charge [6, 7]. Its flexible input format enables comprehensive study of competing termination designs.

III. TERMINATION STRUCTURES

The primary goal of a termination structure is to raise the breakdown voltage of a planar p-n junction to its maximum, or parallel-plane, value [8]. Termination structures do this by countering the effects of p-n junction curvature that arise in planar processing. In power MOSFETs, the drain-body p-n junction limits the breakdown-voltage performance of the device; thus termination structures are built for this junction alone.

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For rad-hard devices, an equally important task for the termination structure is the retention of the pre-irradiation breakdown voltage, even at high values of radiation-induced positive oxide-trapped charge, N_{ot}.

Various methods of junction termination have been proposed and implemented, but the two most frequently used methods are field plates (FPs) and field-limiting rings (FLRs) [6, 7, 8]. FLR termination structures rely on the punchthrough mechanism to decrease the effects of junction curvature [9], while FP termination structures make use of the total bias voltage, V_{tot}, to induce charges in the device that effectively extend the junction they are terminating [10].

IV. Investigation Approach

A. *Parameters*

To demonstrate the similarities and differences between n- and p-channel power MOSFET breakdown voltage behavior, three different devices were simulated over a wide range of radiation-induced oxide charge. Data for each device are summarized in table 1. These values are representative of those found in typical low-, medium-, and high-voltage power integrated circuit (PIC) applications. In all ASEPS-generated figures in this paper, dark circles indicate highest-electric field points (which identify the part(s) of the device where breakdown occurs), and the lines are equipotential lines.

B. *Modeling*

In figures 1a and 1b, ASEPS simulation results for the drain-body junction belonging to the medium-voltage device of table 1 are shown with negligible N_{ot}. (Representative power-MOSFET cross-sections are shown in figure 3.) Note that figure 1a faithfully depicts either the outermost ring of an

		Device Parameter		
		Junction Depth [μm]	Substrate Doping [cm-3]	Parallel-Plane Vbreakdown [V]
Voltage Rating	low	3	1.1×10^{16}	50
	med	5	1.0×10^{15}	300
	high	40	2.0×10^{14}	1000

Table 1. Data for the devices discussed in the text and simulated with ASEPS.

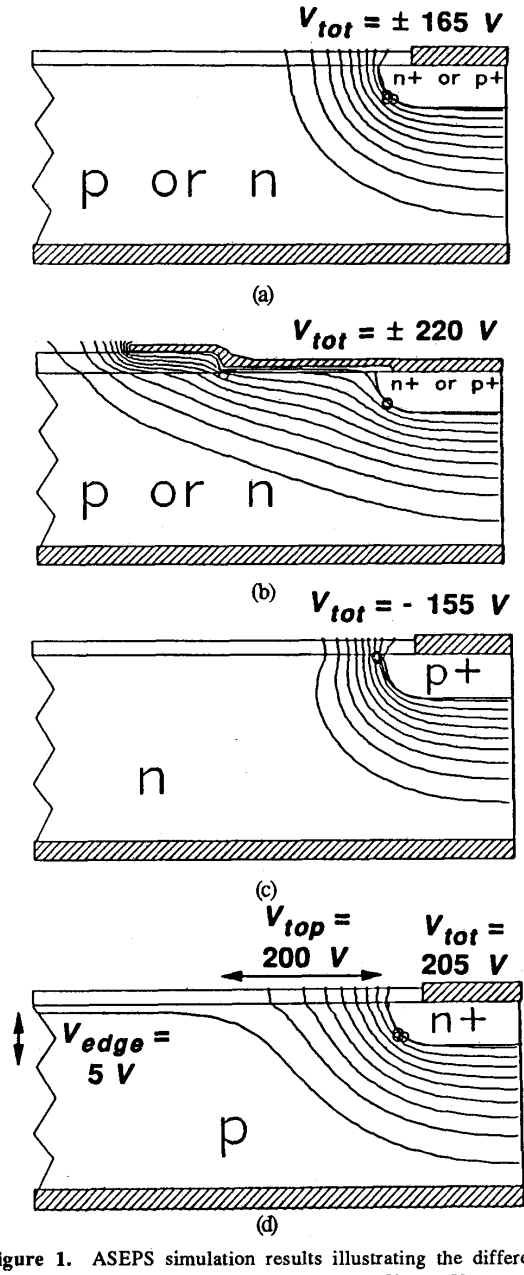


Figure 1. ASEPS simulation results illustrating the different responses of n- and p-channel devices to N_{ot}. $V_{tot} = V_{break}$ in all figures. a) N- or p-channel device without termination and with negligible N_{ot}. b) N- or p-channel device with two-level field plate and negligible N_{ot}. c) N-channel device showing breakdown-voltage degradation with $N_{ot} = 3.0 \times 10^{11}\ cm^{-2}$. d) P-channel device showing breakdown-voltage enhancement with $N_{ot} = 3.0 \times 10^{11}\ cm^{-2}$, but V_{tot} is split between V_{top} and V_{edge}. This splitting can cause breakdown voltage degradation in some topologies.

FLR termination structure or an unterminated drain-body junction, while figure 1b shows an FP termination structure. The equipotential lines are distributed identically for both device polarities. Thus, any termination structure designed for an n-channel device will work equally well for a p-channel device of equal voltage rating, assuming negligible N_{ot}.

As N_{ot} increases, however, the breakdown performance of n- and p-channel devices diverges. Assuming N_{ot} is located at the Si-SiO_2 interface, the induced areal number density of semiconductor charge, N_s, is equal to N_{ot} due to simple electrostatics (i.e. $Q_s = -Q_{ot}$), regardless of device polarity. Thus, N_s serves to compress the equipotential lines in the n-channel device, which lowers breakdown voltage, as seen in figure 1c. A field plate will tend to offset this compression by inducing charge of opposite sign in the semiconductor. In the p-channel device, N_s effectively extends the main junction, decreasing the curvature of the equipotential lines and increasing the initial breakdown voltage, as seen in figure 1d. A field plate enhances this effect, since both the plate-induced charge and the radiation-induced charge carry the same sign.

The breakdown voltage of the p-channel device may not increase indefinitely, however, as has often been assumed [5]. The reason can be understood by considering N_s in more detail. N_s resides in the silicon, and for large N_{ot}, most of it is confined to one extrinsic Debye length, L_D, of the Si-SiO_2 interface, where

$$L_D = \sqrt{\frac{\kappa_{Si}\,\varepsilon_0\,k\,T}{q^2\,N_{sub}}} \quad . \tag{1}$$

In (1), κ_{Si} is the relative dielectric constant of silicon, ε_0 is the permittivity of free space, k is Boltzmann's constant, T is temperature in degrees Kelvin, q is the electronic charge, and N_{sub} is the substrate doping.

An effective n-type volumetric doping, valid within one L_D of the Si-SiO_2 interface, can be defined by $N_{eff} = N_s/L_D \approx N_{ot}/L_D$. (Detailed consideration of the charge profile in this region neither enhances accuracy nor aids physical understanding.) Once a certain critical value of surface charge, $N_{s,crit}$, is present, N_{eff} is sufficiently high that the entire depletion region cannot completely penetrate it. For $N_s > N_{s,crit}$, a fraction of the depletion region extends to the edge of the chip. Thus V_{tot} is divided between the top and the edge of the device, i.e. $V_{tot} = V_{top} + V_{edge}$, as indicated in figure 1d.

Intuitively, it is expected that as N_s increases beyond $N_{s,crit}$, V_{edge} will increase. In fact, simulation has shown that V_{top} and V_{edge} do not change simultaneously, and that V_{edge} has a maximum value for a given N_{ot}, $V_{edge(max)}$. That is, as V_{tot} increases from 0 V to some large positive voltage, V_{edge} increases from 0 V to $V_{edge\ (max)}$, and then V_{top} increases from 0 V to V_{tot} - $V_{edge(max)}$. $V_{edge(max)}$, then, is a function only of N_{ot} and N_{sub}.

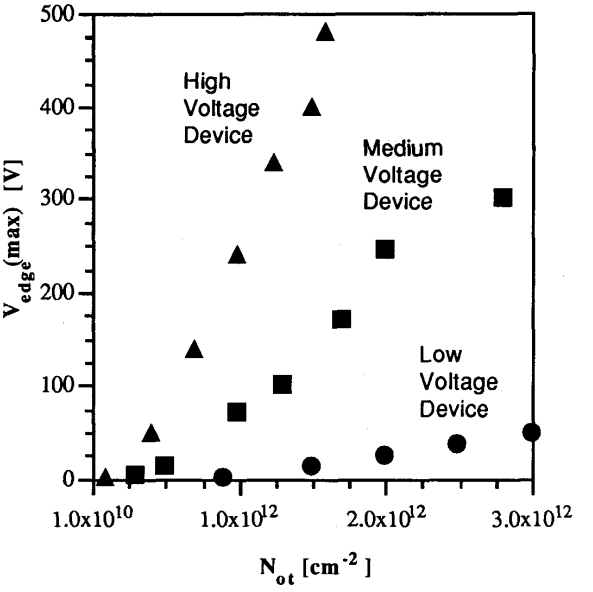


Figure 2. $V_{edge(max)}$ vs. N_{ot} for the three devices of table 1.

In figure 2, $V_{edge(max)}$ is plotted against N_{ot} for the three devices of table 1. In addition to the data displayed in figure 2, simulation has shown that $N_{eff} \approx 2\,N_{sub}$ defines $N_{s,crit}$ for any p-channel device, validating the previous assumptions about the charge distribution in the semiconductor.

Having established the characteristics and magnitude of V_{edge} a key result is obtained: although the p-channel breakdown voltage does legitimately increase for $N_s < N_{s,crit}$, assuming that it increases indefinitely presupposes that having $V_{edge} > 0$ does not degrade the breakdown voltage or circuit performance at all. This assumption is not justified. The V_{edge} component of V_{tot} can cause crosstalk, surface electric fields, and/or sharply reduced breakdown voltage, depending on the topology of the device under consideration.

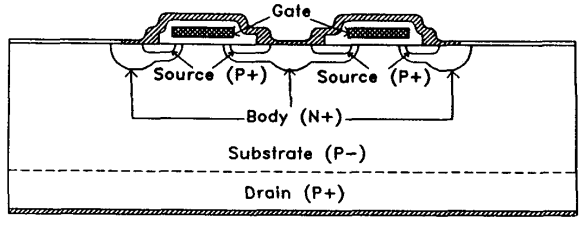
V. Implications for Termination Structures

Based on the results of section IV, the effectiveness of FP and FLR termination structures for p-channel devices in radiation environments can be predicted. For example, multiple-ring FLR termination structures may not be effective, since the punchthrough mechanism on which FLR designs rely is not intact for $N_s \geq N_{s,crit}$.

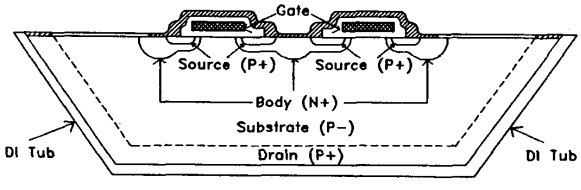
FP termination structures may be a better alternative for p-channel devices in radiation environments than are FLR designs. The reason, mentioned briefly in section IV, is that the presence of Q_{ot} enhances the effect of the FP. Quantitatively, an FP induces voltage-dependent areal charge in the substrate directly below the FP, Q_{plate}, where

$$Q_{plate} = \frac{\kappa_{ox}\,\varepsilon_o}{t_{ox}} V_{tot} \quad , \qquad (2)$$

which carries the same algebraic sign (negative) as Q_S, giving $Q_S \approx Q_{plate} + Q_{ot}$. In (2), κ_{ox} is the dielectic constant of silicon dioxide, ε_o is defined as in (1), and t_{ox} is the oxide thickness under the FP.



(a)



(b)

Figure 3. Types of p-channel power devices. a) Discrete device. b) Dielectrically-isolated integrated device.

The increase in Q_S under the FP for a given V_{tot} improves the breakdown voltage performance of the FP, since FP termination structures become more effective as N_{eff} increases beyond N_{sub}. The maximum breakdown voltage, obtainable for $N_{eff} \gg N_{sub}$, can be predicted from the device parameters N_{sub} and t_{ox} [11].

VI. Implications for Device Isolation

Even with an FP termination structure, Q_{ot} still gives rise to V_{edge}, which now extends from the edge of the FP. So although the electric field near the FP termination structure itself will not cause device breakdown voltage to degrade, the electric field near the device isolation technology may. In fact, the actual termination structure, whether FPs, FLRs, or some other technique, does not influence the following discusion of device isolation, since all conventional termination structures will have a V_{edge} component that interacts with the device isolation. For the puposes of this discussion, then, assume that both $N_{ot} > N_{s,crit}$ and $V_{tot} > V_{edge(max)}$.

A. *Discrete Power Devices*

As seen in figure 3a, a discrete power device has its drain connection at the bottom of the wafer. If there is no isolation scheme to prevent the depletion region from spreading indefinitely, as is often the case, V_{edge} is dropped across the edge of the chip. This gives rise to surface electric fields, and thus unpredictable breakdown performance [12]. V_{edge} must be handled in this case by a beveled termination or some other surface passivation technique. Thus, a discrete p-channel power device should, at the very least, employ some sort of edge passivation and/or termination in addition to its existing termination structure if it is to be used in an ionizing radiation environment.

Beveled terminations are well understood [13], but are undesirable for a modern process. This is because they require a great deal more effort to realize than do planar terminations [14], and are incompatible with integrated power applications.

B. *Integrated Power Devices*

Two classes of integrated power devices are considered: junction-isolated and dielectrically-isolated (DI). A junction-isolated p-channel device can be particularly vulnerable to ionizing radiation, since V_{edge} could either punch through the isolation or simply extend (via its depletion layer) around the isolation and directly influence the logic circuitry. If this happens, it will almost certainly lead to system failure. If V_{edge} does not punch through or go under the isolation, junction isolation is as effective as dielectric isolation.

At first glance, DI p-channel power devices may seem impervious to ionizing radiation, since the p^+ wraparound (the drain contact in figure 3b) forces the depletion layer of V_{edge} through the top of the device. When sufficient N_{ot} is present, however, the breakdown voltage of a DI device will drop precipitously, far below its pre-rad value. The reason is that equipotential crowding, and thus device breakdown, occurs at the intersection of the drain contact with the surface.

To demonstrate this phenomenon, the three devices of table 1 were simulated in DI tubs without any termination structures and their breakdown voltage, V_{break}, vs. N_{ot} was obtained. A representative result is displayed in figure 4a. In figure 4b, ΔV_{break} is plotted vs. N_{ot} for all three devices. The value of

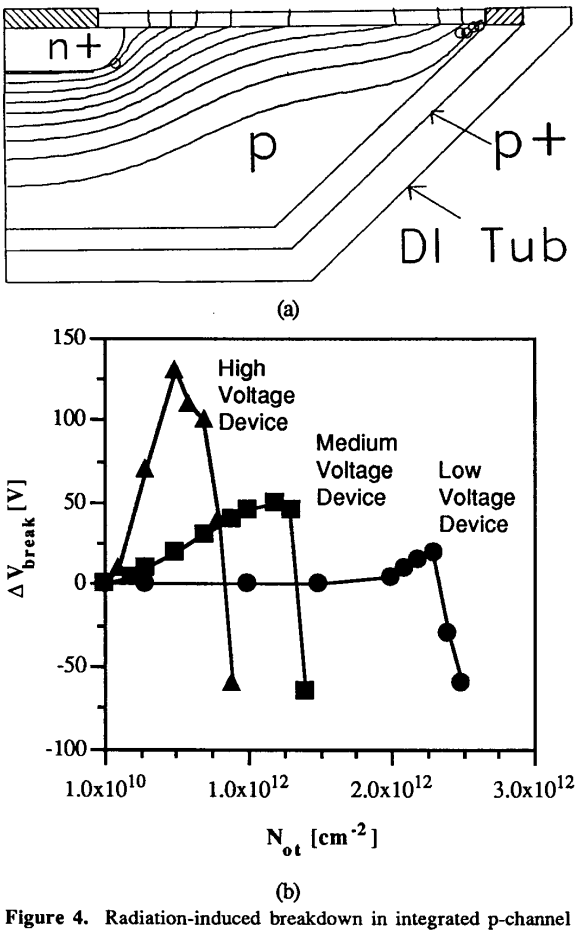


Figure 4. Radiation-induced breakdown in integrated p-channel power devices. a) Medium voltage device of Table 1 with N_{ot} = $1.3x10^{12}$ cm^{-2}, V_{tot} = 215 V. b) ΔV_{break} vs. N_{ot} for all devices of table 1 in DI tubs.

N_{ot} for which sharp reductions in V_{break} first occur is inversely proportional to voltage rating.

In a real device, however, termination structures are always used. Consider the representative DI device of figure 5a, which is equipped with the two-level FP termination illustrated in figure 1b and described in the text of section IV.B. There are two cross-sections of interest in figure 5a, $O - A$ and $O - B$. Through $O - A$, breakdown voltage degradation occurs for smaller N_{ot} than through $O - B$. This is because the source contact acts as a "parasitic FP", inducing N_{plate} along its entire length, which causes $N_{s,crit}$ to be reached for lower values of N_{ot} than through $O - B$. A cross-section through $O - A$ illustrating this effect is shown in figure 5b. In figure 5c, ΔV_{break} versus N_{ot} is plotted for this

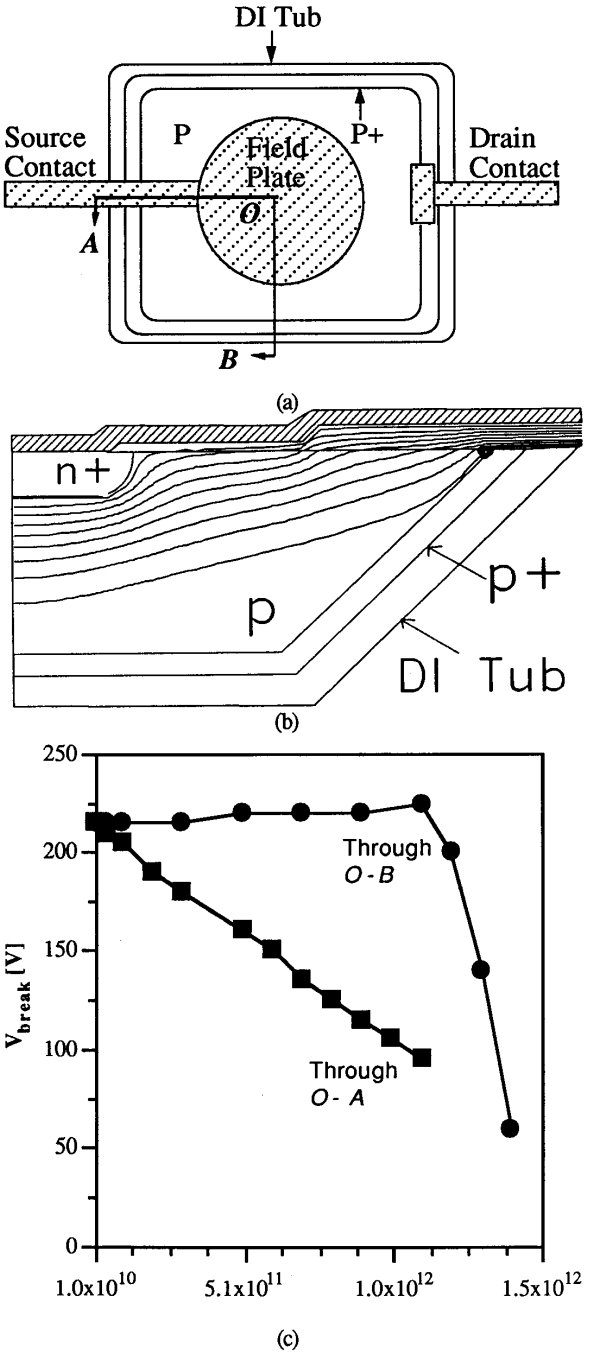


Figure 5. Medium voltage device of Table 1 in a realistic DI application. a) Top view of device. b) Cross section though O - A, demonstrating deleterious effects of the source contact. V_{tot} = 190 V, N_{ot} = $2x10^{11}$ cm^{-2}. c) Breakdown voltage vs. N_{ot} for O - A and O - B cross-sections.

device through both cross-sections $O-A$ and $O-B$, indicating that the $O-A$ cross-section limits the breakdown perfomance of the DI device, as has been reported elsewhere [15].

It is of interest to note that the phenomenon described above is not restricted to p-channel power device applications. The analogy between this case and that of a negative power supply line over a p-tub in a CMOS application, for instance, is apparent.

C. *General Observations*

Ionizing radiation can degrade the performance of all p-channel power devices. The degradation, which depends strongly on the termination structure and isolation technology of the device, is a direct result of the spreading of the depletion region beyond its pre-rad boundary via V_{edge}. It follows that V_{edge} must be controlled in an efficient p-channel termination/isolation scheme.

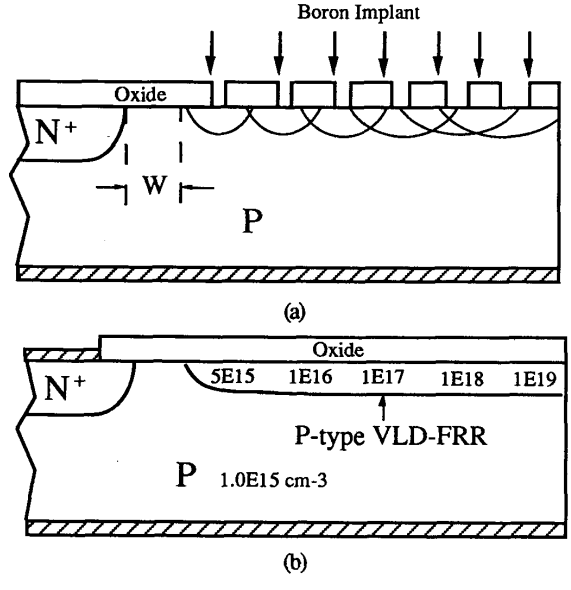


Figure 6. Conceptual illustration of the VLD-FRR. a) Ion implantation of boron takes place through specially-defined windows. The windows increase in thickness and decrease in spacing with lateral distance. W is the pre-rad depletion region width. b) A smoothly-varying VLD-FRR is obtained when boron diffuses in the anneal/drive-in step. The net positive charge in the VLD-FRR will compensate the radiation-induced negative charge, N_s, allowing redirection of the equipotential lines through the Si-SiO_2 interface without crowding.

VII. Termination/Isolation Strategies

In addition to the general statements about the goals of a termination structure outlined in section III, any rad-hard p-channel power device must meet two additional requirements: a) it must confine the depletion region to an acceptable region for all possible values of N_{ot}, and b) it must meet the breakdown voltage specification of the device for all possible values of N_{ot}. As a practical consideration, compatibility with standard planar processes is highly desirable.

In terms of previously defined variables, a method to redirect V_{edge} through the top of the device that avoids equipotential crowding for all values of N_{ot} is needed. To accomplish this task, a new type of termination/isolation technique is proposed: the VLD-FRR, which is an acronym for Variation of Lateral Doping–Field Reduction Region. The concept of a field-reduction region (FRR) has been described and implemented [15], and several ways of smoothly varying the lateral doping of an implant (VLD) for junction termination purposes have been described and implemented as well [16, 17, 18]. A combination of the two techniques will allow efficient redirection of V_{edge} through the device's surface.

The proposed fabrication method is illustrated qualitatively in figures 6a and 6b. This technique will work for integrated as well as discrete devices, and although it may represent an increase in device area, it ensures predictable and stable breakdown voltage for an extended range of N_{ot}. Proper selection of the implant dose, and the range of charge values (i.e., width and spacing of the windows), are, in general, device-specific. The obvious tradeoff is that of area versus performance; by using more lateral distance to vary the VLD-FRR's doping, improved breakdown performance can be expected.

VIII. Conclusion

Two-dimensional simulation has shown that n- and p-channel power-MOSFETs behave differently when exposed to ionizing radiation. These differences, which are not typically accounted for in the design of termination structures, can lead to poor breakdown performance of p-channel devices. The presence of V_{edge} for $N_{eff} > 2\ N_{sub}$ has been demonstrated for all p-channel devices, and the implications of V_{edge} have been examined for FP and FLR termination structures, as well as for various isolation technologies. A VLD-FRR termination/isolation scheme is proposed to counter the effects of V_{edge} for all types of p-channel power devices in radiation environments.

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