Analysis of Breakdown Phenomena in High-Voltage Electron Devices

Qiming Wu
Chimin Yen
Francois E. Cellier

Department of Electrical and Computer Engineering
University of Arizona
Tucson, Arizona 85721
(602) 621-6192

ABSTRACT

This paper presents a program for the two-dimensional simulation of electron devices with high reverse bias voltage together with computational results obtained by using this program. In order to compute the numerical solution within reasonable execution time, the physical model is simplified in that the effect of the emitter current has been neglected. The partial differential equations (PDEs) describing the device have been discretized by use of finite differences, and a Newton iteration approach was used for linearization. Finally, the resulting set of linear algebraic equations is solved by use of several ELLPACK modules. The program is sufficiently flexible for the simulation of devices exhibiting a complex topology that consists of several different materials. At hand of examples, it is demonstrated that this program is an efficient tool for the simulation of industrial high-voltage devices. The computational results are found to be reliable and reasonable.

1. INTRODUCTION

Breakdown voltage is an important parameter in high voltage electron devices. The most frequent causes for the breakdown of a device are avalanche multiplication and punch through. For devices manufactured in planar technology, the breakdown usually occurs either on the Silicon surface or at curved junction regions in the bulk. In order to increase the breakdown voltage, the effects of various device parameters, such as the doping distribution, the junction depth, and the charges at the interface were analyzed, and several topological structures were investigated that are known to raise the breakdown voltage such as floating field limiting rings, floating metal rings, and field plates (Adler et al. 1977; Boisson et al. 1986; Yilmaz and Van Dell 1985). Since no analytic methods exist that allow us to evaluate breakdown phenomena directly, two-dimensional device simulation is the appropriate technique to analyze the influence of technological parameters and device topology on the breakdown voltage.

This research was supported by Burr Brown Corp.

TRANSACTIONS of The Society for Computer Simulation
ISSN 0740-6797/89$2.00 + .10

Volume 6, Number 1, pp. 43-60

For the optimization of high voltage devices, the design engineer needs to compute the electric potential and field distributions inside the device, and from there determine the location where the electric field assumes its highest value. It is at this location where the breakdown of the device occurs. The breakdown voltage can either be estimated by looking at the highest field points (breakdown usually occurs around 250 to 300 kV/cm), or, more accurately, by computing the ionization integral over the electric field distribution (Hwang and Navon 1984).

The device engineer would like to study how modifications in device structure and technological parameters can influence the field distributions. Evaluation of the breakdown voltage by itself is insufficient as it does not give the design engineer a clue as to which type of modification may be successfully employed to increase the breakdown voltage. Our two-dimensional device simulator (ASEPS) is able to compute all pertinent distributions and the ionization integral efficiently and accurately, and has proven very useful in assessing the breakdown behavior of high-voltage devices.

In Section 2, the physical model used by the simulator is briefly described, and the simplifications inherent in the model are discussed together with their impact as to the type of questions that the device simulator can answer.

In Section 3, the numerical techniques used in the simulation, i.e. the discretization of the PDEs, the linearization of the nonlinear equations, and the solution of the resulting linear algebraic equations, are described.

In Section 4, the capabilities of the simulator are introduced. Devices may be composed of several different materials, and may have several surface structure layers.

Computational results are presented in Section 5. Various types of devices have already been simulated by use of the new device simulator, and the obtained simulation results were compared to measurements taken on the devices themselves. The simulation results look reasonable and reliable.

Finally, Section 6 presents conclusions.

2. THE PHYSICAL MODEL

High voltage transistors fabricated in planar technology usually have two different kinds of isolation types: dielectric isolation and p-n junction isolation. Typical samples of bipolar transistors are shown in Fig. 1. The structures of high voltage devices vary also, such as in Fig. 1(a) where there is a floating field ring between collector and base electrodes.

In order to simulate high voltage devices with different kinds of isolation types and structures, the device simulator must have the ability to simulate devices with non-rectangular domains and different kinds of floating field rings.

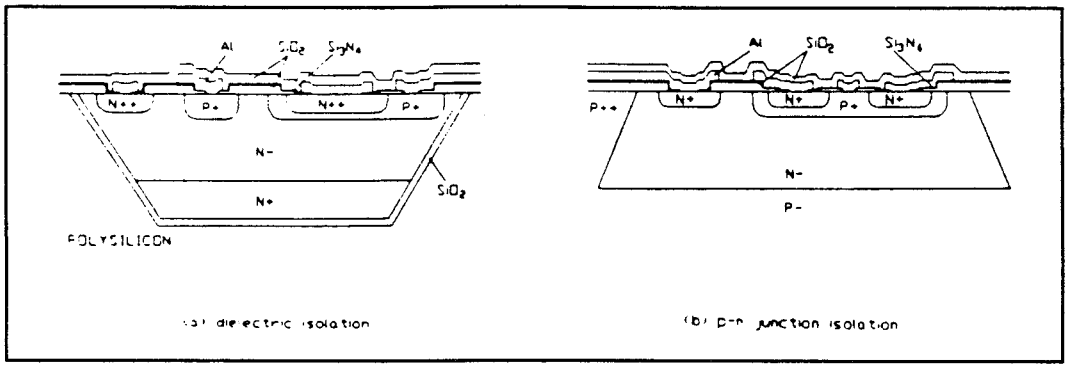

Figure 1. Typical Samples of Bipolar Transistors

For two-dimensional device simulation, the basic semiconductor equations, i.e. the Poisson equation and the current continuity equations, must be solved. The numerical solution of this problem is very time consuming, and the convergence range and speed of the Newton iteration depends heavily on the applied reverse bias voltage. Previously available device simulators such as BAMBI (Franz and Franz 1985) work acceptably well for low-voltage devices, but fail entirely when used for high-voltage devices. When the reverse bias voltage of the junction is increased to several hundred volts, this set of equations becomes almost impossible to solve numerically.

Our experiences with BAMBI (Franz and Franz 1985) and PISCES (Rafferty et al. 1985) have shown that, even for a simple reverse biased p-n junction, the number of iterations required for convergence of the set of elliptic partial differential equations (PDEs) comprised of the Poisson equation and the two current continuity equations depends heavily on the applied voltage. The higher the applied voltage, the larger is the number of Newton-Raphson iterations required for convergence of the set of nonlinear PDEs. If the applied voltage is chosen sufficiently high (in the tested configurations around 50 Volts), the Newton-Raphson iteration fails to converge altogether.

This problem is traditionally tackled by ramping up the supply voltage, i.e. a small voltage is applied first for which the potential distribution inside the device is computed. Thereafter, the voltage is incremented by a certain amount, and a new potential distribution is computed using the previous distribution as an initial condition for the new iteration of the nonlinear equations. This procedure is repeated until the supply voltage has reached the desired value. In this way, high voltage devices can be simulated correctly, but, in order to obtain convergence, the maximum allowable incremental voltage between successive solutions of the nonlinear PDEs decreases drastically with increasing voltage. This approach therefore is number

crunching at its best.

Under high reverse bias voltage on the base-collector junction, the physical model can be simplified. For the analysis of breakdown phenomena, the currents in the device can be neglected, and also the emitter can be eliminated, since the collector-base breakdown voltage is essentially responsible for the breakdown of the device (Hwang and Navon 1984; Yasuda and Kurata 1980). With these simplifications, the quasi-Fermi potentials ϕ_n and ϕ_p can be assumed constant. ϕ_n can be approximated by its *n*-contact bias value, and ϕ_p can be approximated by its *p*-contact bias value, i.e. $\phi_n = V_r$ and $\phi_p = 0$, where V_r is the value of the reverse bias voltage on the base-collector junction. The electron concentration *n* and the hole concentration *p* are thus only functions of the electrical potential. Inside the semiconductor region, the problem can therefore be simplified to solving a (nonlinear) Poisson equation only.

This approach is beneficial for two reasons: (i) The time needed for computing the solution of the linearized set of equations is reduced since we are confronted with a simpler problem; and (ii) The convergence of the Newton-Raphson algorithm is much improved, i.e. the number of iterations needed for convergence of the nonlinear problem is drastically reduced, and no ramping is necessary to converge high-voltage devices. The inaccuracy of the obtained solution as a result of neglecting the device currents is minimal since they are very small in the vicinity of breakdown.

However in order to simulate high-voltage devices realistically, we must take into consideration the regions of insulators and metal electrodes and also eventual charges on the interface between semiconductor and insulator. Accurate modeling of these surface phenomena is important as the breakdown of the device will most frequently happen at the surface of the device, and depends strongly on the shape of the equipotential lines where they intersect the surface.

The normalized equations that are solved by the device simulator together with their corresponding boundary conditions for a typical domain, such as the one shown in Fig. 2, are given as follows.

(1) Semiconductor region (Poisson equation):

$$\partial^2\Psi/\partial x^2 + \partial^2\Psi/\partial y^2 = -(\Phi_p * \exp(-\Psi) - \Phi n * \exp(\Psi) + N_d) \quad (1)$$

(2) Insulator region (Laplace equation):

$$\partial^2\Psi/\partial x^2 + \partial^2\Psi/\partial y^2 = 0 \quad (2)$$

(3) Metal region

$$\Psi = V_0 \quad (3)$$

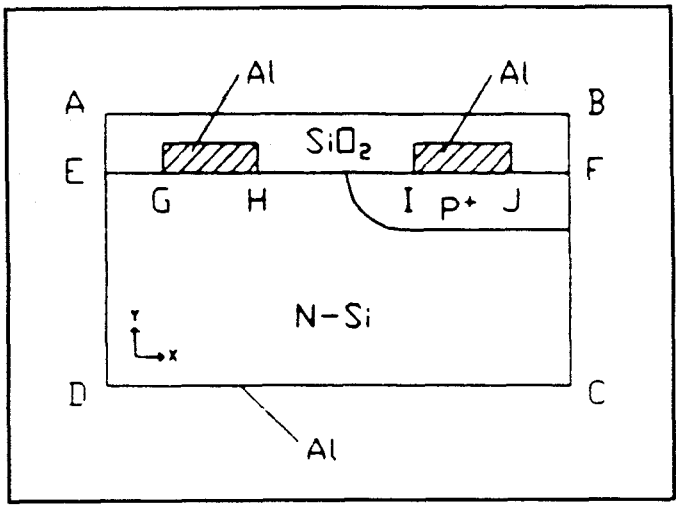

Figure 2. Domain Geometry of a Typical Device

where: Ψ static electric potential, unknown variable
$\Phi_n = e^{-\phi_n}$ ϕ_n: electron quasi-Fermi potential
$\Phi_p = e^{\phi_p}$ ϕ_p: hole quasi-Fermi potential
N_d doping concentration
V_0 known bias voltage

Boundary conditions:

(1) AB:

$$\partial\Psi/\partial y = 0 \tag{4}$$

(2) BC, AD:

$$\partial\Psi/\partial x = 0 \tag{5}$$

(3) EG, HI, JF:

$$\epsilon_s \partial\Psi/\partial y\big|_s - \epsilon_i \partial\Psi/\partial y\big|_i = Q_s \tag{6}$$

where: ϵ_s permittivity of semiconductor
ϵ_i permittivity of insulator
Q_s interface charge density

The procedure of normalizing the equations was e.g. described by DeMari (1968).

The purpose of our device simulation is to allow the investigation of breakdown behavior when the transistor collector is under high reverse bias voltage.

The peak values of electric fields in the semiconductor usually appear in the region around the base-collector junction curvature, the region underneath the oxide layer, and the region near the edge of the isolation in the collector area. Since the regions concerned with the breakdown are near the p-n junction of the collector, it is common practice to simulate only a part of the device rather than the whole transistor.

Our software is capable of simulating rectangular domains as well as non-rectangular domains. If the user is interested in the breakdown around the p-n junction or the simulation of a device with p-n junction isolation, the rectangular geometry can be used. However, users who want to study the effect of dielectric isolation must use the non-rectangular geometry.

In Fig. 3, two different device topologies are depicted. In our program, the following materials can currently be included: Aℓ, AℓSb, CdS, CdSe, CdTe, GaAs, GaSb, Ge, InP, PbS, Si, Si_3N_4, and SiO_2. Insulators and metals can be composed of arbitrary rectangular polygons.

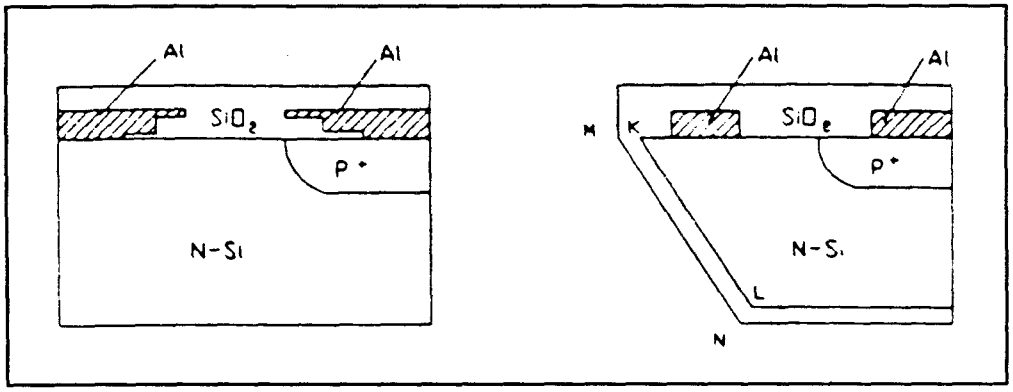

Figure 3. Two Situations for Rectangular and Non-Rectangular Domain

PISCES (Rafferty et al. 1985) offers one simulation mode (carriers=0) in which it operates similarly to ASEPS. However, since PISCES is a much more general program than ASEPS, designed to solve a much larger variety of problems, it has not been as carefully tuned to the simulation of the breakdown behavior of power devices. In particular, PISCES cannot be used to simulate devices with floating structures. The only way that a floating structure can be simulated in PISCES is by declaring it as a current contact with zero current. However, in this case, PISCES will not accept the *carriers=0* instruction, and we are forced to solve the current continuity equations together with the Poisson equation.

3. THE NUMERICAL SOLUTION

The above specified Poisson equation is a highly nonlinear elliptic PDE.

The numerical solution of the Poisson equation includes discretization of the PDE, linearization of the nonlinear equations, and solution of the set of resulting linear algebraic equations.

Initially, the ELLPACK (Rice and Boisvert 1985) toolkit for the solution of general elliptic PDEs was used to determine the optimal combination of algorithms for this task (Wu and Cellier 1986). It was found that finite differences worked better for the discretization of the Poisson equation than finite elements. This is due to the fact that the resulting equations are much more sparse when finite differences are used. Newton iteration worked well for the linearization of the resulting set of nonlinear algebraic equations, and the finally obtained set of linear algebraic equations could be solved by two ELLPACK modules - MINIMUM DEGREE and SPARSE GE NO PIVOTING.

However after determination of the optimal combination of algorithms, we had to rewrite the program for increased efficiency. By extracting a larger percentage of code out of the Newton iteration into an initialization phase, and by tuning the algorithms to our particular task, the execution speed of the program has been increased by about a factor of twenty. Thus, a simple p-n junction which initially required between thirty minutes and one hour of execution time on a VAX-11/750, now executes in about two minutes. A representative industrial device such as the transistors depicted in Fig. 1 executes in roughly thirty to ninety minutes on the same VAX, and requires about five to fifteen minutes of execution time on an FPS 164 array processor which is the machine that we normally use for our simulations. The execution time depends on the numerical condition of the simulated device. It is primarily determined by the number of Newton iterations required for convergence. Generally, devices with floating rings require about three to five times more iterations than devices without such floating rings.

At the time when we experimented with ELLPACK, successive overrelaxation (SOR) as an alternative to Gaussian Elimination (GE) was rejected since we could not get the iterative SOR algorithm to converge. More recently, it was determined that the divergence had not been caused by the Poisson equation itself, but rather by the way in which ELLPACK chose the grid points in the neighborhood of the device boundaries. In order to guarantee convergence of the SOR algorithm, the resulting matrix of the linearized model should be an S-matrix (Wachspress 1966). This can be achieved by placing the grid points at the device boundaries as depicted in Fig. 4.

In our latest software release, we have implemented this algorithm as an alternative to the previously used GE algorithm, and the new code works very reliably. The new algorithm works much more efficiently than the previously used GE algorithm, in particular for highly structured devices which call for a larger number of discretization points. The GE algorithm had been used for structures that could be simulated accurately with 24 by 36 grid points, whereas the now implemented SOR algorithm works also very efficiently when a much larger number of grid points is

required. We recently simulated a device with eight floating rings which required 150 by 200 grid points. We were able to simulate this device on a VAX-11/3600 in 35 minutes.

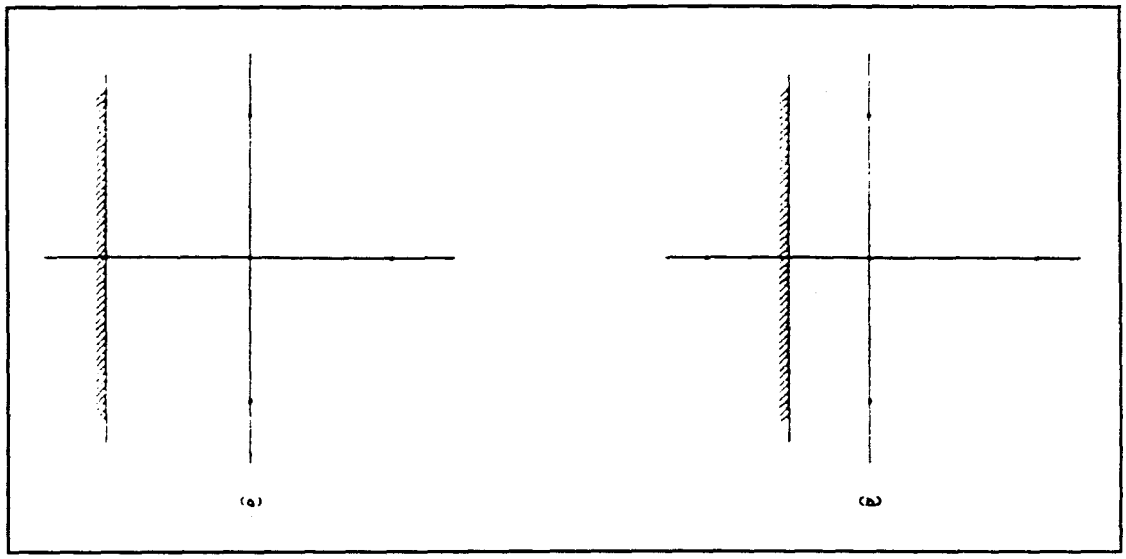

Figure 4. Boundary Nodes: (1) Dirichlet Boundary, (2) Neumann Boundary

In our program, we consider the existence of floating field limiting rings or floating metal rings. The program includes special algorithms for the treatment of floating field rings. The idea behind the algorithm for the determination of the potential on a floating ring is based on the fact that there is no net current into or out of a field ring. In order to satisfy this criterion, the junction underneath the floating ring can neither be completely reverse biased nor heavily forward biased. The potential of the ring must equal the lowest potential along the metallurgical ring-substrate junction minus a built-in potential (Adler et al. 1977). For floating metal rings, the floating rings are always in thermal equilibrium with the semiconductor surface at the contact points, and they keep the surface potential constant at the contact values (Yilmaz and Van Dell 1985). During Newton iteration, this criterion is continuously applied to modify the potential of the floating ring until the final solution is consistent with the physics of the problem.

4. PROGRAM EXECUTION

A pictorial representation of the overall program flow of the device simulation is given in Fig. 5.

Our device simulator can be characterized by the following features:

1. For the two-dimensional Poisson equation, thousands of discrete nodes

may be required. The numerical solution of this partial differential equation requires long execution time, and consumes a large amount of data storage space. It is therefore very important to optimize the program for execution speed. However, also storage requirement is a point of consideration, as high speed computers (such as the FPS-164) do not often provide for memory management.

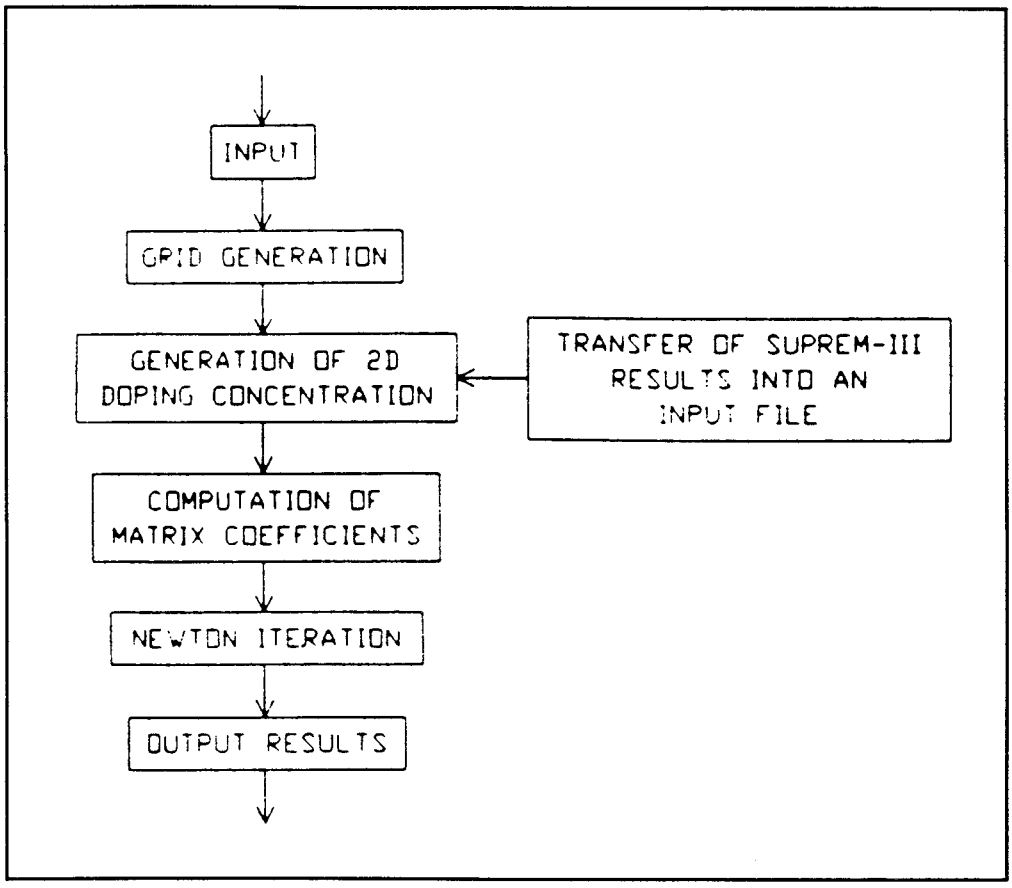

Figure 5. Overall Program Flow Chart

A large percentage of the total execution time is spent in the Newton iteration. Thus, the code inside the iteration loop is the most time critical portion of the code, and therefore deserves the largest attention with respect to possible code optimizations. In particular, all program segments that can be extracted out of the iteration loop should be placed in an initialization phase which is executed only once. Major portions of the coefficient matrix and right hand side terms of the resulting linear equations are invariant to the iteration process, and thus, these terms can be computed once and forever before the Newton iteration is started. Inside the iteration loop remain the computation of the varying terms in the coefficient matrix and right hand side (5-POINT STAR), and the execution of the resulting set of linear equations (either by using the MINIMUM DEGREE indexing scheme together with

the SPARSE GE NO PIVOTING algorithm, or by using the SUCCESSIVE OVERRELAXATION technique).

In our installation, an array processor (FPS-164) is coupled to a VAX-11/750, allowing us to execute FORTRAN-coded programs on either of the two machines. A comparison between the execution times required by the two machines for one step of Newton iteration of a particular device is listed in Table 1.

TABLE I. COMPARISON OF EXECUTION TIME OF ONE STEP OF NEWTON ITERATION BY USING VAX-11/750 AND FPS-164 FOR A PROBLEM WITH 13x22 GRID POINTS (NON-UNIFORM)

	EXECUTION TIME (SECONDS)	
	FPS-164	VAX-11/750
5-POINT STAR	0.01	0.11
MINIMUM DEGREE	0.14	1.03
SPARSE GE NO PIVOTING	0.17	1.82
TOTAL TIME	0.32	3.06

From the above result, we can see that, on the array processor, one iteration requires roughly ten percent of the execution time needed when using the VAX. Between 20 and 30 Newton iterations are required for convergence of a device with 100V to 400V reverse bias voltage if the device does not contain any floating ring. The number of Newton iterations required for a device with floating ring is considerably higher (between 100 and 200). Using the FPS-164, even devices with floating ring require an execution time of a few minutes only. On the VAX however, devices without floating ring can be simulated within a couple of minutes, whereas devices with floating ring may require more than one hour of execution time.

The newly implemented SOR algorithm requires two to three times as many iterations as GE on devices without floating rings, but about the same number of iterations as GE on devices with floating rings. Since the individual SOR iteration step executes about ten times faster than an equivalent GE iteration step for a moderately size grid (24 by 36), SOR is usually preferable over GE, and the speed advantage of SOR grows further with increasing device complexity and increasing number of grid points.

2. The program provides for automatic grid generation. All the user needs to specify is the number of grid points in the two directions that he wants. In most cases, it is more convenient for the user to have the grids generated automatically. However, he can choose to generate the grids manually.

3. The program can interpret the output file of a SUPREM-III (Hansen 1982) process simulation, and convert the one-dimensional doping distribution computed by SUPREM-III into a two-dimensional doping distribution as required by the device simulator. In the SUPREM-III process simulation, the various doping processes are simulated one at a time. The result of each doping process is a one-dimensional doping profile which can be interpreted as a vertical cut through the device from the surface down to the substrate. For the device simulation, we require a two-dimensional doping profile that extends over the entire semiconductor region. ASEPS extracts the doping data from the SUPREM-III output file, generates tables of doping concentration and corresponding depth, and writes these tables onto files. Thereafter, the program takes these preprocessed doping data from the new files, and generates two-dimensional doping distributions by using an elliptic approximation for the transverse distribution on the domain. Thereby, the doping profile depends on the depth only underneath each process window, i.e. for every depth, the doping profile assumes a constant value over the entire mask opening. Outside the mask, an elliptic profile was chosen to represent the lateral diffusion which is a bi-product of the doping process. The maximum extension beyond the mask opening was chosen to be 60% of the junction depth. Several doping processes can take place at the same physical location, and ASEPS is able to superpose the effects of multiple doping.

4. The program structure is kept as flexible and modular as possible to allow new algorithms to be added whenever new types of processes are to be simulated.

5. COMPUTATIONAL RESULTS

The investigation of high reverse voltage planar semiconductor devices has been described in several papers (Adler et al. 1977; Boisson et al. 1986; Hwang and Navon 1984; Sakurai and Ohno 1984; Yasuda and Kurata 1980; Yilmaz and Van Dell 1985). They discuss how physical parameters of the semiconductor, such as its doping concentration, the main junction depth, surface charges, field plates with non-uniform oxide thickness, floating field limiting rings, or floating metal rings influence the field distribution and breakdown voltage. Optimal combinations of device parameters are suggested that help to increase the breakdown voltage.

We simulated several devices with dielectric and with p-n junction isolation similar to those shown in Fig. 1(a) and Fig. 1(b).

1. An industrial device with p-n junction isolation and several layers of different insulation material, such as the one shown in Fig. 1(b), was simulated. Since we were interested in determining the locations of the highest field points near the

p-n junction, only a part of the device was actually simulated. All surface materials including SiO_2, Si_3N_4, and Al were represented in the model, and the device topology (dimensions) was kept as close to reality as possible. The doping concentration was taken from SUPREM-III process simulation results. The substrate was n-Si, and its doping concentration was 1×10^{15} cm^{-3}. The bottom of the substrate was p-Si (grounded). The contour of the electric potential distribution of the p-n junction with 100 Volts reverse bias is shown in Fig. 6.

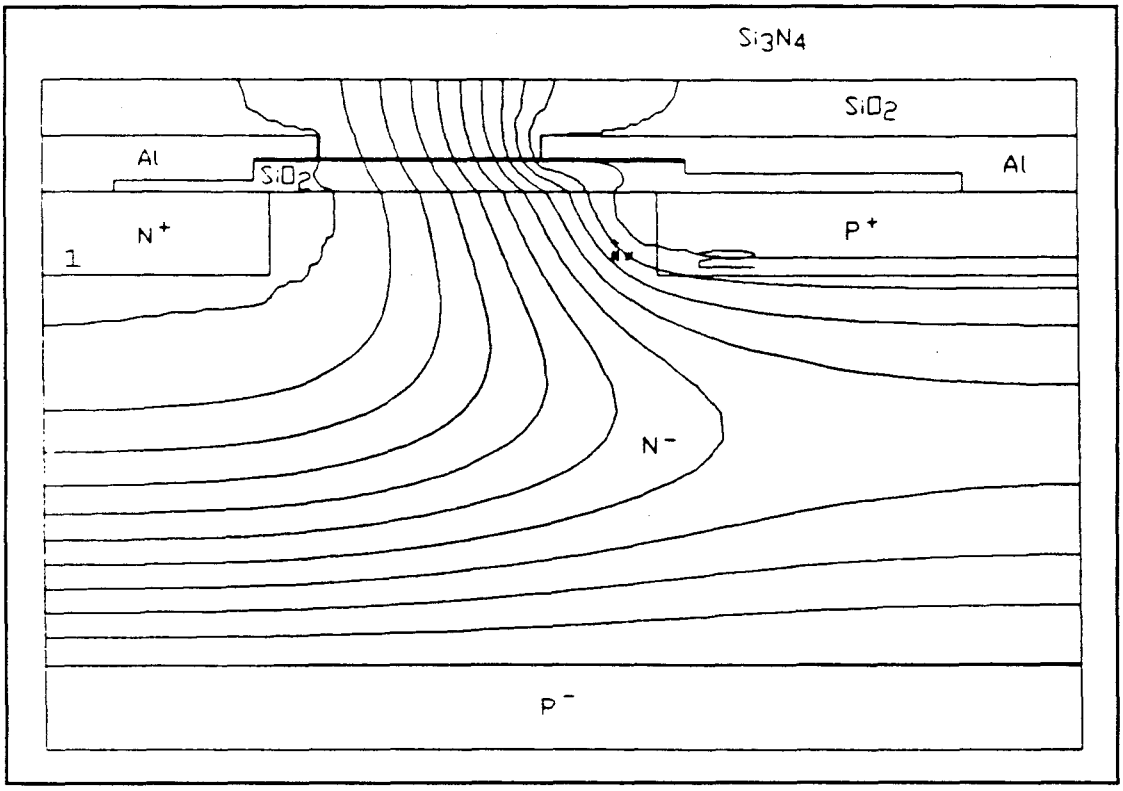

Figure 6. Contour Plot of the Electric Potential Distribution of a p-n Junction with 100 Volts Reverse Bias

2. In Fig. 7, the potential distribution of the same device with 200 Volts reverse bias is shown. The Si_3N_4 layer was meanwhile eliminated as previous simulation had shown that its influence on the potential distribution was minimal. There are three highest field points in the silicon: two of them are on the surface, and the third point is on the junction curvature. The highest field value is 250 kV/cm. This result is very close to the experimentally determined value. The physical data (topology and doping profile) for this simulation were taken from an actually built device. Measurements determined the breakdown to occur at 197 Volts. The simulation confirmed through the highest field point value and the computation of the

ionization integral that, with 200 Volts reverse bias, the device is just at the edge of breakdown.

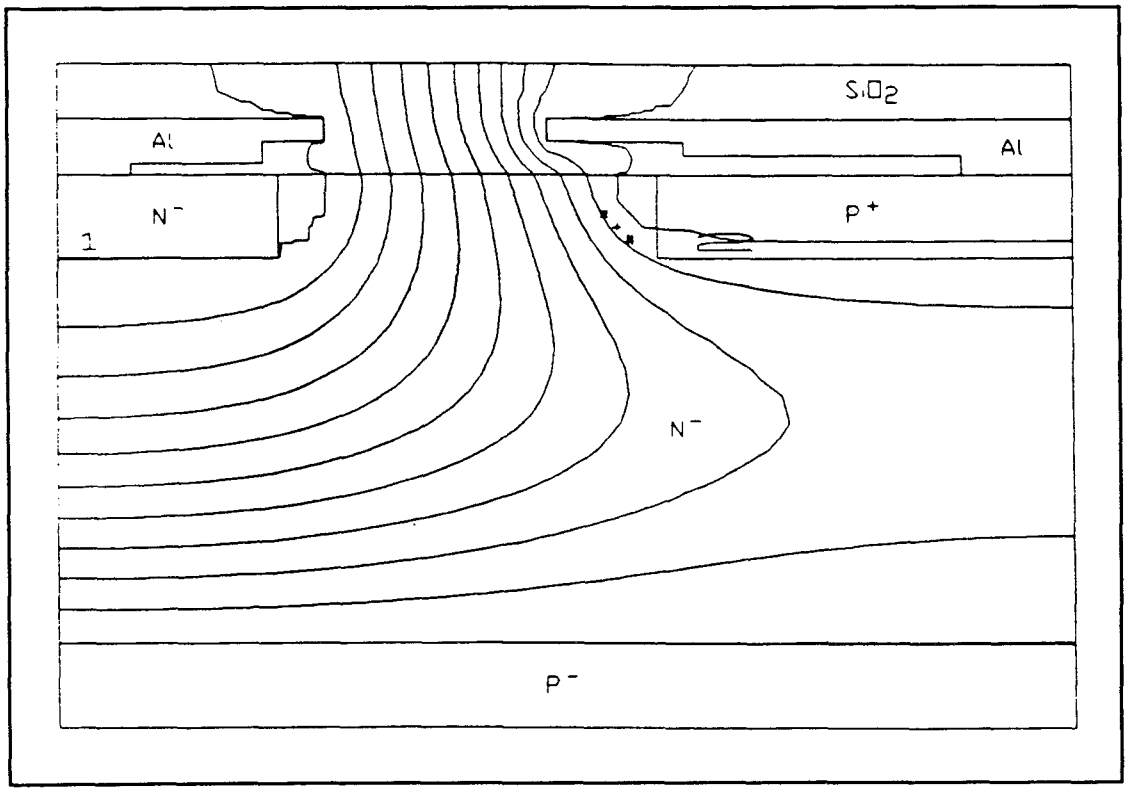

Figure 7. Contour Plot of the Electric Potential Distribution of a p-n Junction with 200 Volts Reverse Bias

3. In Fig. 7, the right side electrode covered the p-n junction. The electrode extended to the left and formed a field plate. This is one of the standard techniques used to increase the breakdown voltage of a device. To study the effectiveness of this measure, we simulated the same device once more, this time with a shortened right side electrode and elimination of the field plate. Computational results for this modified geometry are presented in Fig. 8. Comparing Fig. 7 and Fig. 8, we found that the field plate had caused the field distribution to change, and the equi-potential lines to move to the left, so that the electric field intensity near the p-n junction curvature and the surface was indeed reduced. By removing the field plate, the highest field value was increased from 250 kV/cm to 284 kV/cm, and the highest field point moved from the surface of the silicon to the p-n junction curvature. Measurements for this device indicated that breakdown occurred at a reverse bias voltage of 134 volts. Also this result has been confirmed by our simulation. If we reduce the applied reverse bias voltage from the previous 200 volts to new 135 volts, we see that the highest field value is again around 250 kV/cm which indicates that the device is near breakdown.

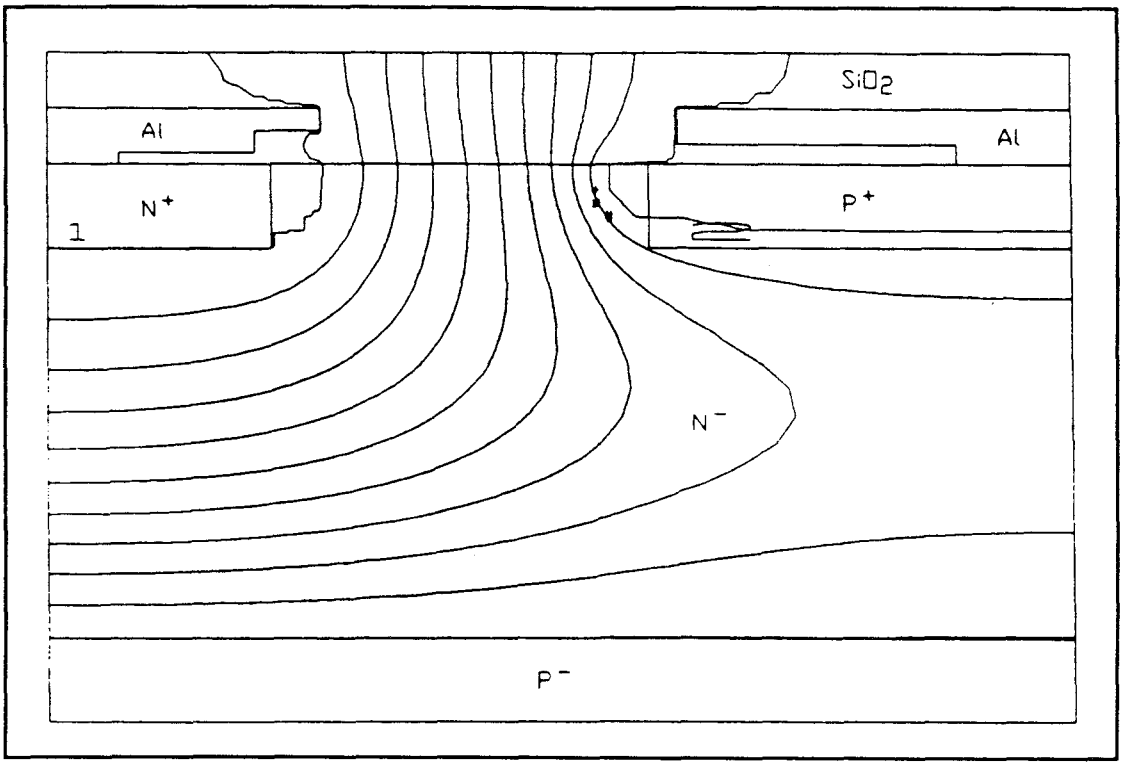

Figure 8. Contour Plot of the Electric Potential Distribution of a p-n Junction with 200 Volts Reverse Bias After Changing the Right Side Electrode Shape.

4. The region near the p-n junction isolation area is shown in Fig. 9. The doping concentration of n-Si was the same as in the above examples. High voltage is applied to the Al electrode. The left side and the bottom of the silicon are grounded. Through the $Si0_2$ layer, the high reverse bias voltage of the electrode directly influences the highest field location on the surface of the p-n junction high resistance area. The thickness of the $Si0_2$ layer t_{ox} changes the value of the highest field in the silicon. In Fig. 10, the highest electric field intensity in the silicon E_{max} is graphed vs. the oxide thickness t_{ox}. When the oxide layer is thinner, the high reverse bias voltage makes the equipotential lines move closer together on the surface of the p-n junction high resistance area.

5. The same device was simulated once with and once without a floating field limiting ring. The doping concentration was the same as in the above examples. The bottom of the silicon was grounded. Results of these simulations are presented in Fig. 11(a) and Fig. 11(b). Due to the floating ring, the equi-potential lines moved towards the high reverse bias electrode contact region, so the location of the highest field occurred no longer on the p-n junction curvature, and the field near the p-n junction could be reduced.

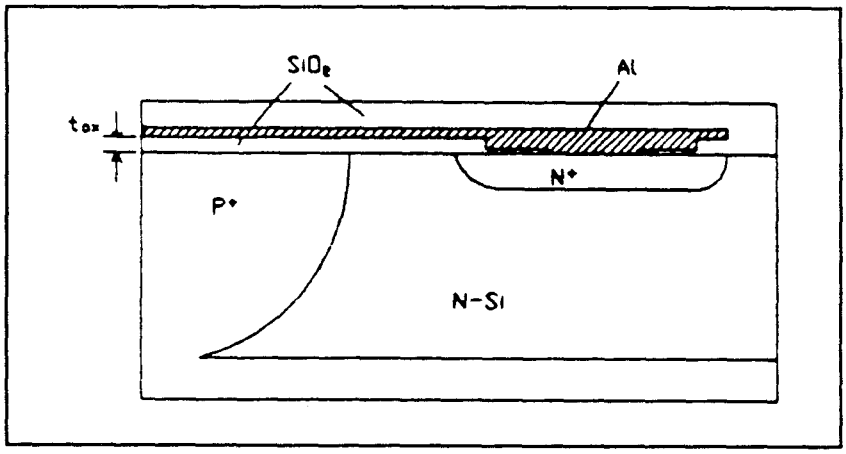

Figure 9. Structure of the Region near the p-n Junction Isolation

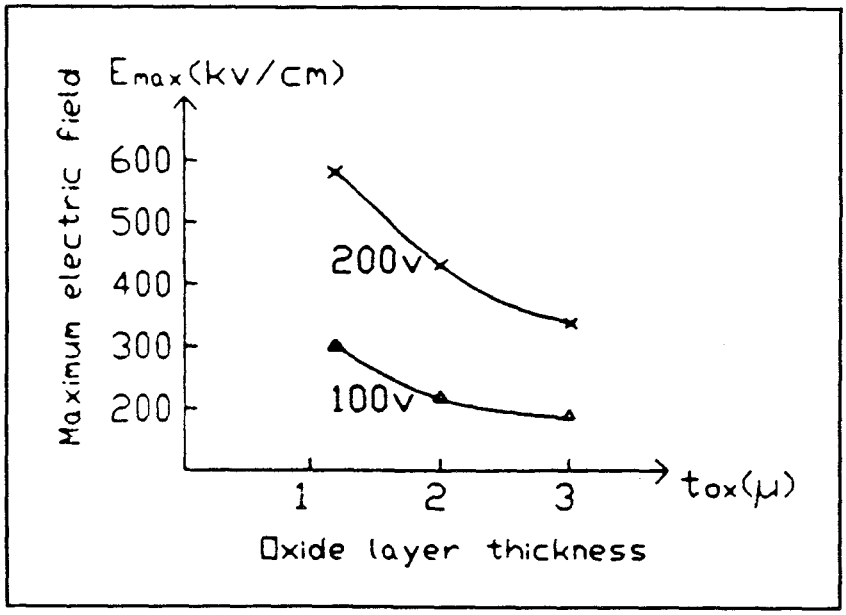

Figure 10. The Highest Electric Field Intensity E_{max} Plotted vs. Oxide Thickness t_{ox}

6. We computed another device with dielectric isolation. This time, we were particularly interested in studying the effect of the dielectric isolation at the slanted edge of the device, and thus, the program for non-rectangular geometry had to be used. Again, the left side and the bottom of the silicon are grounded. A reverse bias voltage of 100V was applied to the p-n junction. In Fig. 12, computational results are shown. It turns out that here the highest field point is on the interface between the dielectric isolation layer and the silicon.

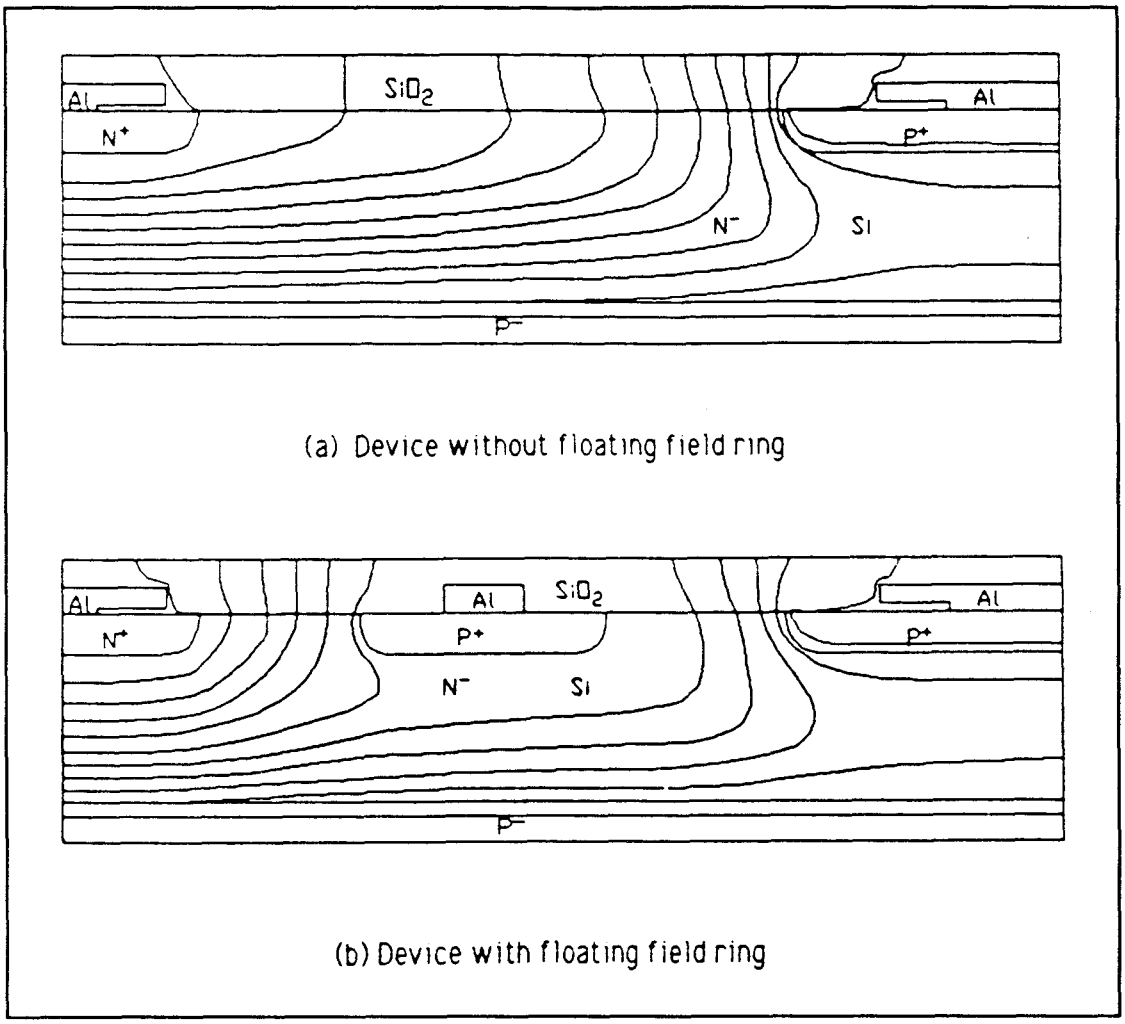

Figure 11. Comparison of a Device With and Without Floating Field Limiting Ring

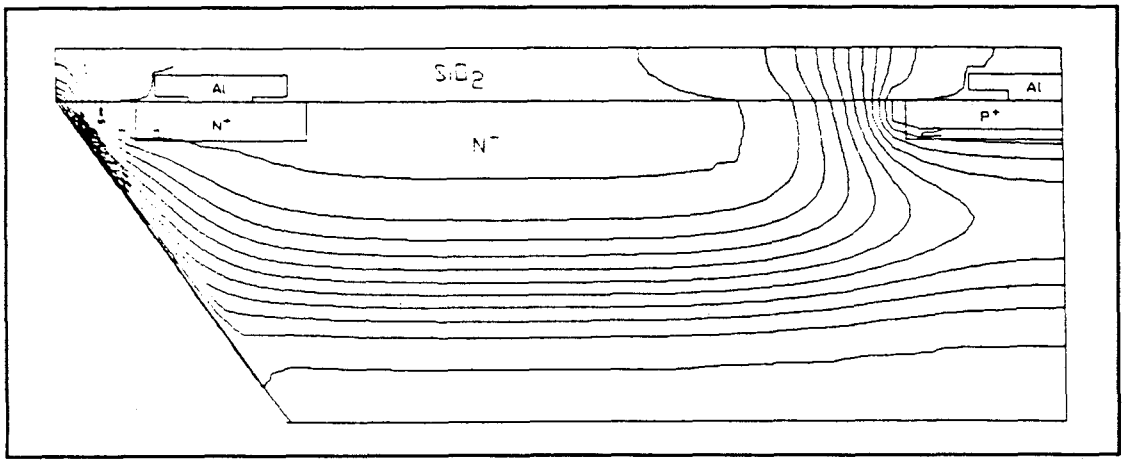

Figure 12. Simulation of a Device with Dielectric Isolation

6. CONCLUSIONS

In order to investigate high reversed bias devices, a program for simulation of such devices was developed.

Computational results have shown that this program can both efficiently and reliably be used to simulate different kinds of high-voltage devices. Since the program allows the devices to consist of several different materials with arbitrary (rectangular) shapes, it is sufficiently flexible for simulation of a large variety of different industrial high-voltage devices. Using this program, comparison between several different layouts of device structures is made easy.

While the device structures shown in this paper are all of the bipolar type, ASEPS has recently been enhanced to operate also on other types of device structures such as power MOSFET devices.

REFERENCES

Adler, M.S., Temple, Y.A.K., Ferro, A.P., and Rustay, R.C., 1977. "Theory and Breakdown Voltage for Planar Devices with a Single Field Limiting Ring," *IEEE Trans. Electron Devices,* **ED-24,** pp. 107-112.

Boisson, Y., LeHelley, M., and Chante, J.P., 1986. "Computer Study of a High-Voltage p-π-n$^-$-n$^+$ Diode and Comparison with a Field-Limiting Ring Structure," *IEEE Trans. Electron Devices,* **ED-33,** pp. 80-84.

DeMari, A., 1968. "An Accurate Numerical Steady-State One-Dimensional Solution of the p-n Junction," *Solid State Electronics,* **11,** pp. 33-58.

Franz, A.F. and Franz, G.A., 1985. *BAMBI 1.0 User's Guide,* Internal Report, Institut für Allgemeine Elektrotechnik and Elektronik, Abt. Physikalische Elektronik, Techn. Universität Wien.

Hansen, S.E., 1982. *SUPREM-III User's Manual,* Internal Report, The Board of Trustees of Stanford University.

Hwang, K. and Navon, D.H., 1984. "Breakdown Voltage Optimization of Silicon p-π-ν Planar Junction Diodes," *IEEE Trans. Electron Devices,* **ED-31,** pp. 1126-1135.

Rafferty, C.S., Pinto, M.R., and Dutton, R.W., 1985. "Iterative Methods in Semiconductor Device Simulation," *IEEE Trans. Computer-Aided Design,* **CAD-4,** pp. 461-471.

Rice, J.R. and Boisvert, R.F., 1985. *Solving Elliptic Problems Using ELLPACK,* Springer-Verlag, New York.

Sakurai, T. and Ohno, T., 1984. "Structural Analysis and Experimental Characteristics of High-Voltage Bipolar Transistors with Shallow Junctions," *Japanese Journal of Applied Physics,* **23,** pp. 413-419.

Wachspress, E.L., 1966. *Iterative Solutions of Elliptic Systems,* Prentice Hall, Englewood Cliffs, N.J.

Wu, Q. and Cellier, F.E., 1986. "Simulation of High-Voltage Bipolar Devices in the Neighborhood of Breakdown," *Mathematics and Computers in Simulation,* **28,** pp. 271-284.

Yasuda, S. and Kurata, M., 1980. "Two-Dimensional Field Distribution Analysis of Reverse Biased p-n Junction Devices," *Solid State Electronics,* **23,** pp. 1077-1084.

Yilmaz, H. and Van Dell, W.R., 1985. "Floating Metal Rings (FMR), A Novel High-Voltage Blocking Technique," *IEEE Electron Device Letters,* **EDL-6,** pp. 600-601.

Qiming Wu *graduated from the Department of Radio and Electronics Engineering of Tsinghua University in 1961 when she joined the faculty of Tsinghua University. Her research interests are concerned with computer-aided design of integrated circuits. Between 1961 and 1965 she worked on the theory and application of photoelectric semiconductor devices. Between 1966 and 1972 she was responsible for the designs of integrated MOS technology for electronic calculators and other digital systems. In 1973, Dr. Wu started to work on the development of software for LSI layout and LSI circuit simulation. In 1980, she became responsible for the design of software for modeling semiconductor devices. In spring of 1985, she joined the University of Arizona as a Visiting Research Associate for a two year period.*

Chimin Yen *received his Bachelor of Science in 1984 from the University of Arizona with a major in Engineering Mathematics and a Master of Science in 1988 from the same university with a major in Electrical Engineering. Currently, Mr. Yen works for Mentor Graphics Corp. in San Jose, California. His job is related to modeling the behavior of semiconductor devices.*

Francois E. Cellier *received his B.S. in Electrical Engineering from the Swiss Federal Institute of Technology (ETH), Zurich, in 1972, his M.S. in Automatic Control in 1973, and his Ph.D. in Technical Sciences in 1979, all from the same university. Following his Ph.D., Dr. Cellier worked as a Lecturer at ETH Zurich. He joined the University of Arizona in 1984 as an Associate Professor. Dr. Cellier's main scientific interests concern modeling and simulation methodology, and the design of advanced software systems for simulation, computer-aided modeling, and computer-aided design. He has designed and implemented the GASP-V simulation package, and he was the designer of the COSY simulation language which has meanwhile become a standard by the British Ministry of Defense. Dr. Cellier has authored or co-authored more than forty technical publications, and he has edited two books. He served as a chairman of the National Organizing Committee (NOC) of the Simulation '75 conference, and as a chairman of the International Program Committee (IPC) of the Simulation '77 and Simulation '80 conferences, and he has also participated in several other NOC's and IPC's. He is associate editor of several simulation related journals, and he served as vice-chairman of two committees on standardization of simulation and modeling software. Memberships include SCS and IMACS.*