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Bit-Exact ECC Recovery (BEER):

Determining DRAM On-Die ECC Functions by Exploiting DRAM Data Retention Characteristics

Minesh Patel, Jeremie S. Kim

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MICRO 2020 (Session 2C – Memory)

PROBLEM

DRAM on-die ECC **complicates** reliability studies
by **obfuscating** DRAM error characteristics

GOAL

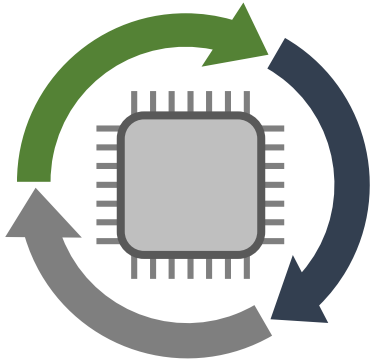
Understand **exactly how** on-die ECC obfuscates errors

CONTRIBUTIONS

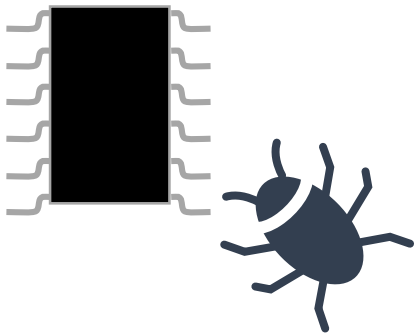
1. **BEER:** Determines a DRAM chip's unique **on-die ECC function** (i.e., its parity-check matrix)
2. **BEEP:** Infers **raw bit error** locations of error-prone cells using only the observed uncorrectable errors

EVALUATIONS

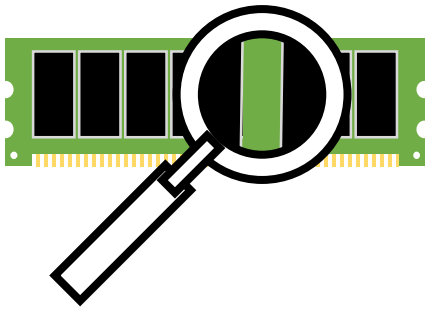
1. **Experiment:** Demonstration using 80 LPDDR4 DRAM chips
2. **Simulation:** Correctness and practicality for >100,000 representative on-die ECC codes (4-247b ECC words)



System Architects
Design Error Mitigations



Test Engineers
Third-Party Testing

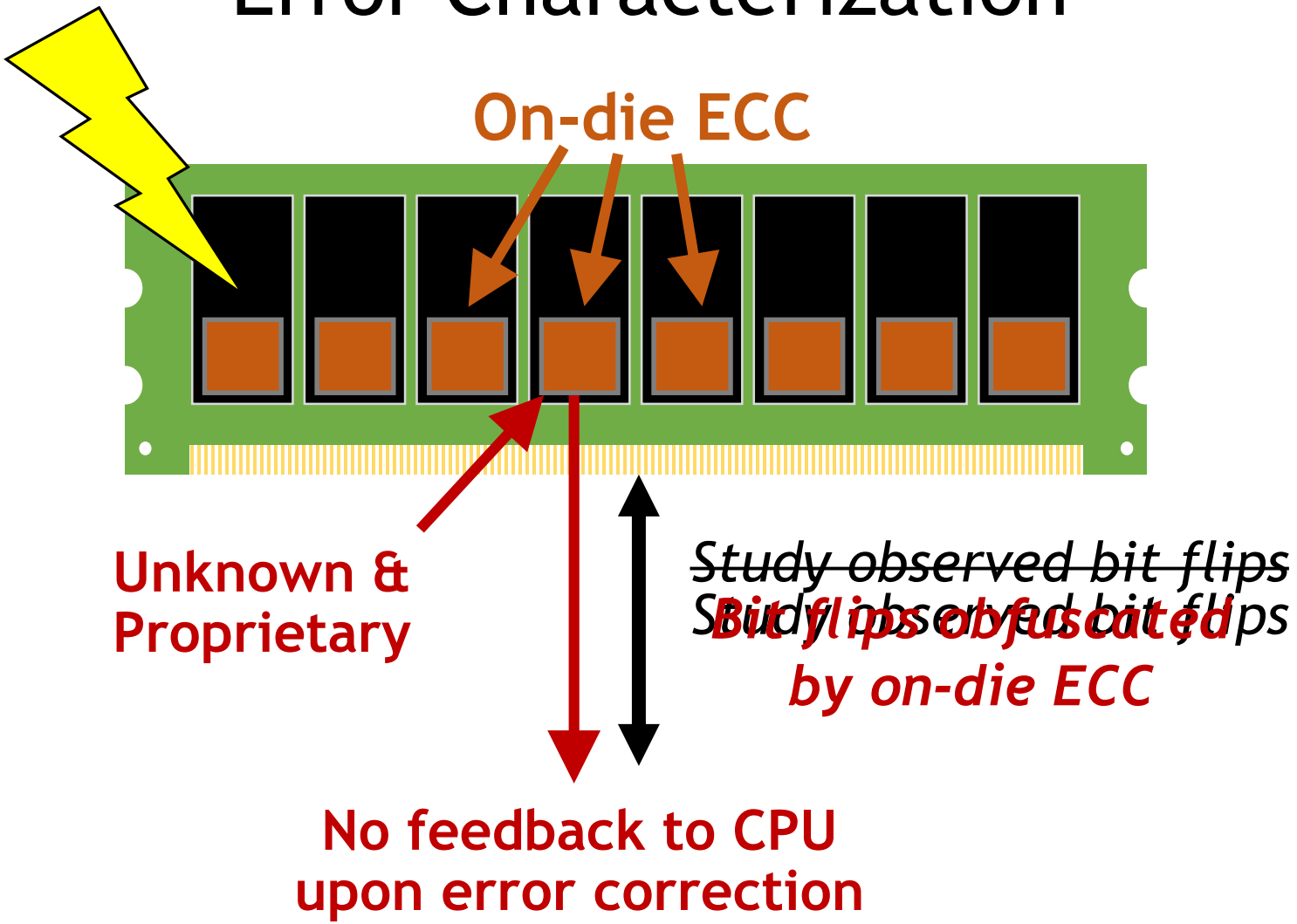


Research Scientists
Error-Characterization

Need to understand
a DRAM chip's **reliability characteristics**

Inter-chip variation?
'Weak' cell locations?
Aggregate failure rates?
Temperature dependence?
Statistical error properties?
Minimum operating timings?

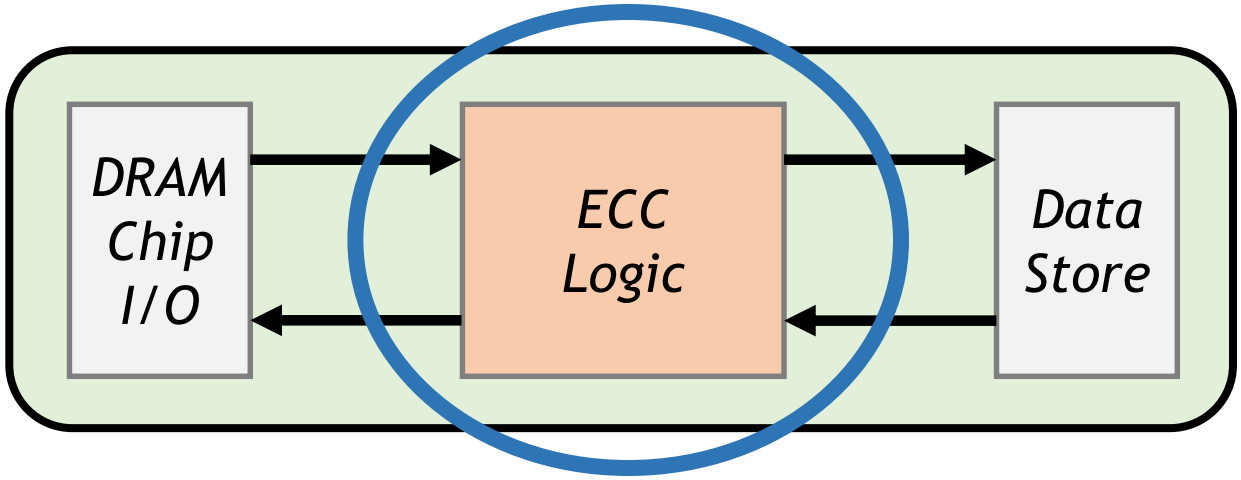
DRAM Testing and Error Characterization



On-die ECC **complicates** reliability studies by **unpredictably obfuscating** raw bit errors

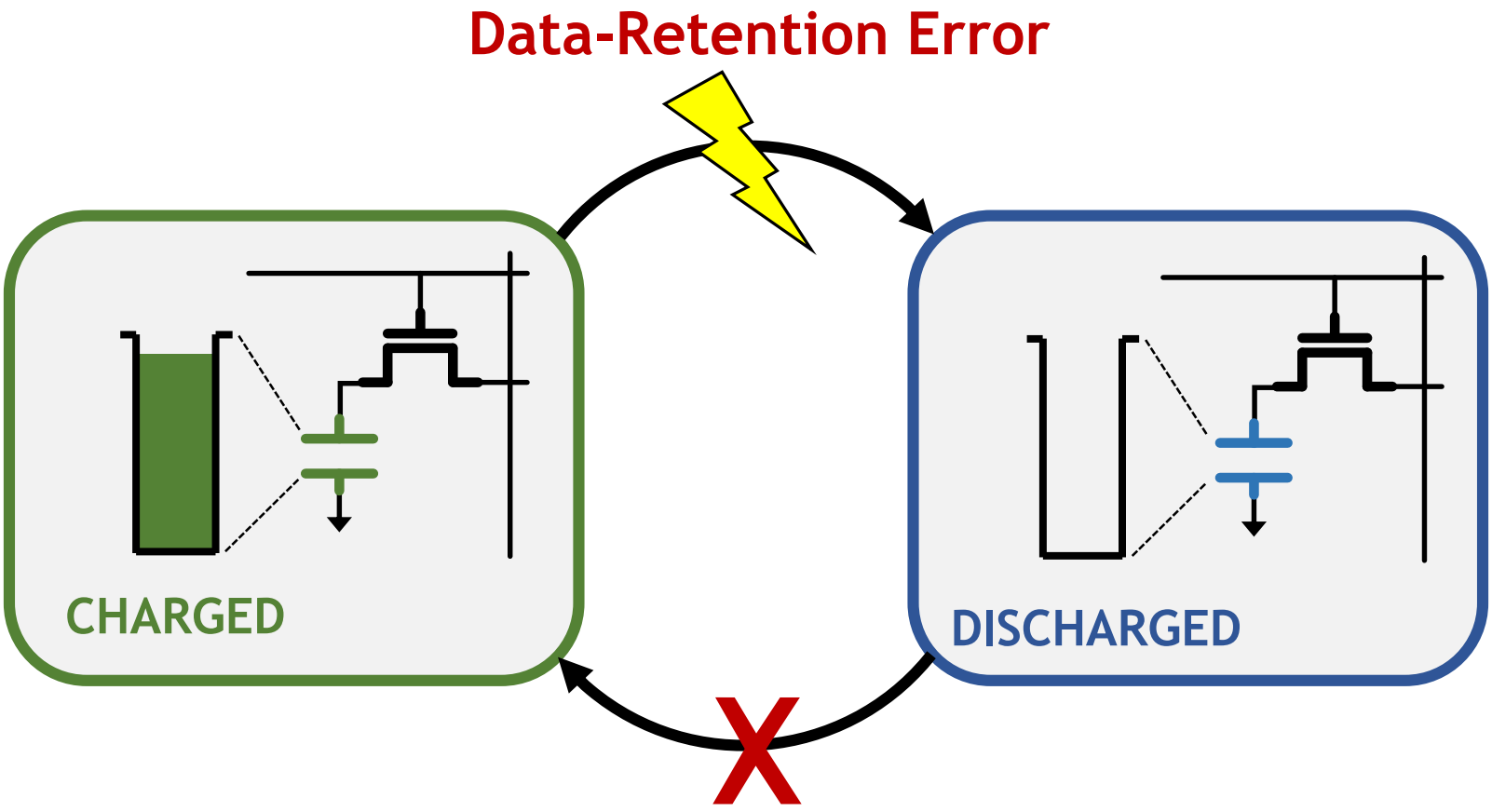
Our goal:

Determine **exactly how** on-die ECC obfuscates errors (i.e., its parity-check matrix)



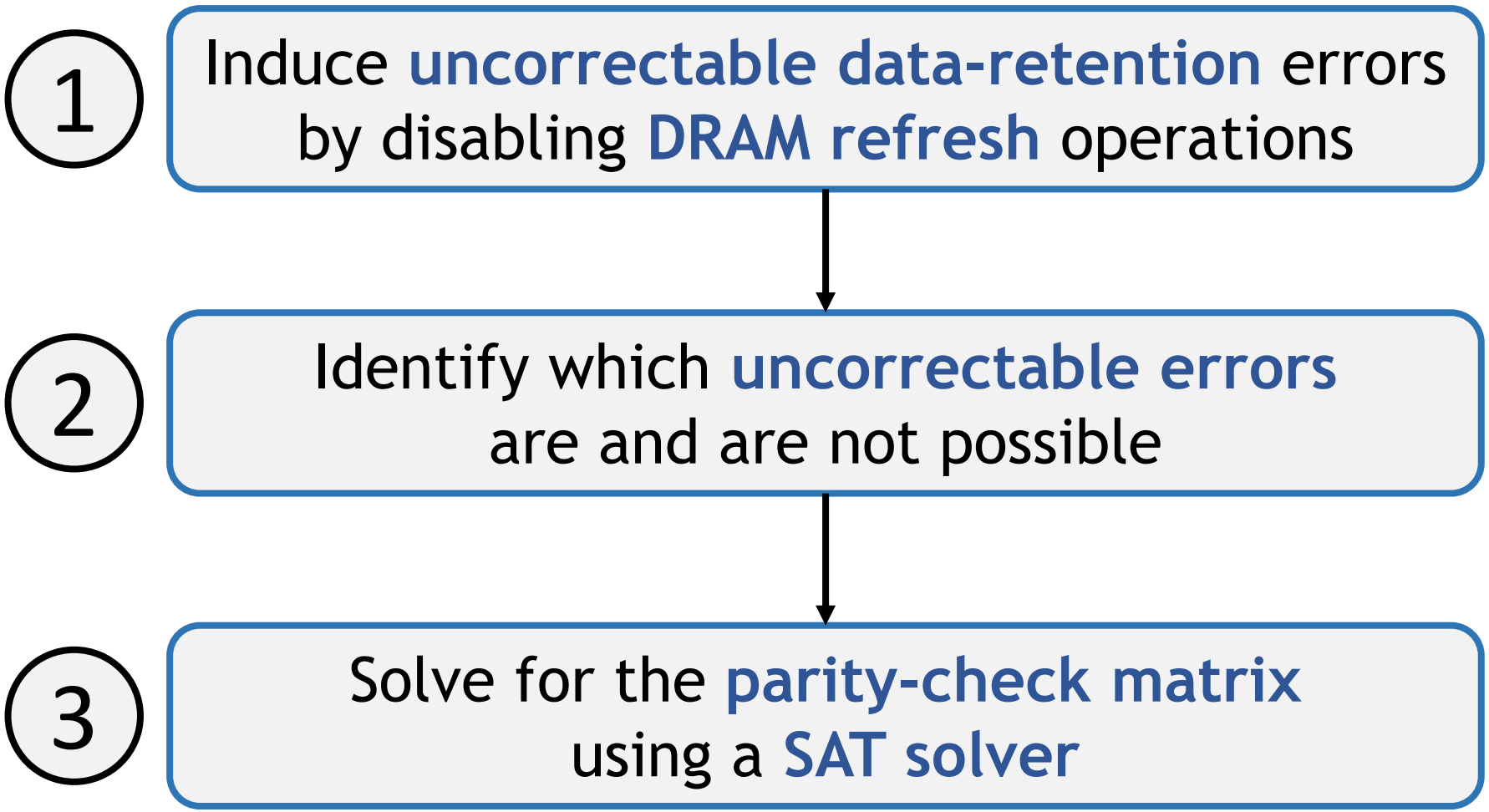
- Reveals **how** on-die ECC scrambles errors (BEER)
- Allows **inferring** raw bit error locations (BEEP)

Key idea: disabling DRAM refresh induces data-retention errors only in CHARGED cells



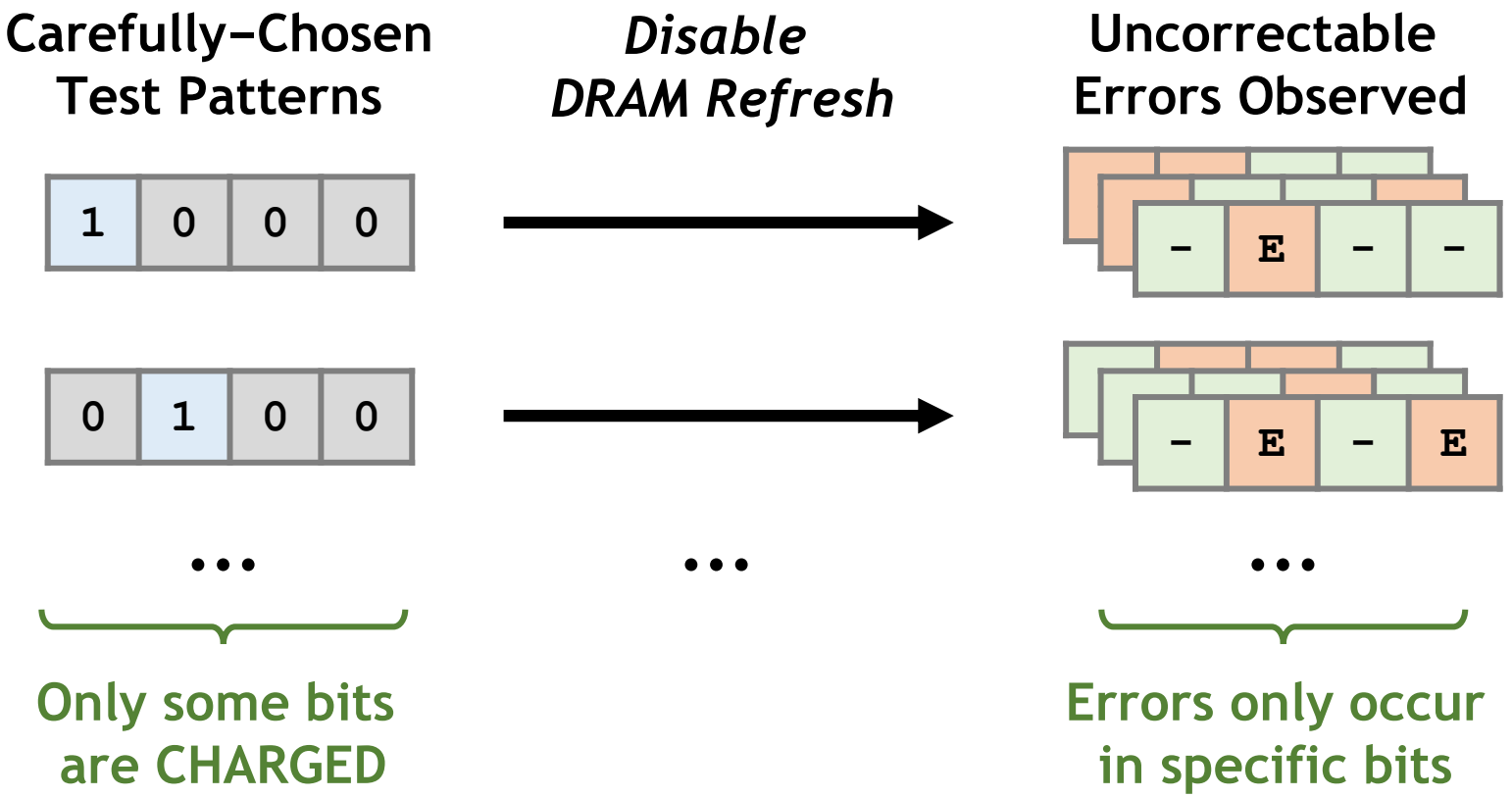
We can **selectively** induce errors by **controlling** bit-flip directions

BEER Testing Methodology



1

Induce **uncorrectable data-retention** errors by disabling **DRAM refresh** operations



2

Identify which **uncorrectable errors** are and are not possible

Test Patterns

1	0	0	0
0	1	0	0
0	0	1	0
0	0	0	1

• • •

Possible Uncorrectable Errors

E	-	E	-
E	E	-	-
-	E	E	E
E	E	-	E

• • •

Different for different ECC Functions

3

Solve for the parity-check matrix using a SAT solver

Observed errors

1	0	0	0	E	-	E	-
0	1	0	0	E	E	-	-
0	0	1	0	-	E	E	E
0	0	0	1	E	E	-	E

Properties of a Hamming code

$$H = \begin{bmatrix} \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \end{bmatrix}$$

SAT Solver

Parity-Check Matrix

$$\begin{bmatrix} \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\ \bullet & \bullet & \bullet & \bullet & \bullet & \bullet \end{bmatrix}$$

BEER Summary

- BEER determines the parity-check matrix **without**:
  (1) hardware support or tools
  (2) prior knowledge about on-die ECC
  (3) access to ECC metadata (e.g., syndromes)

- Open-source C++ tool on GitHub

  https://github.com/CMU-SAFARI/BEER

Experimental demonstration

80 LPDDR4 DRAM chips

(3 major manufacturers)

Two-Part Evaluation

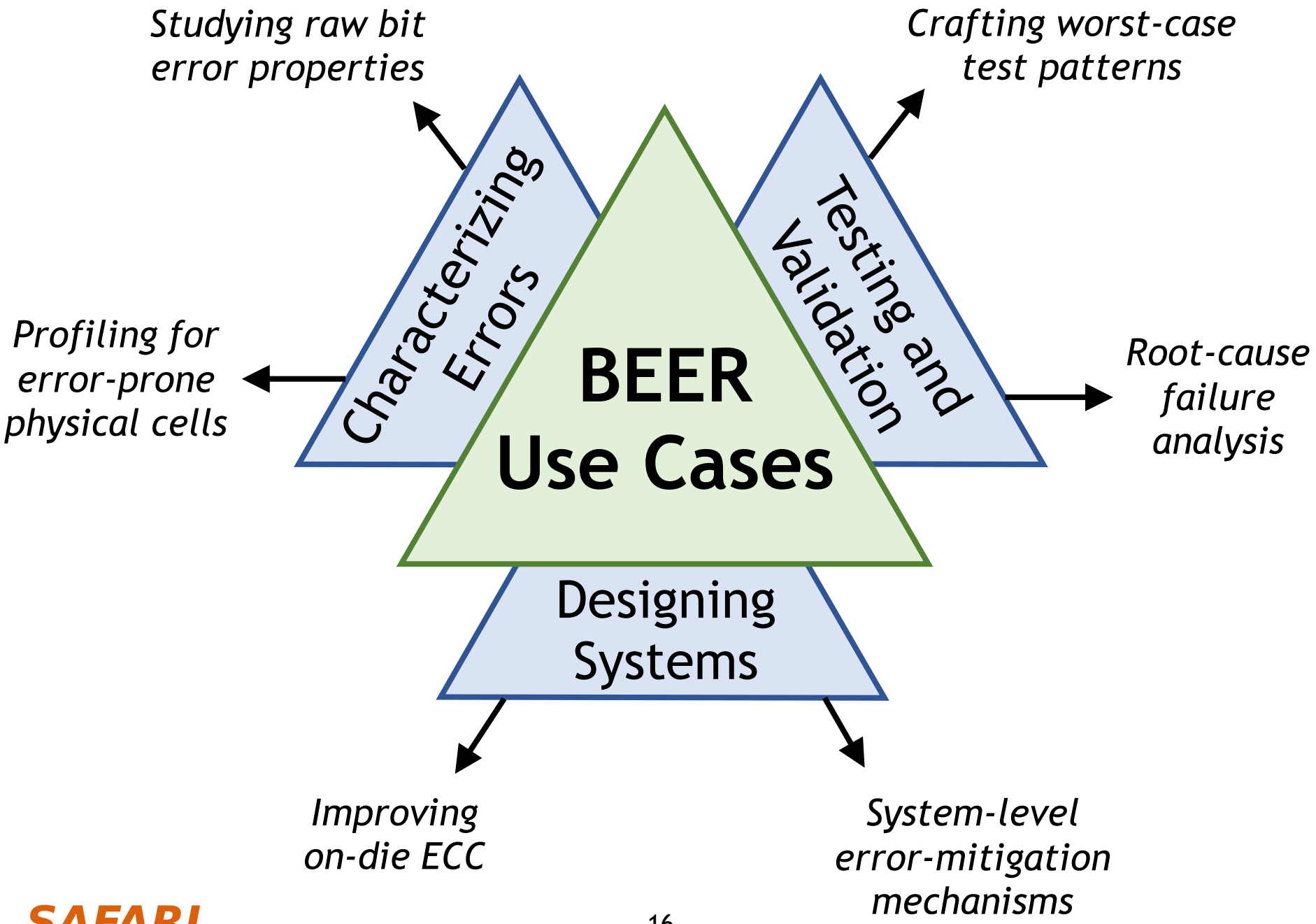
Simulated correctness and practicality

Over 100,000 representative ECC codes of varying word lengths (4 – 247 bits)

1. Different manufacturers appear to use **different** parity-check matrices
2. Chips of the same model appear to use **identical** parity-check matrices

Two-Part Evaluation

1. BEER works for **all** simulated test cases
2. BEER is **practical** in both runtime and memory usage


Studying raw bit error properties
Crafting worst-case test patterns
Characterizing Errors
Testing and Validation
Profiling for error-prone physical cells
BEER Use Cases
Root-cause failure analysis
Designing Systems
Improving on-die ECC
System-level error-mitigation mechanisms

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