DRAM Bender

An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips

Ataberk Olgun
Yahya Can Tugrul
Minesh Patel
Hasan Hassan
Lois Orosa
Oguz Ergin
A. Giray Yaglikci
Haocong Luo
Onur Mutlu

SAFARI
ETH zürich

Factors Affecting DRAM Reliability and Latency

DRAM timing violation | *Inter-cell interference* | *Manufacturing process* | *Temperature* | *Voltage*

Factors affecting DRAM reliability and latency cannot be properly **modeled** in simulation or analytically

We need to perform experimental studies of real DRAM chips

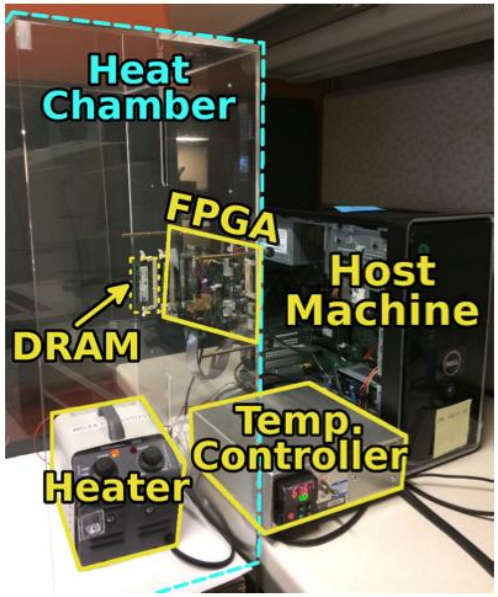
DRAM Testing Infrastructure

Allow experimental studies of real DRAM chips

Open-source FPGA-based testing infrastructure

- Publicly-available: Start using today
- Relatively low cost: An FPGA board + DRAM modules

SoftMC



Litex Tester

Limitations of Existing Infrastructure

Testing Infrastructure	Interface (IF) Restrictions	Ease of Use	Extensibility
SoftMC [134]	Data IF	✗	✗
LiteX RowHammer Tester (LRT) [17]	Command & Data IF	✗	✓
DRAM Bender (this work)	**No Restrictions**	✓	✓

Impose restrictions on the DDR4 interface.
Restrictions limit various characterization experiments.

Difficult to set up (based on discontinued HW/SW)
and use (require developing HW)

Monolithic hardware design
makes extensions (new standards, prototypes) relatively difficult

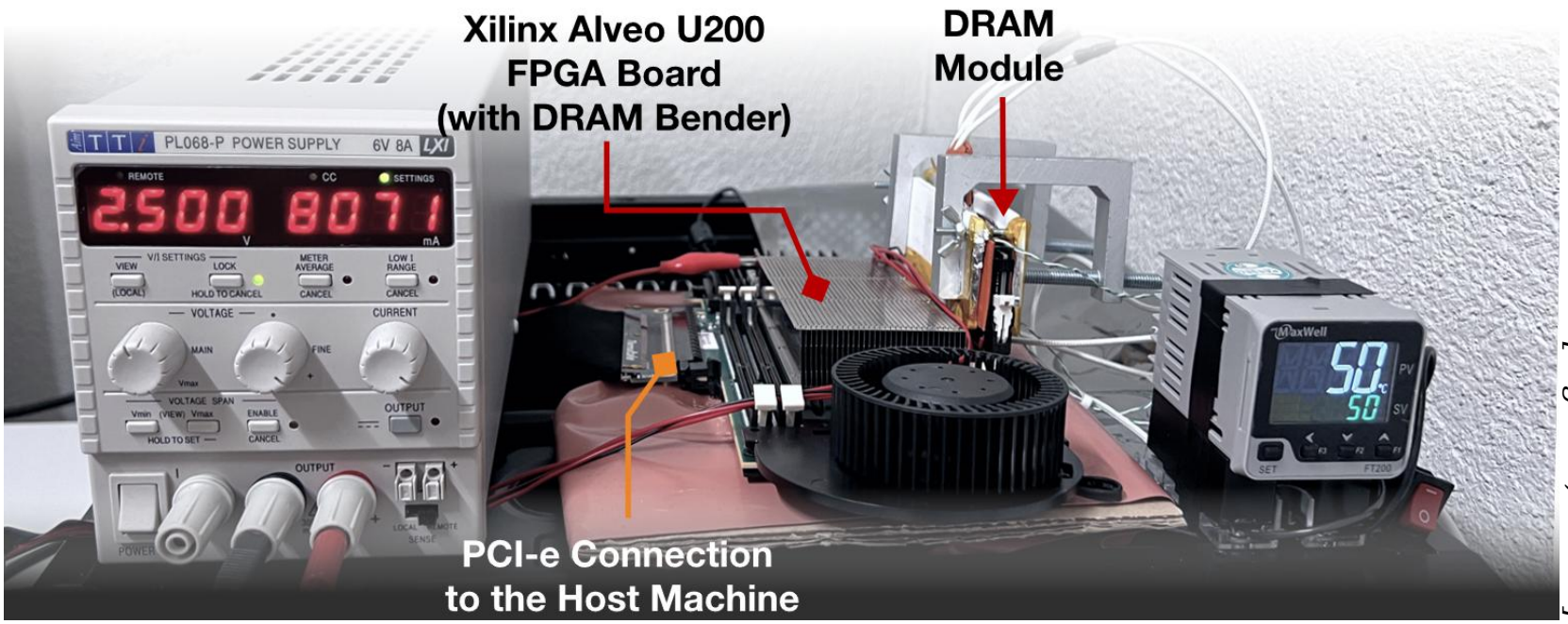
DRAM Bender: Design Goals

- Flexibility
  - Ability to test any DRAM operation
  - Ability to test any combination of DRAM operations and custom timing parameters
- Ease of use
  - Simple programming interface (C++)
  - Minimal programming effort and time
  - Accessible to a wide range of users
    - *who may lack experience in hardware design*
- Extensibility
  - Modular design
  - Well-defined interfaces between hardware modules

DRAM Bender: Overview

Publicly-available FPGA-based
DDR4/3 (and HBM2) characterization infrastructure

Easily programmable using the DRAM Bender C++ API

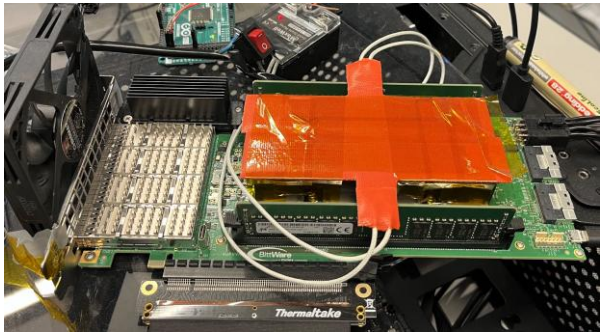


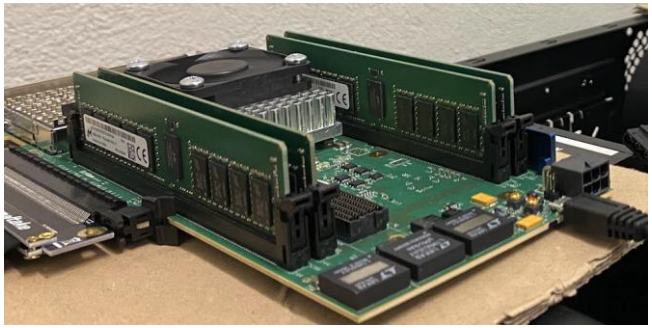
[Yaglikci+, DSN'22]

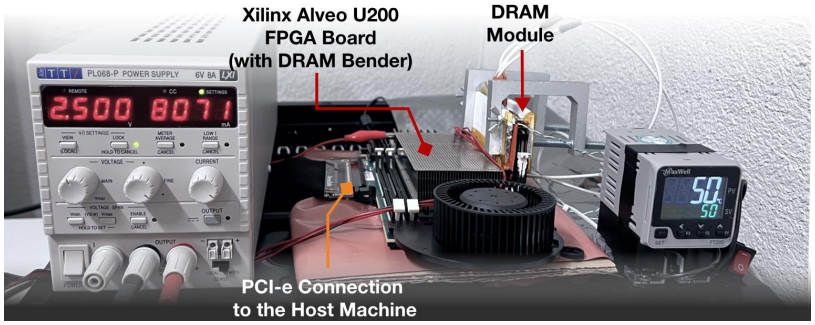
DRAM Bender: Prototypes

Testing Infrastructure	Protocol Support	FPGA Support
SoftMC [134]	DDR3	One Prototype
LiteX RowHammer Tester (LRT) [17]	DDR3/4, LPDDR4	Two Prototypes
DRAM Bender (this work)	**DDR3/DDR4**	**Five Prototypes**

Five out of the box FPGA-based prototypes







DRAM Bender: Three Case Studies

1. RowHammer: Interleaving Pattern of Activations
   - Interleaving pattern significantly affects the number of RowHammer bitflips

2. RowHammer: Random Data Patterns
   - Use 512-bit random data patterns
   - Uncover more bitflips than 8-bit SoftMC random patterns

3. In-DRAM Bitwise Operations
   - Demonstrate in-DRAM bitwise AND/OR capability in real DDR4 chips

DRAM Bender is flexible:
supports many different types of experiments

DRAM Bender: Ease of Use

Easily programmable using the DRAM Bender C++ API

1. RowHammer: Interleaving Pattern of Activations

```
1   p.appendLI(hammerCount, 0);
2   p.appendLabel("HAMMER1");
3   p.appendACT(bank, false, A1, false, tRAS);
4   p.appendPRE(bank, false, false, tRP);
5   p.appendADDI(hammerCount, hammerCount, 1);
6   p.appendBL(hammerCount, T, "HAMMER1");
7   p.appendLI(hammerCount, 0);
8   p.appendLabel("HAMMER2");
9   p.appendACT(bank, false, A2, false, tRAS);
10  p.appendPRE(bank, false, false, tRP);
11  p.appendADDI(hammerCount, hammerCount, 1);
12  p.appendBL(hammerCount, T, "HAMMER2");
```

one iteration of the RowHammer test

Easy to devise new experiments to uncover new insights.

More in the paper (II)

- DRAM Bender design details
  - DRAM Bender instruction set architecture
  - Hardware & software modules
  - Prototype design
  - Temperature controller setup
- DRAM Bender application programming interface
- Detailed results for three case studies
- Future work & improvements

More in the paper (II)

DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips

Ataberk Olgun[§] Hasan Hassan[§] A. Giray Yağlıkçı[§] Yahya Can Tuğrul[§†]
Lois Orosa[§⊙] Haocong Luo[§] Minesh Patel[§] Oğuz Ergin[†] Onur Mutlu[§]
[§]*ETH Zürich* [†]*TOBB ETÜ* [⊙]*Galician Supercomputing Center*

https://arxiv.org/abs/2211.05838

Research DRAM Bender Enabled

1) **[DSN'24]** Olgun+, "Read Disturbance in High Bandwidth Memory: A Detailed Experimental Study on HBM2 DRAM Chips"
2) **[DSN'24]** Yuksel+, "Simultaneous Many-Row Activation in Off-the-Shelf DRAM Chips: Experimental Characterization and Analysis"
3) **[DSN'24 Disrupt]** Luo+, "An Experimental Characterization of Combined RowHammer and RowPress Read Disturbance in Modern DRAM Chips"
4) **[HPCA'24]** Yaglikci+, "Spatial Variation-Aware Read Disturbance Defenses: Experimental Analysis of Real DRAM Chips and Implications on Future Solutions"
5) **[HPCA'24]** Yuksel+, "Functionally-Complete Boolean Logic in Real DRAM Chips: Experimental Characterization and Analysis"
6) **[ISCA'23]** Luo+, "RowPress: Amplifying Read Disturbance in Modern DRAM Chips"
7) **[DSN'23 Disrupt]** Olgun+, "An Experimental Analysis of RowHammer on HBM2 DRAM Chips"
8) **[arXiv Preprint, 2023]** Orosa+, "SpyHammer: Using RowHammer to Remotely Spy on Temperature"
9) **[MICRO'22]** Yaglikci+, "HIRA: Hidden Row Activation for Reducing Refresh Latency of Off-the-Shelf DRAM Chips"
10) **[DSN'22]** Yaglikci+, "Understanding RowHammer Under Reduced Wordline Voltage: An Experimental Study Using Real DRAM Devices"
11) **[MICRO'21]** Orosa+, "A Deeper Look into RowHammer's Sensitivities: Experimental Analysis of Real DRAM Chips and Implications on Future Attacks and Defenses"
12) **[MICRO'21]** Hassan+, "Uncovering In-DRAM RowHammer Protection Mechanisms: A New Methodology, Custom RowHammer Patterns, and Implications"
13) **[ISCA'21]** Olgun+, "QUAC-TRNG: High-Throughput True Random Number Generation Using Quadruple Row Activation in Commodity DRAM Chips"

More Research DRAM Bender Enabled

14) **[ISCA'21]** Orosa+, "CODIC: A Low-Cost Substrate for Enabling Custom In-DRAM Functionalities and Optimizations"

15) **[ISCA'20]** Kim+, "Revisiting RowHammer: An Experimental Analysis of Modern Devices and Mitigation Techniques"

16) **[S&P'20]** Frigo+, "TRRespass: Exploiting the Many Sides of Target Row Refresh"

17) **[HPCA'19]** Kim+, "D-RaNGe: Using Commodity DRAM Devices to Generate True Random Numbers with Low Latency and High Throughput"

18) **[MICRO'19]** Koppula+, "EDEN: Enabling Energy-Efficient, High-Performance Deep Neural Network Inference Using Approximate DRAM"

19) **[SIGMETRICS'18]** Ghose+, "What Your DRAM Power Models Are Not Telling You: Lessons from a Detailed Experimental Study"

20) **[SIGMETRICS'17]** Chang+, "Understanding Reduced-Voltage Operation in Modern DRAM Devices: Experimental Characterization, Analysis, and Mechanisms"

21) **[MICRO'17]** Khan+, "Detecting and Mitigating Data-Dependent DRAM Failures by Exploiting Current Memory Content"

22) **[SIGMETRICS'16]** Chang+, "Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization"

Even More Research DRAM Bender Enabled

23) **[ISCA'24]** Nam+, "DRAMScope: Uncovering DRAM Microarchitecture and Characteristics by Issuing Memory Commands"

24) **[DATE'24]** Zhou+, "DRAM-Locker: A General-Purpose DRAM Protection Mechanism Against Adversarial DNN Weight Attacks"

25) **[DRAMSec'23]** Lang+, "BLASTER: Characterizing the Blast Radius of Rowhammer"

26) **[IEEE CAL'23]** Nam+ "X-ray: Discovering DRAM Internal Structure and Error Characteristics by Issuing Memory Commands"

27) **[MICRO'22]** Gao+, **"**FracDRAM: Fractional Values in Off-the-Shelf DRAM"

28) **[Applied Sciences'22]** Bepary+, "DRAM Retention Behavior with Accelerated Aging in Commercial Chips"

29) **[ETS'21]** Farmani+, "RHAT: Efficient RowHammer-Aware Test for Modern DRAM Modules"

30) **[HOST'20]** Talukder+, "Towards the Avoidance of Counterfeit Memory: Identifying the DRAM Origin"

31) **[MICRO'19]** Gao+, "ComputeDRAM: In-Memory Compute Using Off-the-Shelf DRAMs"

32) **[IEEE Access'19]** Talukder+, "PreLatPUF: Exploiting DRAM Latency Variations for Generating Robust Device Signatures"

33) **[ICCE'18]** Talukder+, "Exploiting DRAM Latency Variations for Generating True Random Numbers"

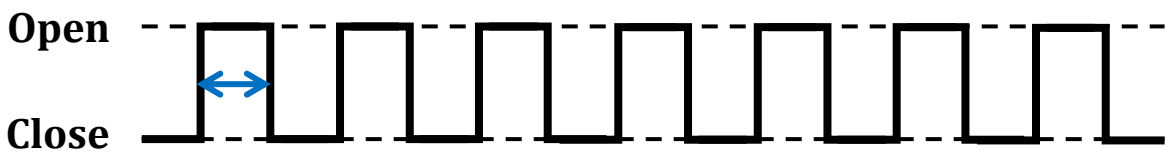
A Highlight: RowPress

Keeping a DRAM row **open for a long time** causes bitflips in adjacent rows

These bitflips do **NOT** require many row activations

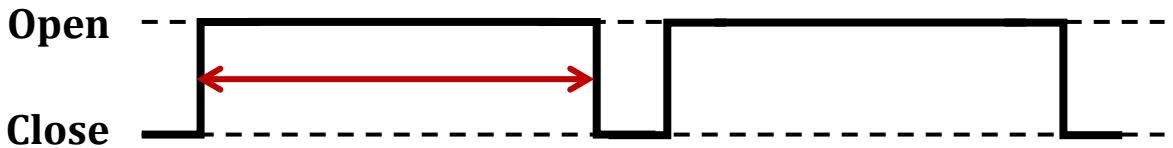
Only one activation is enough in some cases!

RowHammer Aggressor Row



36ns, 47K activations to induce bitflips

RowPress Aggressor Row



7.8µs, only 5K activations to induce bitflips

RowPress Results & Source Code

RowPress: Amplifying Read Disturbance in Modern DRAM Chips

Haocong Luo Ataberk Olgun A. Giray Yağlıkçı Yahya Can Tuğrul Steve Rhyner
Meryem Banu Cavlak Joël Lindegger Mohammad Sadrosadati Onur Mutlu

ETH Zürich

Fully open source and artifact evaluated

- https://github.com/CMU-SAFARI/RowPress

RowPress [ISCA 2023]

- Haocong Luo, Ataberk Olgun, Giray Yaglikci, Yahya Can Tugrul, Steve Rhyner, M. Banu Cavlak, Joel Lindegger, Mohammad Sadrosadati, and Onur Mutlu,
  "RowPress: Amplifying Read Disturbance in Modern DRAM Chips"
  Proceedings of the 50th International Symposium on Computer Architecture ***(ISCA)***, Orlando, FL, USA, June 2023.
  [Slides (pptx) (pdf)]
  [Lightning Talk Slides (pptx) (pdf)]
  [Lightning Talk Video (3 minutes)]
  [RowPress Source Code and Datasets (Officially Artifact Evaluated with All Badges)]
  Officially artifact evaluated as available, reusable and reproducible.
  Best artifact award at ISCA 2023.

RowPress: Amplifying Read-Disturbance in Modern DRAM Chips

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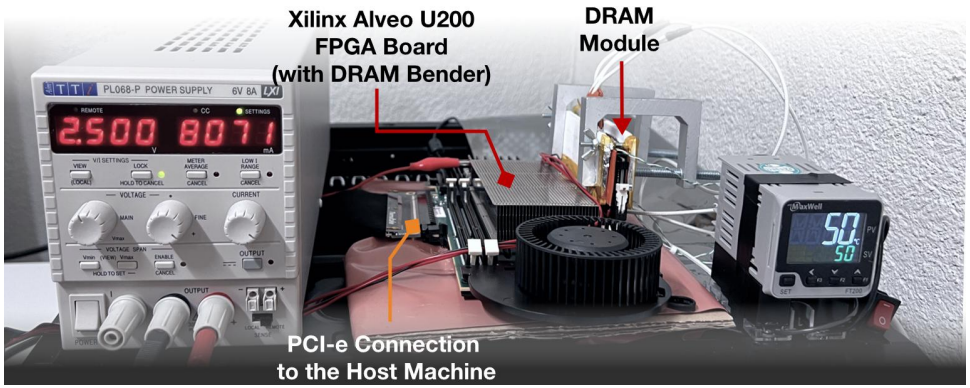
Summary

DRAM Bender

The first **publicly-available** DDR4 characterization infrastructure

- Flexible and Easy to Use
- **Source code** available:



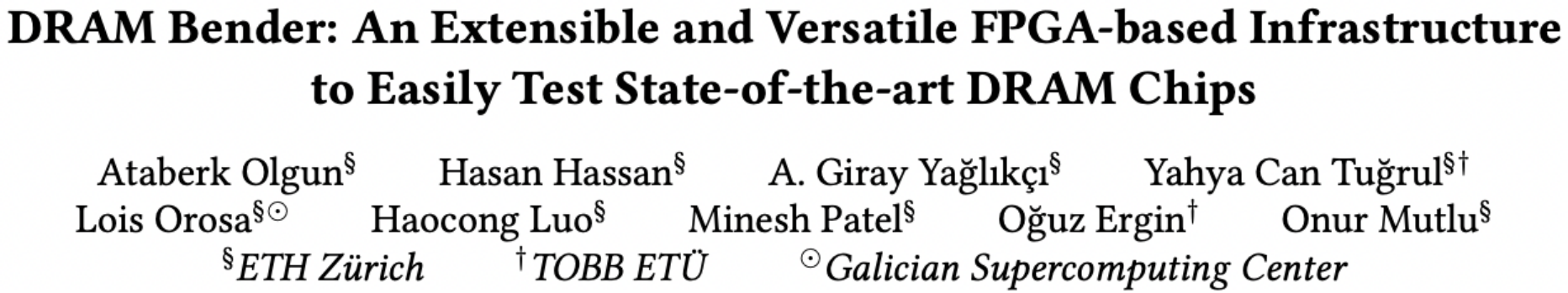
[Yaglikci+, DSN'22]

github.com/CMU-SAFARI/DRAMBender

DRAM Bender enables many studies, ideas,
and methodologies in the design of future memory systems

DRAM Bender Paper, Slides, Videos, Code

- Ataberk Olgun, Hasan Hassan, A Giray Yağlıkçı, Yahya Can Tuğrul, Lois Orosa, Haocong Luo, Minesh Patel, Oğuz Ergin, and Onur Mutlu,
  "DRAM Bender: An Extensible and Versatile FPGA-based Infrastructure to Easily Test State-of-the-art DRAM Chips"
  IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (***TCAD***), 2023.
  [Extended arXiv version]
  [DRAM Bender Source Code]
  [DRAM Bender Tutorial Video (43 minutes)]



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