Ramulator 2.0: A Modern, Modular, and Extensible DRAM Simulator

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Abstract—We present Ramulator 2.0, a highly modular and extensible DRAM simulator that enables rapid and agile implementation and evaluation of design changes in the memory controller and DRAM to meet the increasing research effort in improving the performance, security, and reliability of memory systems. Ramulator 2.0 abstracts and models key components in a DRAM-based memory system and their interactions into shared *interfaces* and independent *implementations*. Doing so enables easy modification and extension of the modeled functions of the memory controller and DRAM in Ramulator 2.0. The DRAM specification syntax of Ramulator 2.0 is concise and human-readable, facilitating easy modifications and extensions. Ramulator 2.0 implements a library of reusable templated lambda functions to model the functionalities of DRAM commands to simplify the implementation of new DRAM standards, including DDR5, LPDDR5, HBM3, and GDDR6. We showcase Ramulator 2.0's modularity and extensibility by implementing and evaluating a wide variety of RowHammer mitigation techniques that require *different* memory controller design changes. These techniques are added modularly as separate implementations *without* changing *any* code in the baseline memory controller implementation. Ramulator 2.0 is rigorously validated and maintains a fast simulation speed compared to existing cycle-accurate DRAM simulators. Ramulator 2.0 is open-sourced under the permissive MIT license at https://github.com/CMU-SAFARI/ramulator2.

1 INTRODUCTION

Cycle-accurate DRAM simulators enable modeling and evaluation of detailed operations in the memory controller and the DRAM device. In recent years, growing research and design efforts in improving the performance, security, and reliability of DRAM-based memory systems require a cycle-accurate simulator that facilitates rapid and agile implementation and evaluation of intrusive design changes (i.e., modification of functionalities of the simulated system as opposed to simple parameter changes) in the memory controller and DRAM. Unfortunately, existing cycle-accurate DRAM simulators are not modular and extensible *enough* to meet such a requirement.

We identify two key issues in the design and implementation of existing cycle-accurate DRAM simulators. First, they do *not* model key components of a DRAM-based memory system in a *fundamentally modular* way, making it difficult to implement and maintain different intrusive design changes. For example, USIMM [1] does not separate the DRAM specification from the memory controller. Similarly, the templated implementations of the DRAM specifications in Ramulator [2] (referred to as Ramulator 1.0 in this paper) cause undesired coupling between the DRAM specification and the memory controller.

Second, existing simulators do *not* implement DRAM specifications in a concise and intuitive way, making it difficult to add new DRAM commands and define new timing constraints. For example, both DRAMsim2 [3] and DRAMsim3 [4] implement a single DRAM device model that aggregates all the DRAM specifications from all supported DRAM standards in a single C++ class. Ramulator 1.0's DRAM specifications are based on low-level and verbose C++ syntax (e.g., it uses eight full lines of C++ code just to specify solely a single `tCCD_L` timing constraint in DDR4 [5]).

To address these issues, we present Ramulator 2.0 [6], a successor to Ramulator 1.0 [2] that provides an easy-to-use, modular, and extensible software infrastructure for rapid and agile implementation and evaluation of DRAM-related research and design ideas. Ramulator 2.0 has two distinguishing features. First, it implements a modular and extensible code framework by identifying and modeling the key components in a DRAM-based memory system into separate *interfaces* and *implementations*. With this framework, different design changes (e.g., different address mapping schemes, request scheduling policies, new DRAM standards, RowHammer mitigations) can be implemented as *independent* implementations that share the *same* interface, enabling easy modification and extension of Ramulator 2.0.

Second, to facilitate easy modification of DRAM specifications (e.g., DRAM organization, commands, timing constraints), Ramulator 2.0 implements concise and human-readable definitions of DRAM specifications on top of the lookup table based hierarchical DRAM device model in Ramulator 1.0. Ramulator 2.0's DRAM specifications 1) are defined with simple string literals, 2) leverage permutations of different DRAM commands to concisely define timing constraints, and 3) use a library of templated lambda functions that are *reusable* across different DRAM standards to define the functionalities of DRAM commands (e.g., the same RFM command implementation can be (and is) used by DDR5 [7], LPDDR5 [8], and GDDR6 [9], HBM3 [10]). These improvements are implemented with the new features of C++20 [11] (e.g., constant-evaluated immediate functions), enabling significant duplicate-code reduction and easy modification and extension of the modeled DRAM device's functionalities *without* sacrificing simulation speed.

We showcase the modularity and extensibility of Ramulator 2.0 by implementing and evaluating a variety of RowHammer mitigation techniques (PARA [12], TWiCe [13], Graphene [14], Hydra [15], Randomized Row-Swap (RRS) [16], and an ideal refresh-based mitigation [17]) that require *different* additional functionalities in the memory controller. These RowHammer mitigations plug themselves into the *same* baseline memory controller implementation *without* changing the memory controller's code, which was not possible in Ramulator 1.0 [2] and is not possible in any other DRAM simulator we are aware of [1, 3, 4].

The key features and contributions of Ramulator 2.0 are:

- Ramulator 2.0 is a modular and extensible DRAM simulator written in C++20 that enables rapid and agile implementation and evaluation of design changes in the memory system. Ramulator 2.0 can either work as a standalone simulator, or be used as a memory system library by a system simulator (e.g., gem5 [18], zsim [19]).
- We showcase the modularity and extensibility of Ramulator 2.0 by implementing and evaluating six different RowHammer mitigation techniques as plugins to a single unmodified memory controller implementation.
- Ramulator 2.0 implements a wide range of new DRAM standards, including DDR5 [7], LPDDR5 [8], HBM3 [10], and GDDR6 [9] (as well as old ones, e.g., DDR3 [20], DDR4 [5], HBM(2) [21]).
- Ramulator 2.0 is rigorously validated and maintains a fast simulation speed compared to existing cycle-accurate DRAM simulators.
- We open-source Ramulator 2.0 [6] under the permissive MIT license to facilitate and encourage open research and

agile implementation of new ideas in memory systems. We also integrate it with gem5 [18].

2 Ramulator 2.0 Design Features

We walk through the two key design features of Ramulator 2.0 that enable rapid and agile implementation of design changes in the memory system. Section 2.1 introduces the high-level software architecture of Ramulator 2.0 based on the key concepts of *interface(s)* and *implementation(s)*. Section 2.1.1 provides a deeper look into the modularity and extensibility enabled by Ramulator 2.0 by showcasing how different RowHammer mitigations can all be implemented as *plugins* of the same baseline unmodified memory controller implementation. Section 2.2 introduces the concise and human-readable DRAM specification syntax of Ramulator 2.0 that facilitates easy modification and extension of the functionality of the DRAM device.

2.1 Modular and Extensible Software Architecture

Ramulator 2.0 models all components in a DRAM-based memory system with two fundamental concepts, *Interface* and *Implementation*, to achieve high modularity and extensibility. An interface is an abstract C++ class defined in a `.h` header file that models the common high-level functionality of a component as seen by other components in the system. An implementation is a concrete C++ class defined in a `.cpp` file that inherits from an interface, modeling the actual behavior of a component. Components interact with each other through pointers to each other's interfaces stored in the implementations. With such a design, the functionality of a component can be easily changed by instantiating a different implementation for the same interface, involving *no* changes in the code of unrelated components.

Figure 1 shows the high-level software architecture of Ramulator 2.0 with the key interfaces we identify in a DRAM-based memory system (dark boxes) and their typical implementations (light boxes) when modeling a DDR5 system with RowHammer mitigation. The arrows illustrate the relationships among different components in the simulated system (i.e., how they call each other's interface functions). We highlight the memory request path with red arrows, DRAM command path with blue arrows, and DRAM maintenance requests (e.g., refreshes) with green arrows. A typical execution of the simulation is as follows: First, memory requests are sent ❶ from the frontend (either parsed from traces or generated by another simulator, e.g., gem5 [18]) to the memory system, where the memory addresses are mapped ❷ to the DRAM organization through the address mapper. Then, the requests are enqueued ❸ in the request buffers of the DRAM controller. The DRAM controller is responsible for 1) ticking the refresh manager ❹, which could enqueue high-priority maintenance requests (e.g., refreshes) back to the controller, 2) querying the request scheduler ❺, which in turn consults the DRAM device model ❻ to decode the best DRAM command to issue ❼ to serve a memory request, and 3) issuing the DRAM command ❽, which updates the behavior and timing information of the DRAM device model. Finally, the memory controller executes the finished request's callback ❾ to notify the frontend of the completion of the memory request.

Users can easily extend Ramulator 2.0 without intrusive changes to existing code by creating different implementations of each existing interface in three easy steps: 1) create a new `.cpp` file, 2) create the new implementation class that inherits from both the implementation base class and the existing interface class, and 3) implement the new functionality in the new implementation class. Similarly, a new interface can be added simply adding a `.h` file containing the abstract interface class definitions. All interfaces and implementations in Ramulator 2.0 *register themselves* to a class registry that bookkeeps the relationship among different interfaces and implementations. Using this registry, Ramulator 2.0 automatically recognizes and instantiates different implementations for each interface from a human-readable configuration file. Users do *not* need to manually maintain any boilerplate code to describe the relationships between interfaces and implementations.

2.1.1 Memory Controller Plugins

We make a key observation that many modeled functions in the memory controller (e.g., controller-based RowHammer mitigations that tracks the issued activation commands) and utilities needed for evaluation (e.g., collecting statistics from the issued DRAM commands and analyzing the memory access patterns) are triggered (updated) by the currently-scheduled DRAM command. To avoid having many similar memory controller implementations for every single such modeled function and utility, we model these functions as plugins to the memory controller. As an example, Figure 2 shows in detail how various RowHammer mitigation techniques (e.g., PARA [12], Graphene [14], Hydra [15], TRR [22, 23], RFM [7]) can be implemented as such memory controller plugins.

The plugin interface has a simple `update(DRAM_CMD, ADDR)` function that the controller calls (① in Figure 1 and 2) to notify the plugin implementations about the DRAM command and address issued by the memory controller. The RowHammer mitigation implementation then updates its internal state (e.g., generates a random number for PARA, updates the row activation count table (bank

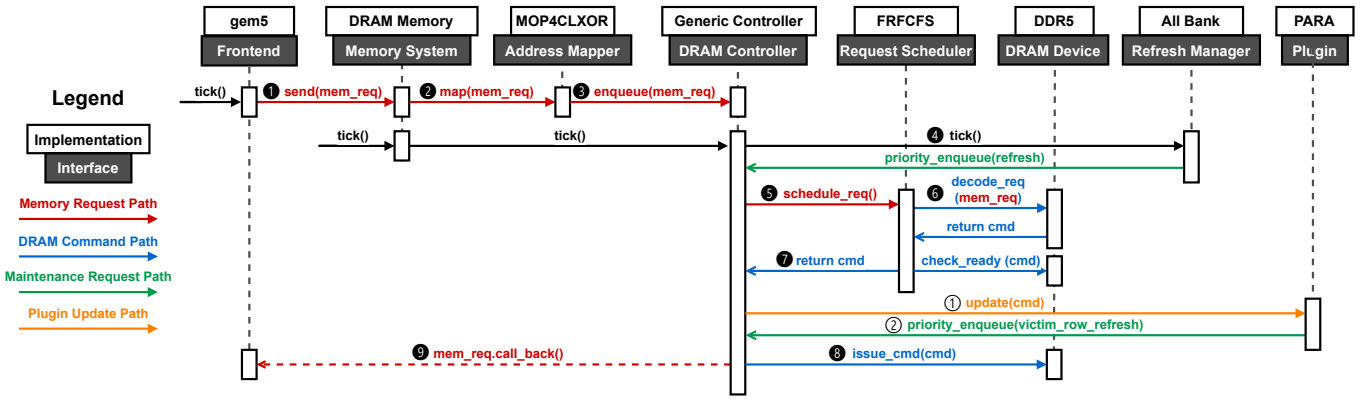

Fig. 1: High-level software architecture of Ramulator 2.0 using an example DDR5 system configuration

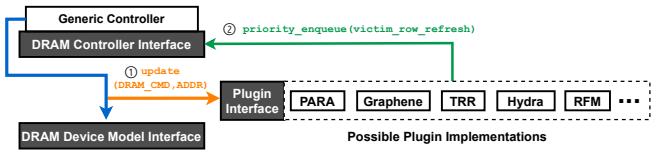

Fig. 2: Implementing RowHammer mitigation techniques as controller plugins. Legend is in Figure 1.

activation counter) for Graphene and TRR (RFM), or queries the row count cache for Hydra). If the implementation detects the need to refresh the potential RowHammer victim rows, it calls the `priority_enqueue()` function (② in Figure 1 and 2) of the memory controller interface to send a high-priority refresh request for the identified victim rows, ready to be scheduled in the following cycles, as determined by the mitigation techniques. To showcase the modularity and extensibility of memory controller plugins, Section 3.3 provides a cross-sectional evaluation of the performance overhead of six different RowHammer mitigation techniques, all implemented as memory controller plugins.

2.2 Concise and Intuitive DRAM Specifications

Ramulator 2.0 facilitates easy modification and extension of DRAM specifications (e.g., the organization of the DRAM device hierarchy, DRAM commands, timing constraints, mapping between DRAM commands and organization levels) in two major ways. First, Ramulator 2.0 allows the user to directly define the DRAM specifications *by their names* with human-readable string literals, as Listing 1 shows.

Listing 1: Example Definition of DRAM Organization and Commands

```
1  // Different levels in the organizaton hierarchy
2  inline static constexpr ImplDef m_levels = {
3    "channel", "rank", "bankgroup",
4    "bank", "row", "column",
5  };
6  // Different DRAM commands
7  inline static constexpr ImplDef m_commands = {
8    "ACT", "PRE", "PREab", "RD",  "WR", "REF"
9  };
10 // Mapping between commands and levels
11 inline static const ImplLUT m_cmd_scopes = LUT (
12   m_commands, m_levels, {
13     {"ACT", "row"}, {"PRE", "bank"},
14     {"RD",  "column"}, {"WR", "column"},
15     {"REF", "rank"}, {"PREab","rank"},
16   }
17 );
```

Internally, Ramulator 2.0 *automatically* encodes these string literals into integers. These integers are used to *efficiently* index the the lookup table-based finite state machines that Ramulator 2.0 uses to model the hierarchical organization and behavior of DRAM devices, similarly to Ramulator 1.0 [2]. This encoding is done statically at *compile-time* within the frequently queried and updated DRAM device model so that it does *not* incur any run-time performance overhead (e.g., the expression `m_levels["bank"]` is a `consteval` expression that is evaluated to the integer "3" by the compiler). Other components in the simulated system that need to know the DRAM device's specifications (e.g., the organization of the DRAM device hierarchy, DRAM commands, timing constraints, the mapping between DRAM commands and organization levels) can query the DRAM specification with string literals during initialization to get the underlying integer encoding (or an error indicating the component is incompatible with the DRAM specification). Doing so *completely* decouples the DRAM specifications from other parts of the simulated system, thereby achieving higher modularity and extensibility than Ramulator 1.0.

Based on these string-literal based definitions, Ramulator 2.0 develops a concise and human-readable way to model the timing constraints of DRAM commands. The key idea is to define timing constraints based on the permutation of the preceding and following DRAM commands. Doing so reduces redundant code by merging the timing constraint definitions that have the same numerical value but are between different pairs of preceding and following DRAM commands into a single definition. For example, Listing 2 shows the definition of the timing constraint `nRCD` that specifies the minimum delay between a preceding `ACT` command and either a following `RD` or `WR` command at the `bank` level. With this modeling, Ramulator 2.0 defines the key DDR4 timing constraints with only 32 lines of code, a 61% reduction from Ramulator 1.0's 82 lines. Such code deduplication enables the addition of new DRAM standards in an easier and less error-prone way.

Listing 2: Example Definition of Timing Constraints

```
1  {.level = "bank",
2   .preceding = {"ACT"}, .following = {"RD", "WR"},
3   .latency = V("nRCD")},
```

Second, Ramulator 2.0 implements the DRAM commands (e.g., the state changes caused by the DRAM commands and the prerequisite commands based on the current state) using a library of lambda functions. These functions are implemented in a templated way so that they are defined only once, but can be *reused* many times for similar DRAM commands across *different* standards. As an example, Listing 3 shows a part of implementations of the `RFMab` command (all-bank refresh management, which exists in the DDR5 [7], LPDDR5 [8], GDDR6 [9], and HBM3 [10] standards) that requires all the banks to be closed before it can be issued.

Listing 3: Example Implementation of a DRAM Command, *RFMab* (shared across different DRAM standards, including DDR5, LPDDR5, GDDR6, HBM3)

```
1  template <class DRAM_t>
2  int RequireAllBanksClosed(typename DRAM_t::Node* node,
       int cmd, int target_id, Clk_t clk) {
3    // for all banks {
4    // ...
5      if (bank->m_state == DRAM_t::m_states["Closed"]) {
6        continue;
7      } else {
8        return T::m_commands["PREab"];
9      }
10   // }
11   return cmd;
12 };
13
14 // In DDR5.cpp
15 m_preqs[m_levels["rank"]][m_commands["RFMab"]] =
       RequireAllBanksClosed<DDR5>;
16 // In LPDDR5.cpp
17 m_preqs[m_levels["rank"]][m_commands["RFMab"]] =
       RequireAllBanksClosed<LPDDR5>;
18 // In GDDR6.cpp
19 m_preqs[m_levels["channel"]][m_commands["RFMab"]] =
       RequireAllBanksClosed<GDDR6>;
20 // In HBM3.cpp
21 m_preqs[m_levels["channel"]][m_commands["RFMab"]] =
       RequireAllBanksClosed<HBM3>;
```

Ramulator 2.0 defines a `RequireAllBanksClosed` generic function that checks for all banks in the organization hierarchy if all of them are closed (lines 6-7). If so, it simply returns the input command argument `cmd` (line 12), indicating that no prerequisite command is needed for `cmd`. Otherwise, it returns the `PREab` (precharge all-bank) command to close all the banks first. This function is templated on the DRAM standard implementation (i.e., the `DRAM_t` template parameter on line 2) so that it can automatically get the correct integer encoding of the commands and states for different DRAM standards at compile-time. By reusing this templated function in different DRAM standards (lines 16, 18, 20, and 22), implementing the prerequisite checks for the `RFMab` command needs only a single line of code in each standard (instead of duplicating the entire `RequireAllBanksClosed` function for each DRAM standard as in Ramulator 1.0).

3 Validation & Evaluation

3.1 Validating the Correctness of Ramulator 2.0

To make sure Ramulator 2.0's memory controller and DRAM device model implementation is correct (i.e., the DRAM commands issued by the controller obey both the timing constraints and the state transition rules), we verify the DRAM command trace against Micron's DDR4 Verilog Model [24] using a similar methodology to prior works [2–4]. To do so, we implement a DRAM command trace recorder as a DRAM controller plugin that can store the issued DRAM commands with the addresses and time stamps using the DDR4 Verilog Model's format. We collect DRAM command traces from eight streaming-access and eight random-access synthetic memory traces and different intensities (i.e., the number of non-memory instructions between memory instructions). We feed the DRAM command trace to the Verilog Model, configured to use the same DRAM organization and timings as we use in Ramulator 2.0. We find no timing or state transition violations.

3.2 Performance of Ramulator 2.0

We compare the simulation speed of Ramulator 2.0 with three other cycle-accurate DRAM simulators: Ramulator 1.0 [2], DRAMsim2 [3], DRAMsim3 [4], and USIMM [1]. All four simulators are compiled with `gcc-12 -O3`, and configured with comparable system parameters. We generate two memory traces, one with a random access pattern and another with a streaming access pattern, each containing five million memory requests (read-write ratio = 4:1). For each simulator and trace, we run the simulation for each trace ten times on a machine with an Intel Xeon Gold 5118 processor. Table 1 shows the minimum, average, and maximum simulation runtimes across the ten runs. We conclude that, despite the increased modularity and extensibility, Ramulator 2.0 achieves a comparably fast (and even faster) simulation speed versus other existing cycle-accurate DRAM simulators. We provide the scripts, configurations, and traces to reproduce our results in Ramulator 2.0's repository [6].

Simulator (gcc-12 -O3)	Runtime (sec) min./avg./max.		Avg. Requests/sec	
	Random	Stream	Random	Stream
Ramulator 2.0	**50.3/50.6/51.4**	**26.1/26.2/26.4**	**98.8K**	**190.8K**
Ramulator 1.0	58.2/59.0/62.3	31.7/31.9/33.0	84.7K	156.7K
DRAMsim3	51.4/51.7/52.3	37.5/37.8/38.6	96.7K	132.3K
DRAMsim2	51.6/51.9/52.4	53.7/53.9/54.1	96.3K	92.8K
USIMM	402.9/407.0/410.0	31.2/31.3/31.4	12.3K	159.7K

TABLE 1: Simulation Performance Comparison

3.3 Cross-Sectional Study of RowHammer Mitigations

To demonstrate the modularity and extensibility of Ramulator 2.0, we implement six different RowHammer mitigation techniques, PARA [12], an idealized version of TWiCe [13], Graphene [14], Hydra [15], Randomized Row-Swap (RRS) [16], and an ideal refresh-based mitigation (Ideal) [17]. All of these mechanisms are implemented in the form of memory controller plugins as described in Section 2.1.1. Figure 3 shows the performance overhead (weighted speedup normalized to a baseline configuration running the same workloads *without* any RowHammer mitigation, y-axis) of different RowHammer mitigations as the RowHammer threshold (i.e., the minimum number of DRAM row activations to cause at least one bitflip, t_{RH}, x-axis) decreases from 5000 to 10. We use traces generated from SPEC2006 [25] and SPEC2017 [26] to form 25 four-core multiprogrammed workloads that we feed through a simplistic out-of-order core model (the complete set of scripts and traces to reproduce these experiments are in [6]).

We make the following two observations. First, all evaluated RowHammer mitigations (except for Ideal) cause significant performance overhead compared to the ideal mitigation as t_{RH} decreases to very low values. Second, for $t_{RH} < 50$, the performance overhead of RRS becomes too high for the simulation to make progress. This is because the activation caused by a row swap triggers even more row swaps, preventing DRAM from serving memory access requests. We conclude that existing RowHammer mitigation techniques are not scalable enough to low t_{RH} values (<50). As such, more research effort is needed to develop more efficient and scalable RowHammer mitigation techniques.

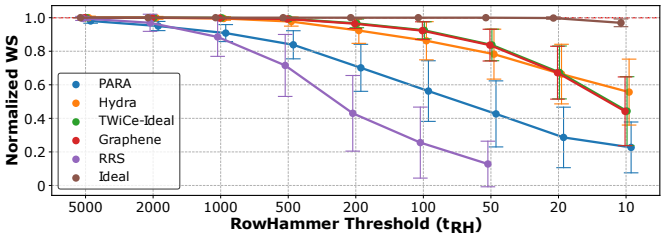

Fig. 3: Performance overhead of RowHammer mitigation techniques vs. different RowHammer thresholds

4 Conclusion

We present Ramulator 2.0, a modern, modular, and extensible DRAM simulator as a successor to Ramulator 1.0. We introduce the key design features of Ramulator 2.0 and demonstrate its high modularity, extensibility, and performance. We hope that Ramulator 2.0's modular and extensible software architecture and concise and intuitive modeling of DRAM facilitates more agile memory systems research.

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