Revisiting RowHammer

An Experimental Analysis of Modern Devices and Mitigation Techniques

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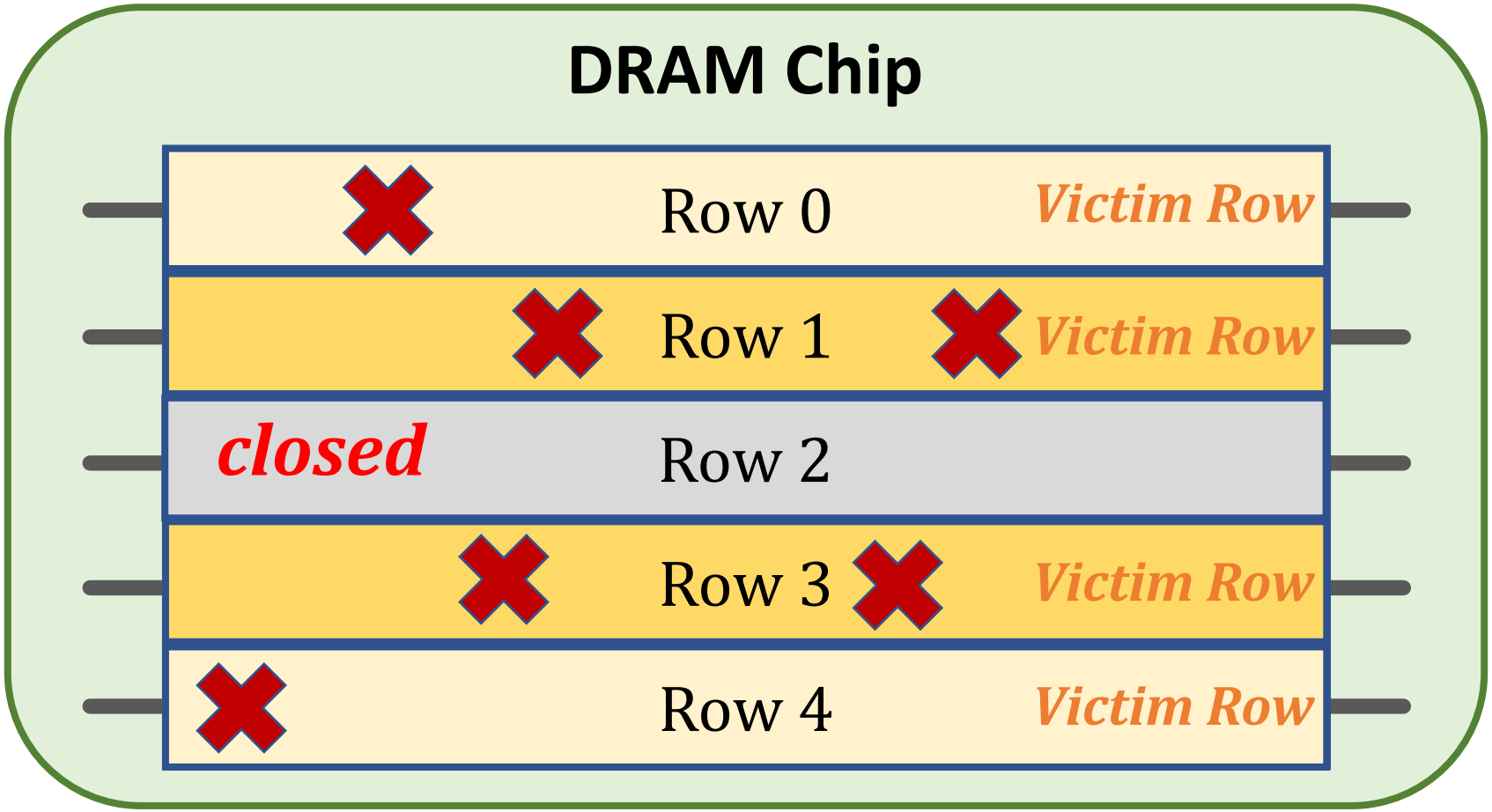
The RowHammer Vulnerability



Repeatedly **opening** (activating) and **closing** (precharging) a DRAM row causes **RowHammer bit flips** in nearby cells

Motivation and Goal

- Denser DRAM chips are **more vulnerable** to RowHammer
- Three prior works **[Kim+, ISCA'14], [Park+, MR'16], [Park+, MR'16]**, **over the last six years** provide RowHammer characterization data on real DRAM
- However, there is **no comprehensive experimental study** that demonstrates **how vulnerability scales** across DRAM types and technology node generations
- **Unclear whether current mitigation mechanisms will remain viable** for future DRAM chips that are likely to be more vulnerable to RowHammer

Goal:

1. **Experimentally demonstrate** how vulnerable modern DRAM chips are to RowHammer and study how this vulnerability will scale going forward
2. Study viability of existing **mitigation mechanisms** on more vulnerable chips

Experimental Characterization

We examine 1580 total DRAM chips from 300 DRAM modules

- **Three** major DRAM manufacturers {A, B, C}
- **Three** DRAM *types* or *standards* {DDR3, DDR4, LPDDR4}
- **Two** technology nodes per DRAM type {old/new, 1x/1y}

Key Takeaways

1. Chips of newer DRAM technology nodes are **more vulnerable** to RowHammer
2. There are chips today whose weakest cells fail after **only 4800 hammers** (i.e., 4800 accesses to two rows each)
3. Chips of newer DRAM technology nodes can exhibit RowHammer bit flips 1) in **more rows** and 2) **farther away** from the victim row.

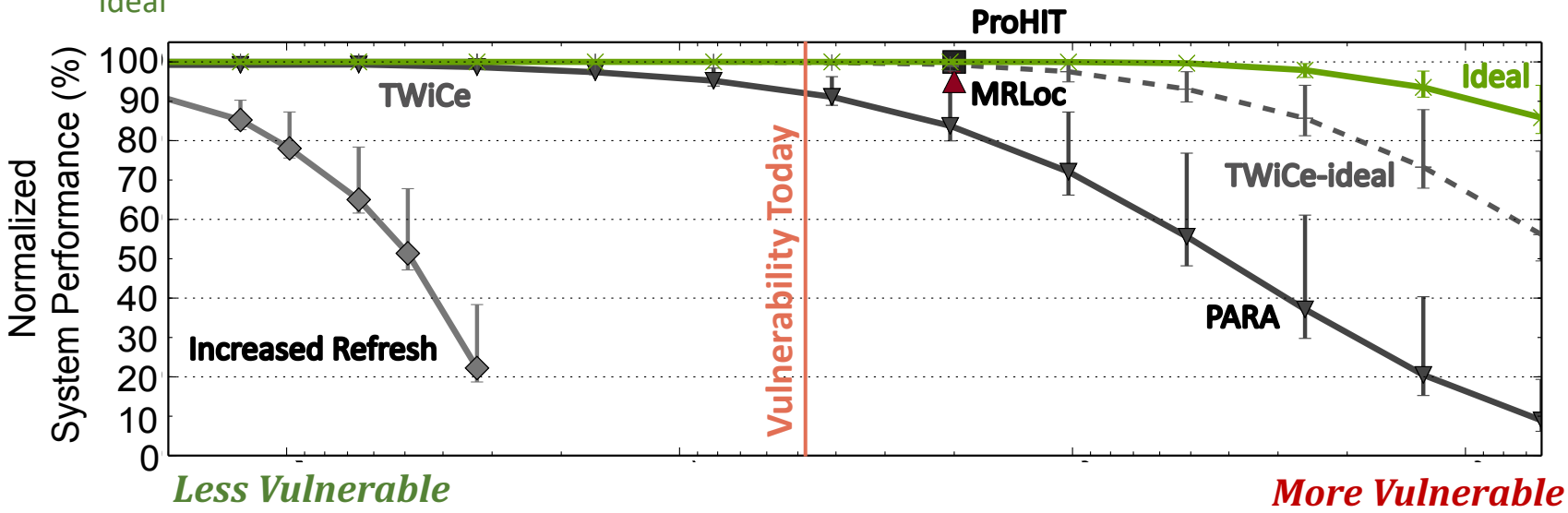
Mitigation Mechanism Evaluation

We evaluate system performance impact on chips of varying degrees of vulnerability for **five** state-of-the-art mitigation mechanisms:

Increased Refresh Rate [Kim+, ISCA'14], PARA [Kim+, ISCA'14], ProHIT [Son+, DAC'17], MRLoc [You+, DAC'19], TWiCe [Lee+, ISCA'19]

one ideal refresh-based mitigation mechanism:

Ideal



DRAM's Vulnerability to RowHammer

Available mechanisms mitigate RowHammer in worst chips today with reasonable system performance (92%, 100%, 100%)

We need better solutions for future chips that are likely more vulnerable

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