Understanding RowHammer Under Reduced Wordline Voltage

An Experimental Study Using Real DRAM Devices

Session 14 (June 30, 10:30 AM)
Hardware and Software Security

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Executive Summary

Motivation:

- Repeatedly **toggling a DRAM row's wordline voltage** causes bit flips in nearby rows
- This vulnerability, **RowHammer**, **worsens in denser DRAM chips**
- Understanding RowHammer enables designing **effective and efficient solutions**

Problem: No study demonstrates how **wordline voltage (V_{PP})** affects RowHammer

Goal: Experimentally understand how **V_{PP} affects RowHammer and DRAM operation**

Experimental study: 272 DRAM chips from **three major manufacturers**

VPP's effect on RowHammer: *Six observations* show that with reduced V_{PP},

- A row needs to be hammered **7.4% more times (85.8% max)** to induce a bit flip
- **Bit error rate** caused by a RowHammer attack reduces by **15.2% (66.9% max)**

VPP's effect on DRAM operation: *Nine observations* show that with reduced V_{PP},

- **208 out of 272** tested DRAM chips **reliably operate** using nominal timing parameters
- Erroneous DRAM chips can reliably operate with
  - **A longer row activation latency,** i.e., 24ns/15ns for 48/16 chips,
  - **Single-error-correcting codes or 2x the refresh rate** *only for* 16.4% of rows

Conclusion: Scaling down the wordline voltage can **reduce RowHammer vulnerability** *without* significantly affecting reliable DRAM operation

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