Towards Efficient Sparse Matrix Vector Multiplication on Real Processing-In-Memory Systems

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Abstract

Sparse Matrix Vector Multiplication (SpMV) has been characterized as one of the most thoroughly studied scientific computation kernels, because it is a fundamental linear algebra kernel for important applications from the scientific computing, machine learning, and graph analytics domains. SpMV performs indirect memory references as a result of storing the sparse matrix in a compressed format, and irregular memory accesses to the input vector due to the sparsity pattern of the input matrix [6, 13, 27]. Therefore, in commodity processor-centric systems, SpMV is a primarily memory-bandwidth-bound kernel for the majority of real sparse matrices, and is bottlenecked by data movement between memory and processors [6, 9, 10].

One promising way to alleviate the data movement bottleneck is the Processing-In-Memory (PIM) paradigm [1, 2, 7–10, 14, 15, 17]. PIM moves computation close to application data by equipping memory chips with processing capabilities [1, 14, 15]. To provide large aggregate memory bandwidth for the in-memory processors, several manufacturers have already started to commercialize *near-bank* PIM designs [1, 9, 10, 19, 20]. *Near-bank* PIM designs tightly couple a PIM core with each DRAM bank, exploiting bank-level parallelism to expose high on-chip memory bandwidth of standard DRAM to processors. Three *real* near-bank PIM architectures are Samsung's FIMDRAM [19], SK hynix's GDDR6-AiM [20] and the UPMEM PIM system [1, 9, 10].

Most real near-bank PIM architectures [1, 9, 10, 19, 20] support several PIM-enabled memory chips connected to a host CPU via memory channels. Each memory chip comprises multiple low-power PIM cores with relatively low computation capability [9, 10], and each of them is located close to a DRAM bank [9, 10, 19, 20]. Each PIM core can access data located on its local DRAM bank, and typically there is no direct communication channel among PIM cores. Overall, near-bank PIM systems provide high levels of parallelism and very large memory bandwidth. As such, they are a very promising computing platform to accelerate memory-bound kernels. Recent works leverage near-bank PIM architectures to provide high performance and energy benefits on bioinformatics [5, 9, 10], skyline computation [22], compression [11] and neural network [9, 10, 16, 19] kernels. A recent study [9, 10] provides PrIM benchmarks [25], which are a collection of 16 kernels for evaluating near-bank PIM architectures. However, there is *no* prior work to thoroughly study the widely used, memory-bound SpMV kernel on a real PIM system.

Our work is the first to efficiently map the SpMV kernel on near-bank PIM systems, and understand its performance implications on a real-world PIM system. We make two key contributions. First, we design efficient SpMV algorithms to accelerate the SpMV kernel in current and future PIM systems, while covering a wide variety of sparse matrices with diverse sparsity patterns. Second, we provide the first comprehensive analysis of SpMV on a real PIM architecture. Specifically, we conduct our rigorous experimental analysis of SpMV kernels in the UPMEM PIM system, the first publicly-available real-world PIM architecture.

We present the freely and openly available *SparseP* library [26] that includes 25 SpMV kernels for real PIM systems. *SparseP* supports (1) the most popular compressed matrix formats (i.e., CSR, COO, BCSR, BCOO formats), (2) a wide range of data types (i.e., 8-bit integer, 16-bit integer, 32-bit integer, 64-bit integer, 32-bit float and 64-bit float data types), (3) two types of well-crafted data partitioning techniques of the sparse matrix to PIM-enabled memory, (4) various load balancing schemes across PIM cores, (5) various load balancing schemes across threads of a multithreaded PIM core, and (6) three synchronization approaches among threads within multithreaded PIM core.

We conduct an extensive characterization and analysis of *SparseP* kernels on the UPMEM PIM system [9, 10]. We analyze the SpMV execution (1) using one single multithreaded PIM core, (2) using thousands of PIM cores, and (3) comparing its performance and energy consumption with that achieved on conventional processor-centric CPU and GPU systems. Our extensive evaluation provides programming recommendations for software designers, and suggestions and hints for hardware and system designers of future PIM systems.

We highlight our most significant recommendations for PIM software designers:

(1) *Design algorithms that provide high load balance across threads of a multithreaded PIM core in terms of computations, loop control iterations, synchronization points and memory accesses.* In SpMV, we find that when the parallelization scheme used causes *high* disparity in the non-zero elements/blocks/rows processed across threads of a PIM core, or the number of lock acquisitions/lock releases/DRAM memory accesses performed across threads, performance severely degrades in low-area PIM cores with relatively low computation capabilities [9, 10].

(2) *Design compressed data structures that can be effectively partitioned across DRAM banks, with the goal of providing high computation balance across PIM cores.* We observe that the compressed matrix format used to store the input matrix in SpMV determines the data partitioning across DRAM banks of PIM-enabled memory, thereby affecting the load balance across PIM cores with corresponding performance implications.

(3) *Design adaptive algorithms that trade off computation balance across PIM cores for lower data transfer costs to PIM-enabled memory, and adapt the software strategies to the particular patterns of each input given, as well as the characteristics of the PIM hardware.* Our analysis demonstrates that the best-performing

SpMV execution on the UPMEM PIM system is achieved using algorithms that (i) trade off computation for lower data transfer costs, and (ii) select the load balancing strategy and data partitioning policy based on the particular sparsity pattern of the input matrix and the characteristics of the underlying PIM hardware.

We highlight our most significant suggestions for PIM hardware and system designers:

(1) *Provide low-cost synchronization support and hardware support to enable concurrent memory accesses by multiple threads to the local DRAM bank to increase parallelism in a multithreaded PIM core.* For instance, fine-grained locking approaches in SpMV to increase parallelism in critical sections do not improve performance over coarse-grained approaches. This is because concurrent DRAM accesses performed by multiple threads are serialized by the UPMEM PIM hardware. To improve parallelism, subarray level parallelism [23] or multiple DRAM banks per PIM core could be supported in the PIM hardware, along with lightweight synchronization schemes for PIM cores [2].

(2) *Optimize the broadcast collective operation in data transfers from main memory to PIM-enabled memory to minimize overheads of copying the input data into all DRAM banks in the PIM system.* When the sparse matrix is horizontally partitioned across PIM cores and the whole input vector is copied into the DRAM bank of *each* PIM core, SpMV cannot scale up to a large number of PIM cores. This is because it is severely limited by data transfer costs to broadcast the input vector into each DRAM bank of PIM-enabled DIMMs. Such data transfers incur high overheads, because they take place via the narrow off-chip memory bus.

(3) *Optimize the gather collective operation at DRAM bank granularity for data transfers from PIM-enabled memory to the host CPU to minimize overheads of retrieving the output results.* When the sparse matrix is split in 2D tiles, each of them is assigned to each PIM core, SpMV is severely limited by data transfers to retrieve results for the output vector from DRAM banks of PIM-enabled memory. This is due to two reasons: (i) PIM cores create a large number of partial results that need to be gathered from PIM-enabled memory to the host CPU via the narrow memory bus in order to assemble the final output vector, and (ii) the current implementation of the UPMEM PIM system has the limitation that the transfer sizes from/to all DRAM banks involved in the same parallel transfer need to be the same, and therefore a large amount of padding with empty bytes is performed in such SpMV kernels.

(4) *Design high-speed communication channels and optimized libraries for data transfers to/from thousands of DRAM banks of PIM-enabled memory.* We find that SpMV execution on the memory-centric UPMEM PIM system achieves a much higher fraction of the machine's peak performance (on average 51.7% for the 32-bit float data type), compared to that on processor-centric CPU and GPU systems. However, its end-to-end performance is still significantly limited by data transfer overheads on the narrow memory bus. Thus, the software stack of real PIM systems needs to be enhanced with fast data transfers to/from PIM-enabled memory modules, and/or the PIM hardware needs to be enhanced to support efficient direct communication among PIM cores [12, 18, 21, 24].

For more information about our thorough characterization on the SpMV PIM execution, results, insights and the open-source *SparseP* software package [26], we refer the reader to the full version of the paper [3, 4]. We hope that our work can provide valuable insights to programmers in the development of efficient sparse linear algebra kernels and other irregular kernels from different application domains tailored for real PIM systems, and enlighten architects and system designers in the development of future memory-centric computing systems. The *SparseP* software package is publicly and freely available at https://github.com/CMU-SAFARI/SparseP.

Keywords

high-performance computing, sparse matrix-vector multiplication, SpMV library, multicore, processing-in-memory, near-data processing, memory systems, data movement bottleneck, DRAM, benchmarking, real-system characterization, workload characterization

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