What Your DRAM Power Models Are Not Telling You: Lessons from a Detailed Experimental Study

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ABSTRACT

Main memory (DRAM) consumes as much as half of the total system power in a computer today, due to the increasing demand for memory capacity and bandwidth. There is a growing need to understand and analyze DRAM power consumption, which can be used to research new DRAM architectures and systems that consume less power. A major obstacle against such research is the lack of detailed and accurate information on the power consumption behavior of modern DRAM devices. Researchers have long relied on DRAM power models that are predominantly based off of a set of standardized current measurements provided by DRAM vendors, called IDD values. Unfortunately, we find that state-of-the-art DRAM power models are often highly inaccurate when compared with the real power consumed by DRAM. This is because existing DRAM power models (1) are based off of the *worst-case* power consumption of devices, as vendor specifications list the current consumed by the most power-hungry device sold; (2) do *not* capture variations in DRAM power consumption due to different *data value* patterns; and (3) do *not* account for any *variation* across different devices or within a device.

To build an *accurate* model and provide insights into DRAM power consumption, we perform the first comprehensive experimental characterization of the power consumed by modern real-world DRAM modules. We build a custom FPGA-based infrastructure that allows us to execute precise test procedures that characterize variation and data dependency in the power consumed by DRAM. Our extensive characterization of 50 DDR3L DRAM modules from three major vendors (A, B, and C) yields four key new observations about DRAM power consumption that prior models cannot capture:

(1) Across all IDD values that we measure, the current consumed by real DRAM modules varies significantly from the current specified by the vendors. For example, to read one cache line of data from DRAM, the measured current of modules from Vendor A is lower than the current specified in the datasheet by an average of 54.1% (up to 61.6%).
(2) DRAM power consumption strongly depends on the data value that is read or written. Reading a cache line where all bits are *ones* uses an average of 39.2% (up to 91.6%) more power than reading a cache line where all bits are *zeroes*.
(3) There is significant *structural variation*, where the current varies based on which bank or row is selected in a DRAM module. For example, in modules from Vendor C, the idle current consumed when one of the eight banks is active (i.e., open) can vary by an average of 15.4% (up to 23.6%) depending on the bank.
(4) Across successive process technology generations, the actual power savings of DRAM is *much lower* than the savings indicated by vendor specifications in datasheets. Across five key IDD values, the measured savings of modules from Vendor A are lower than indicated by an average of 48.0% (up to 66.7%).

Because state-of-the-art DRAM power models do *not* account for any of these four key characteristics, they are highly inaccurate, and have a mean error ranging between 17.4% and 58.3% compared to the actual, measured power consumption of 50 real DDR3L modules.

Based on our detailed analysis and characterization data, we develop the *Variation-Aware model of Memory Power Informed by Real Experiments* (VAMPIRE). VAMPIRE is a new, accurate power consumption model for DRAM that takes into account (1) module-to-module and intra-module variations, and (2) power consumption variation due to data value dependency. VAMPIRE enables a wide range of studies that were *not* possible using prior DRAM power models. As an example, we use VAMPIRE to evaluate the energy efficiency of three different encodings that can be used to store data in DRAM. We find that a new power-aware data encoding mechanism can reduce total DRAM energy consumption by an average of 12.2%, across a wide range of applications.

For more information on our extensive experimental characterization and on VAMPIRE, please refer to the full version of our paper [1]. We plan to open-source both VAMPIRE and our extensive raw data collected during our experimental characterization [2]. We hope that the findings in this work and our new power model will inspire new research directions, new ideas, and rigorous evaluations in power- and energy-aware DRAM design.

KEYWORDS

DRAM; memory systems; energy; power consumption; power modeling; experimental characterization; data encoding; low-power design

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