Fairness via Source Throttling:

A configurable and high-performance fairness substrate for multi-core memory systems

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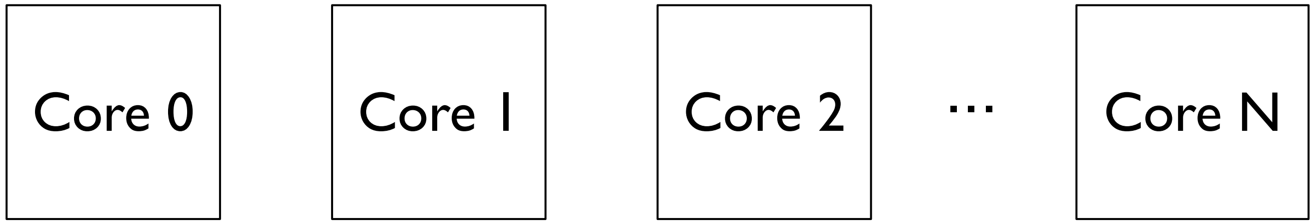
Background and Problem



Core 0

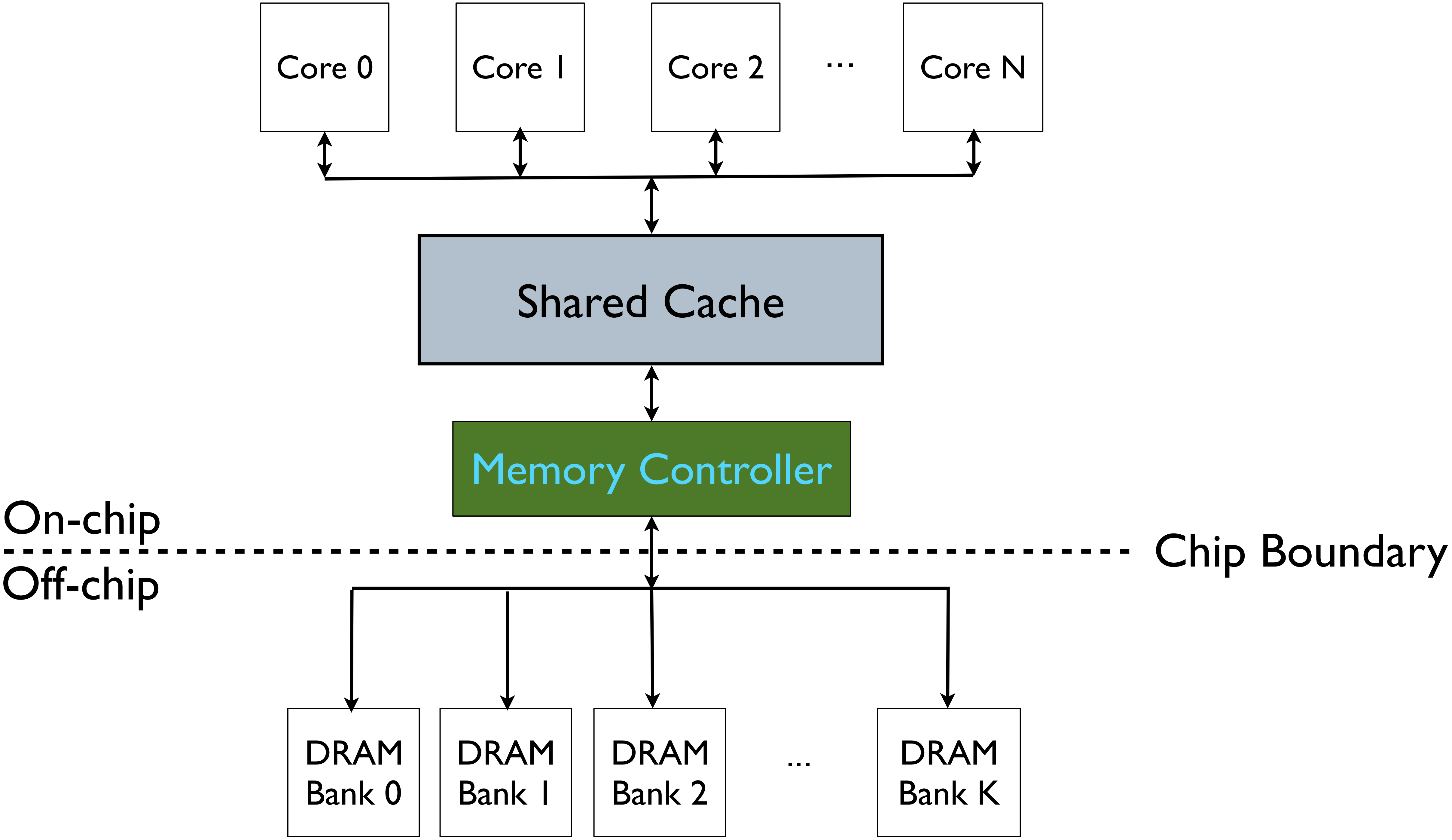
Core 1

Core 2

…

Core N

Background and Problem



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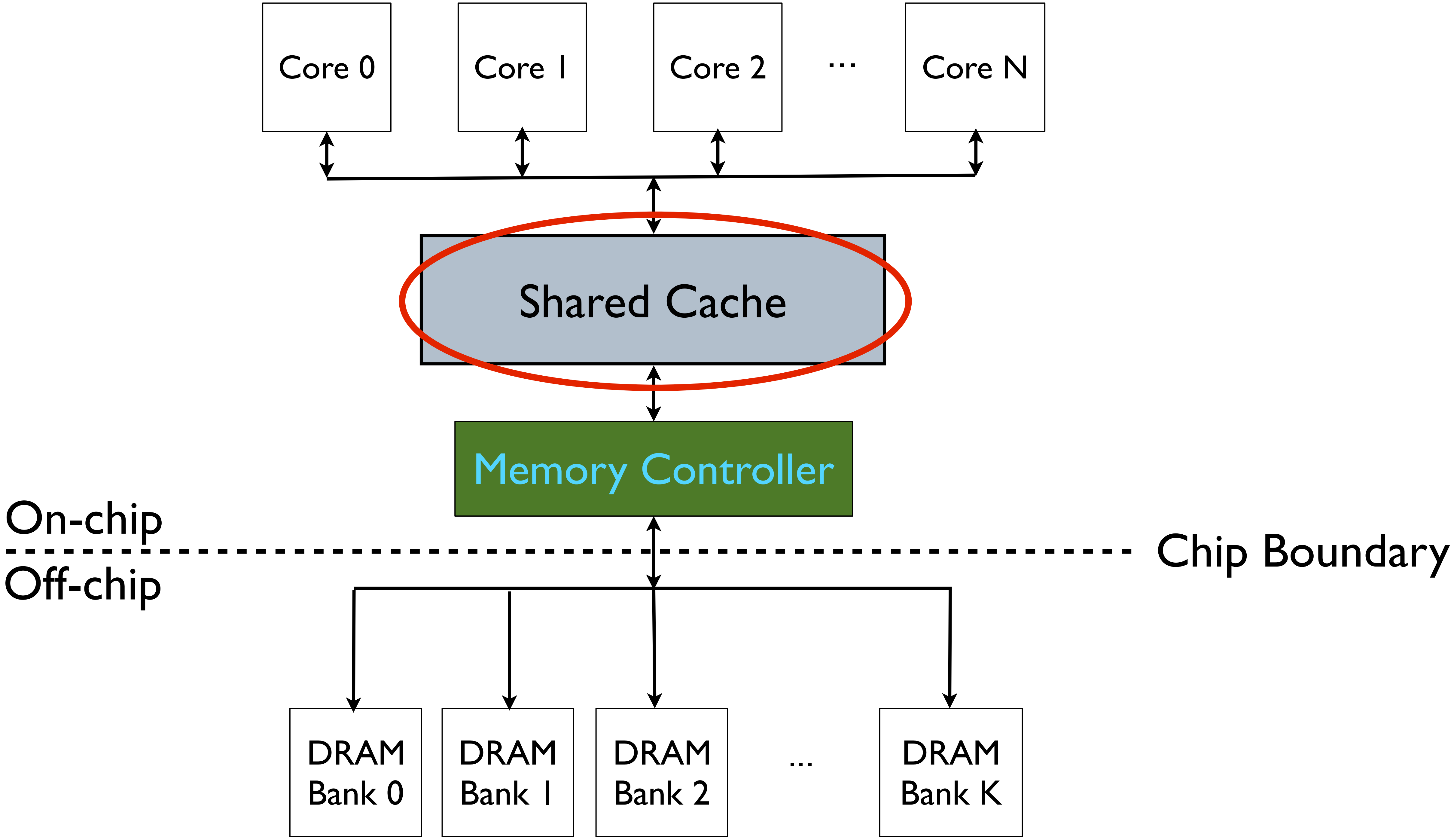

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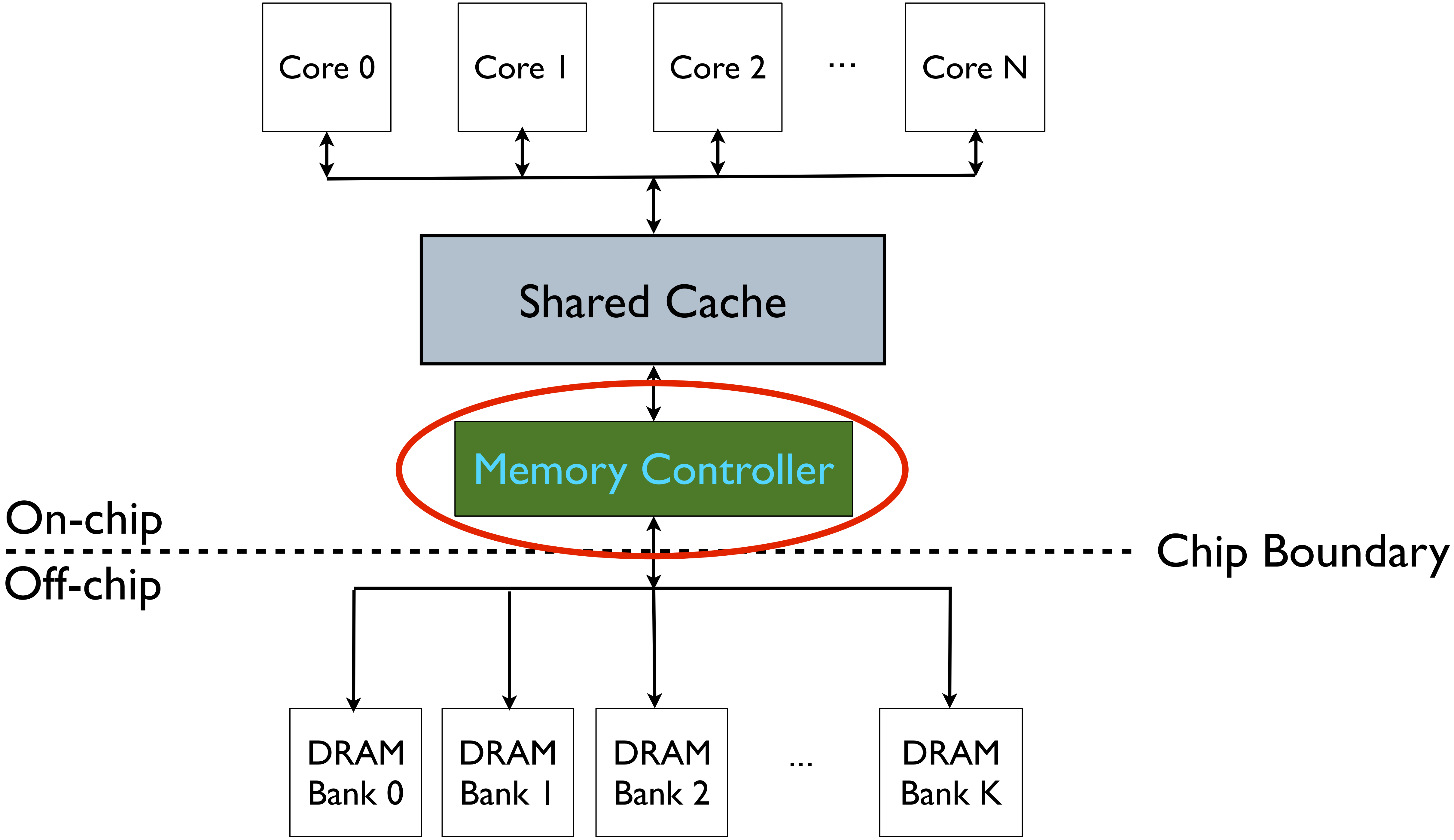

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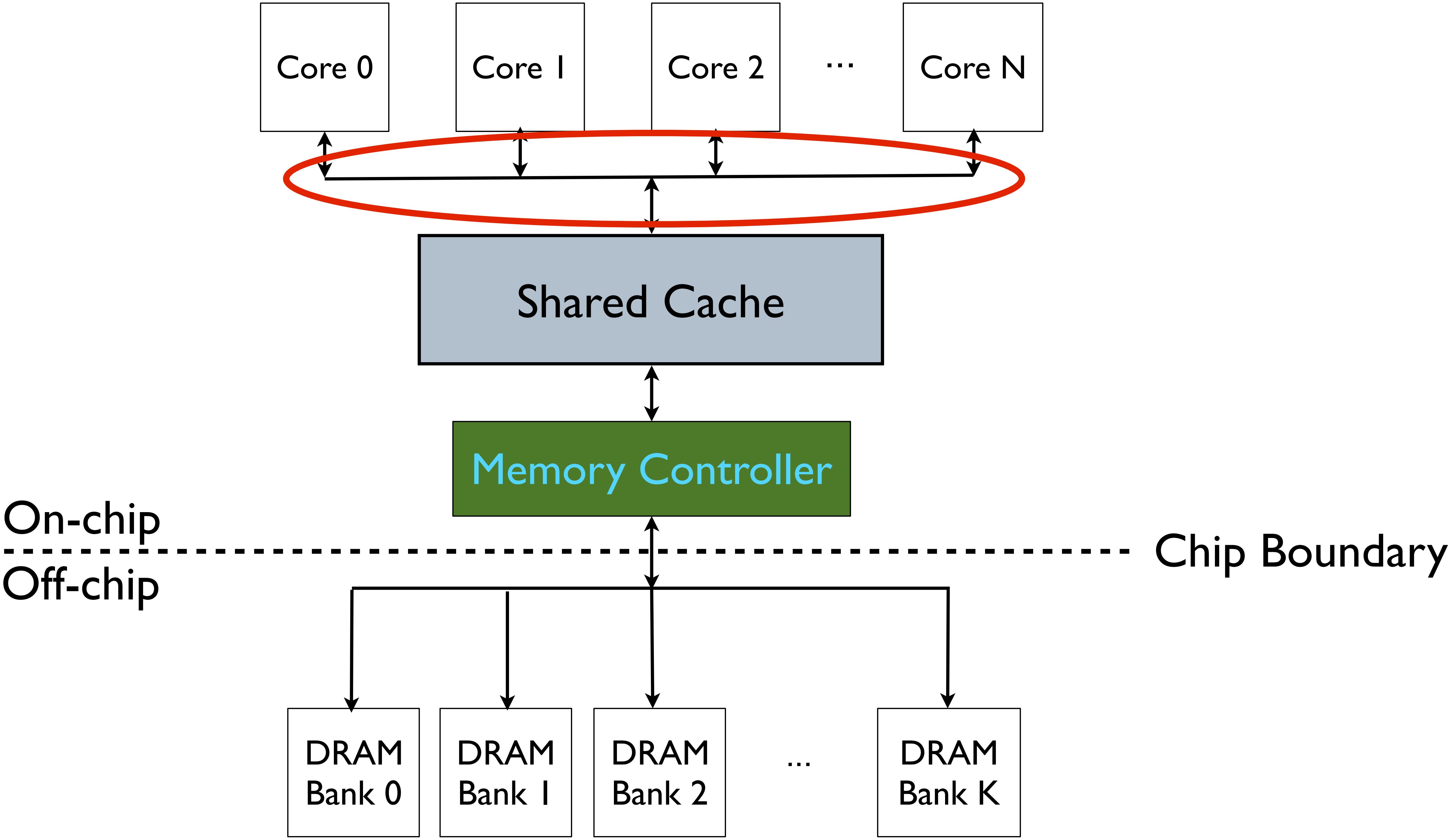

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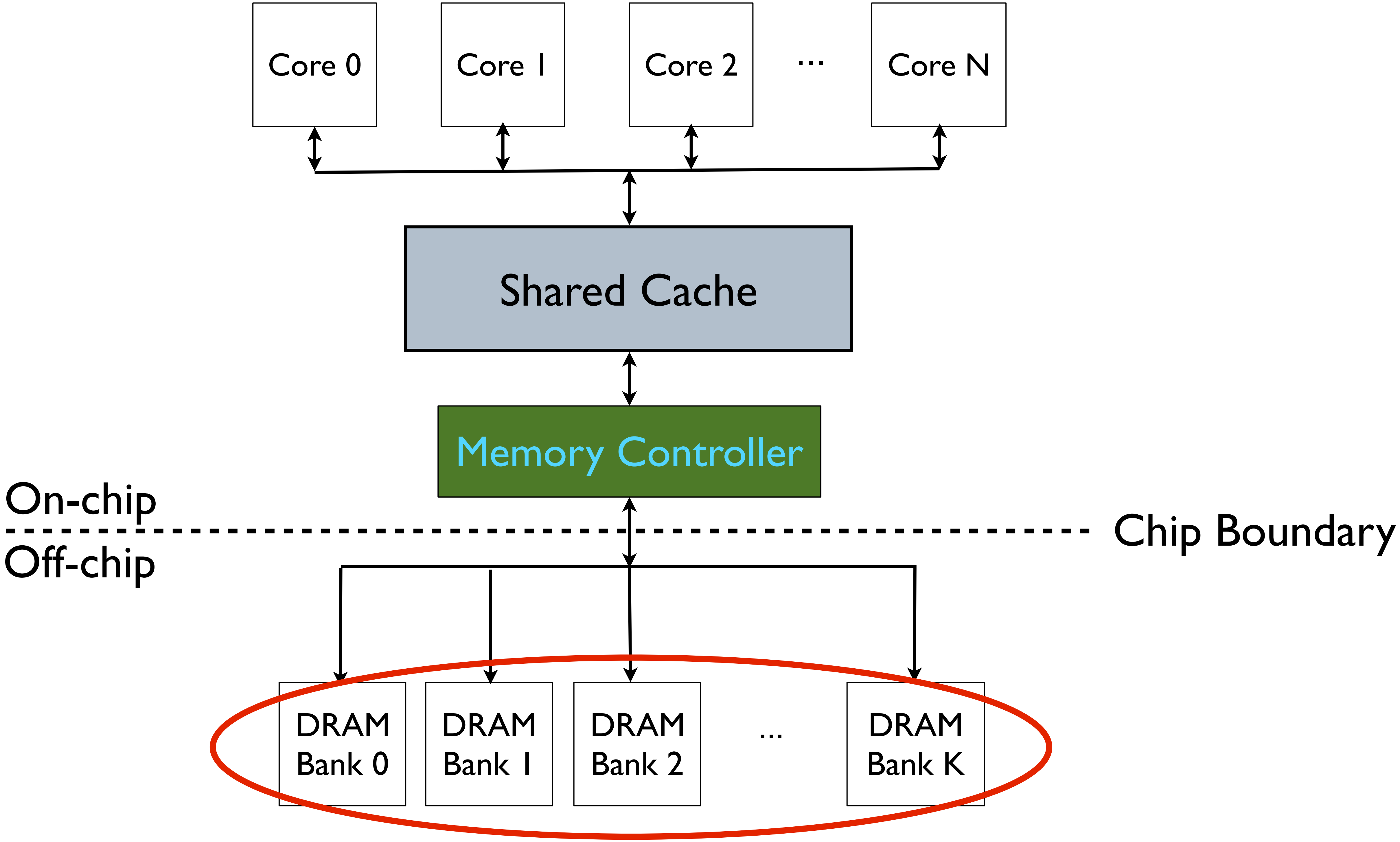

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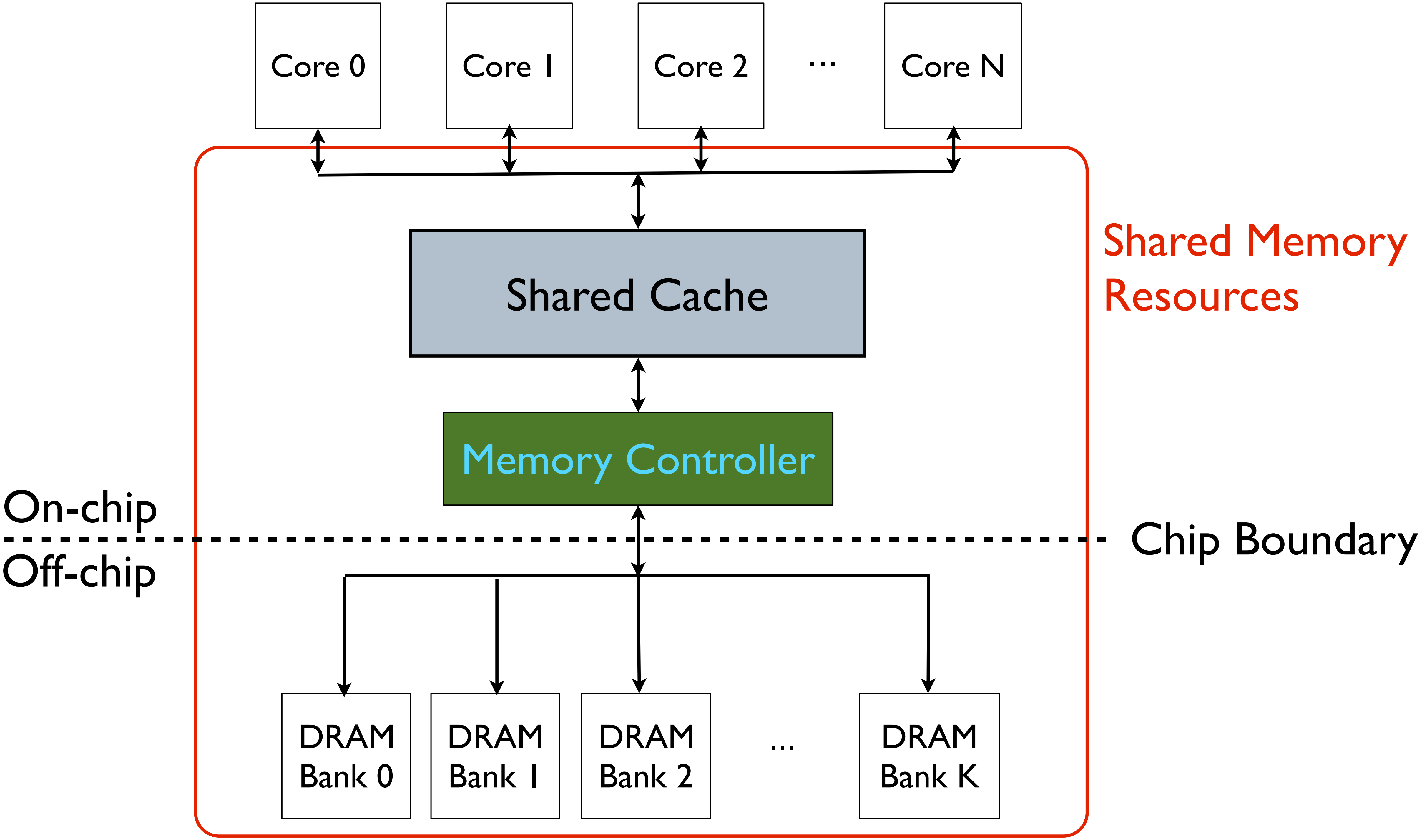

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- A memory system is **fair** if slowdowns of same-priority applications are equal (MICRO '06, MICRO '07, ISCA '08)
- Slowdown of application *i* = $\dfrac{T_i^{\text{Shared}}}{T_i^{\text{Alone}}}$
- Unfairness = $\dfrac{\text{Max}\{\text{Slowdown } i\} \text{ over all applications } i}{\text{Min}\{\text{Slowdown } i\} \text{ over all applications } i}$

(MICRO '07)

Background and Problem

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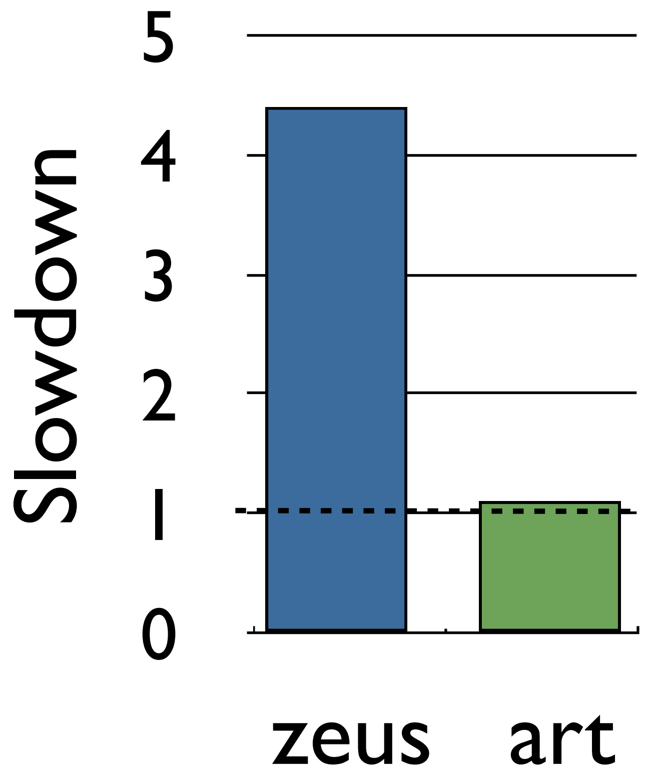

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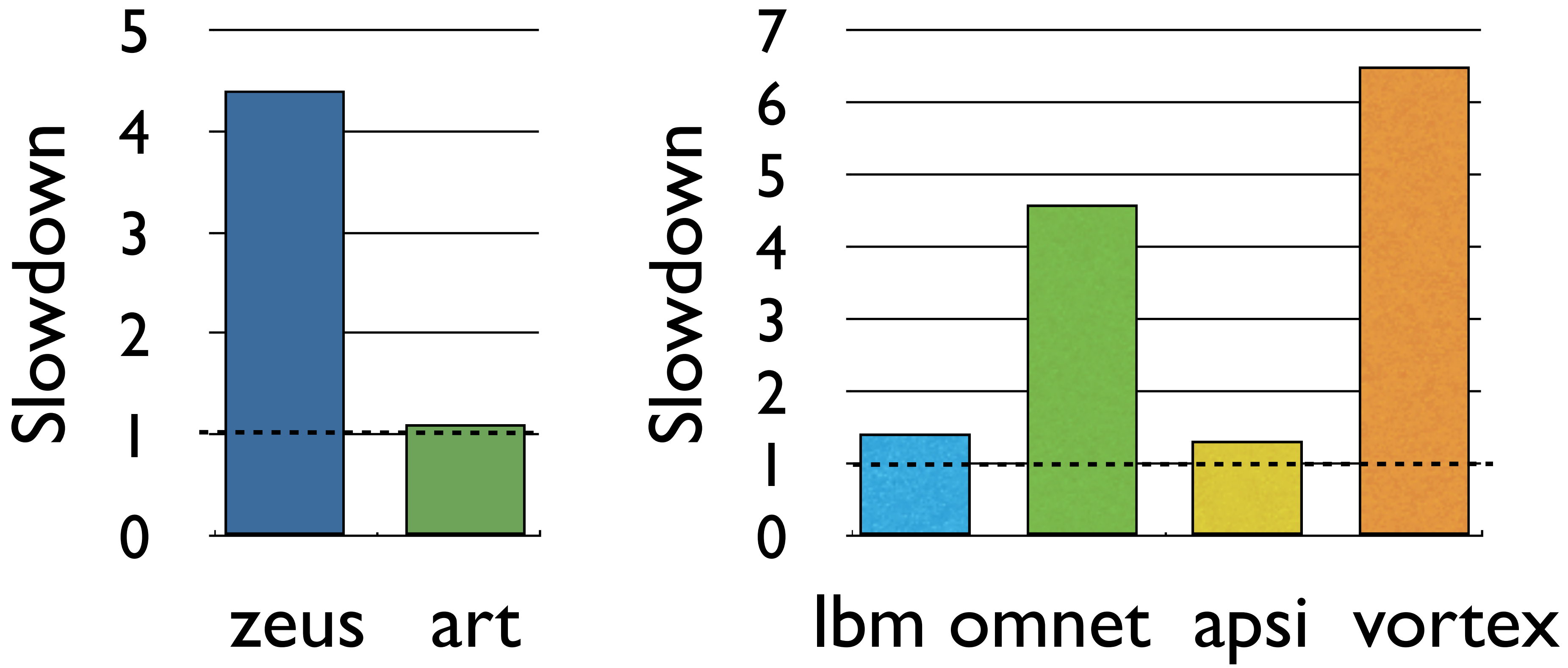

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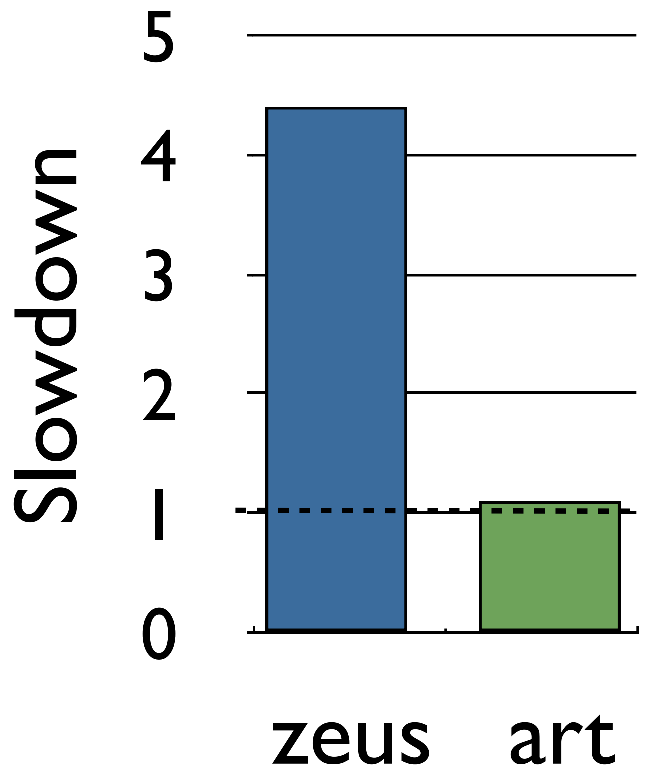

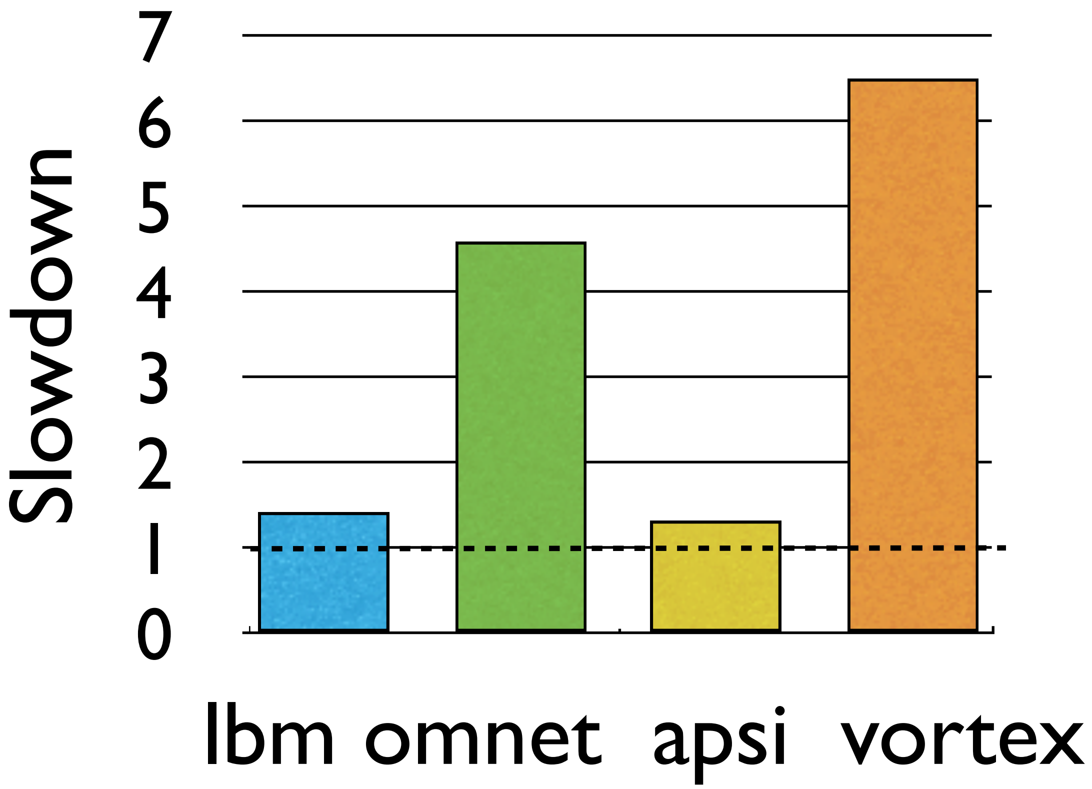

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Background and Problem

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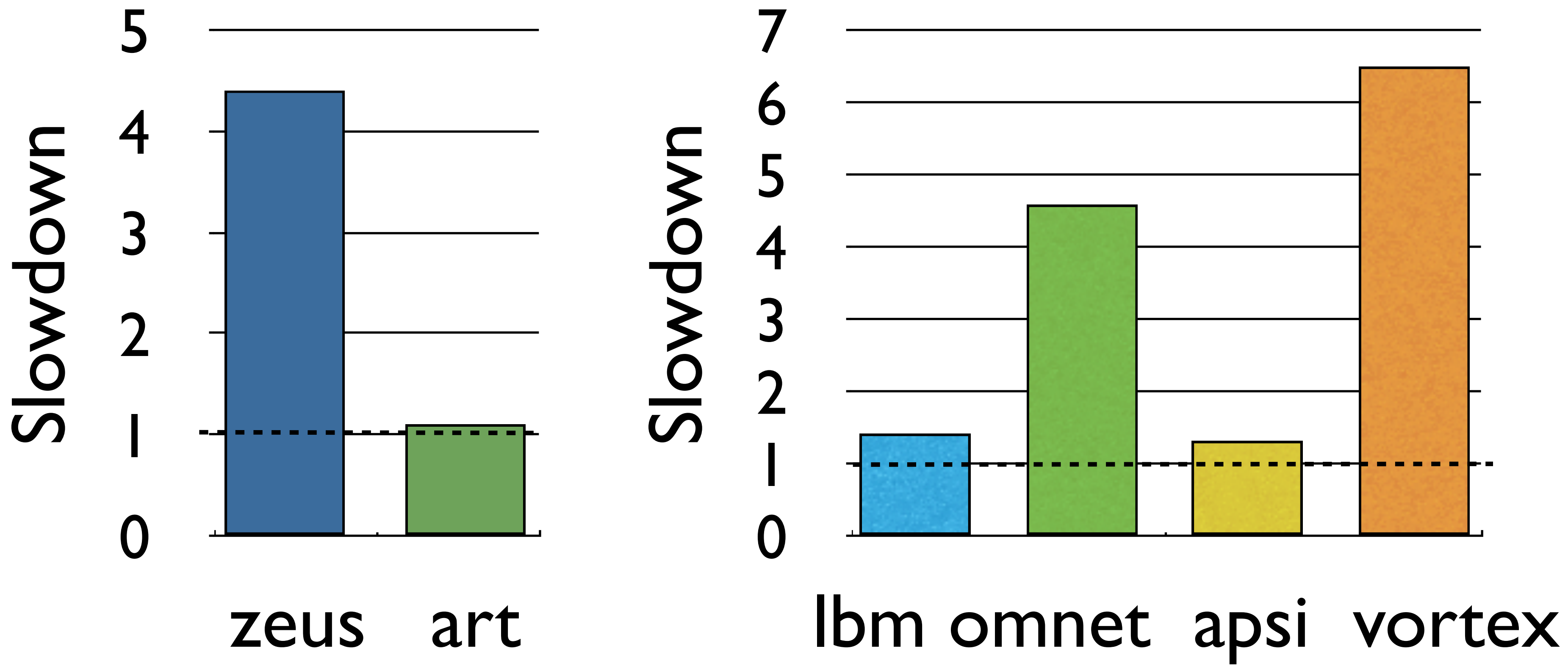

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  - Low system performance

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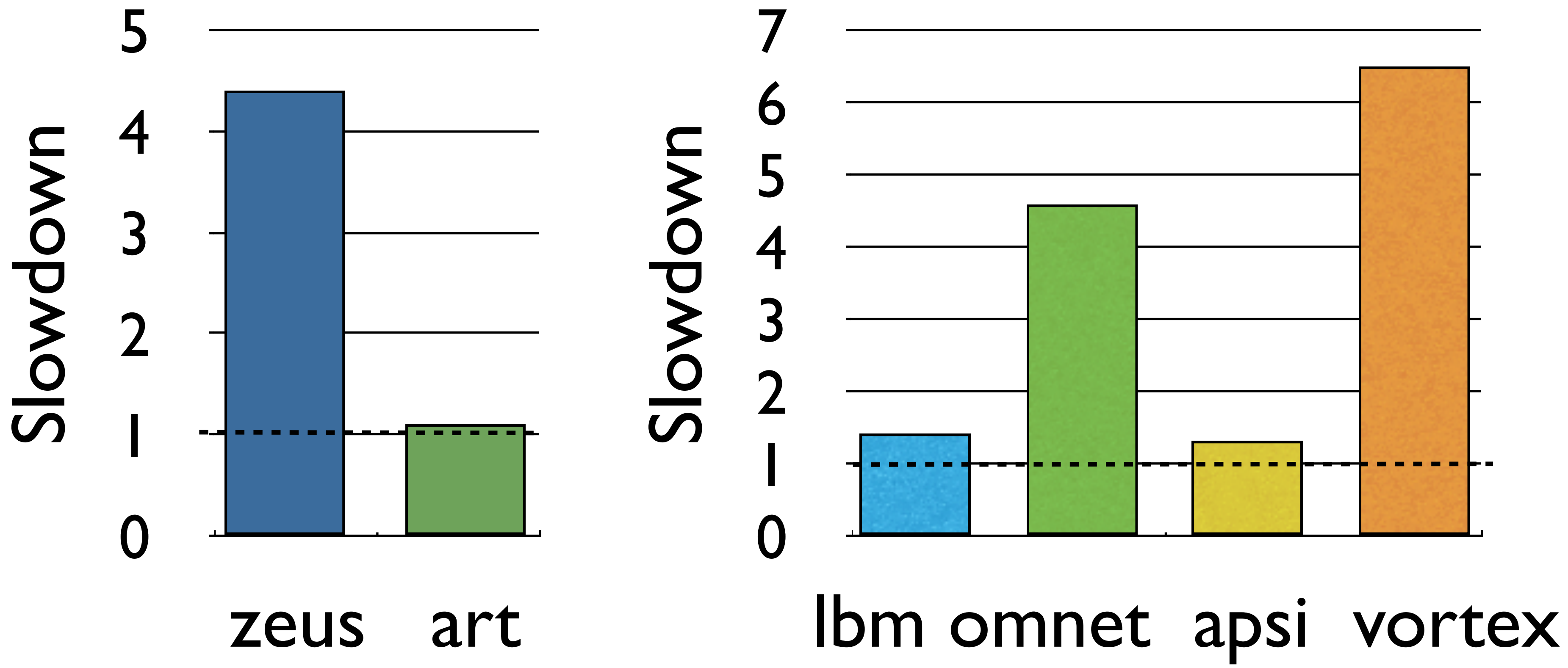

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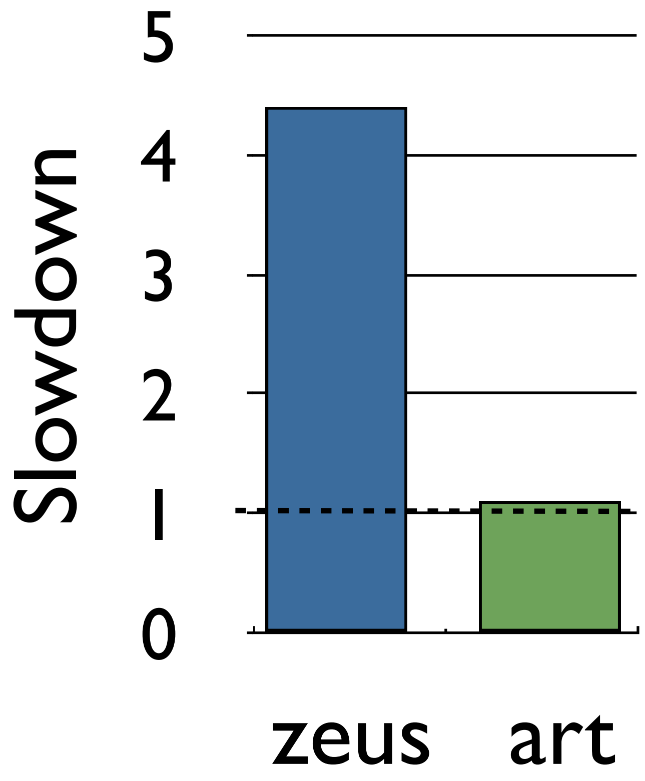

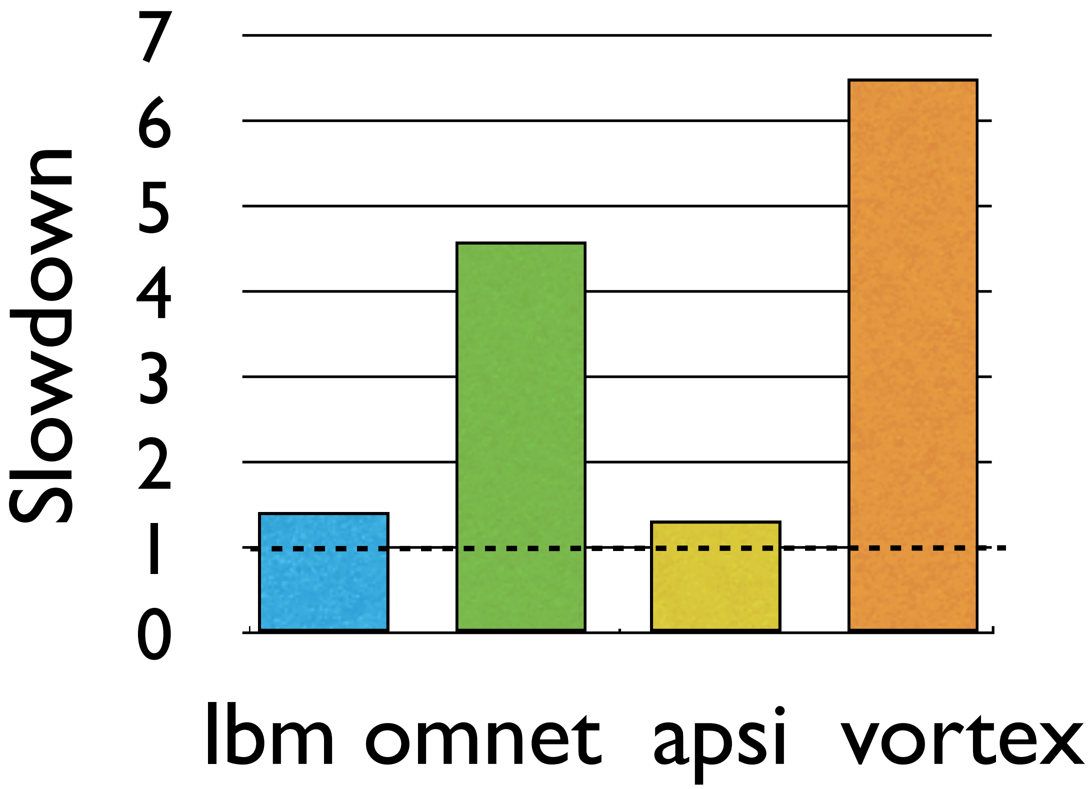

- Large disparities in slowdowns are unacceptable
  - Low system performance
  - Vulnerability to denial of service attacks
  - Difficult for system software to enforce priorities

Outline

- Background and Problem
- Motivation for Source Throttling
- Fairness via Source Throttling (FST)
- Evaluation
- Conclusion

Prior Approaches

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- Primarily manage inter-application interference in only one particular resource
  - Shared Cache, Memory Controller, Interconnect, etc.

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Our Goal: Enable fair sharing of the entire memory system by dynamically detecting and controlling interference in a coordinated manner

Our Approach

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- Manage inter-application interference at the cores, not at the shared resources
- Dynamically estimate unfairness in the memory system
- If unfairness > system-software-specified target then
  throttle down core causing unfairness &
  throttle up core that was unfairly treated

Unmanaged Interference

A:

B:

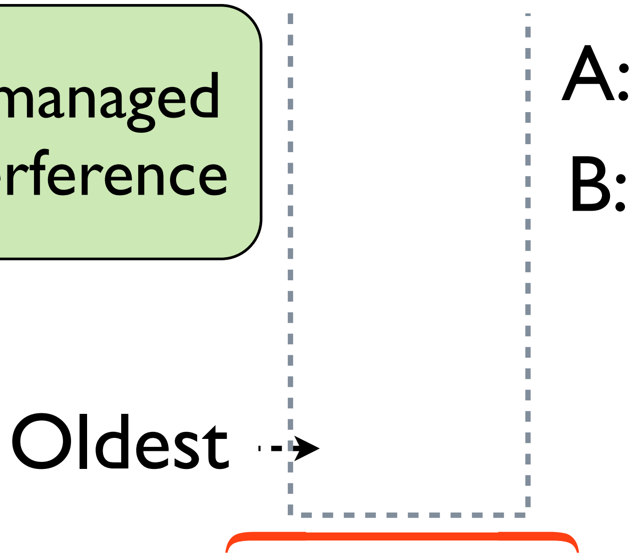
Fair Source Throttling

A:

B:

queue of requests to shared resources

Unmanaged Interference

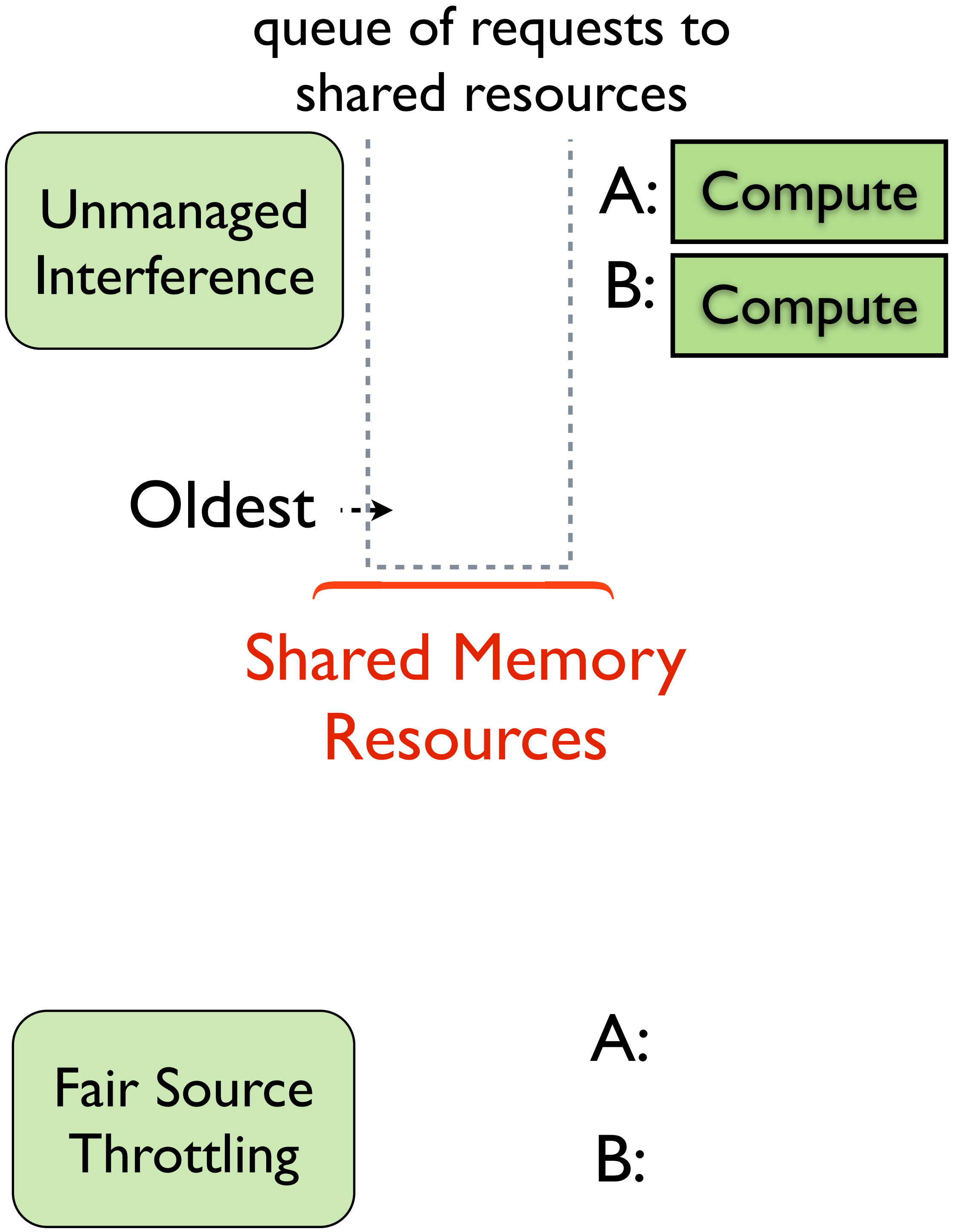


Shared Memory Resources

Fair Source Throttling

A:

B:



queue of requests to shared resources

Unmanaged Interference

A: Compute

B: Compute

Oldest

Shared Memory Resources

Fair Source Throttling

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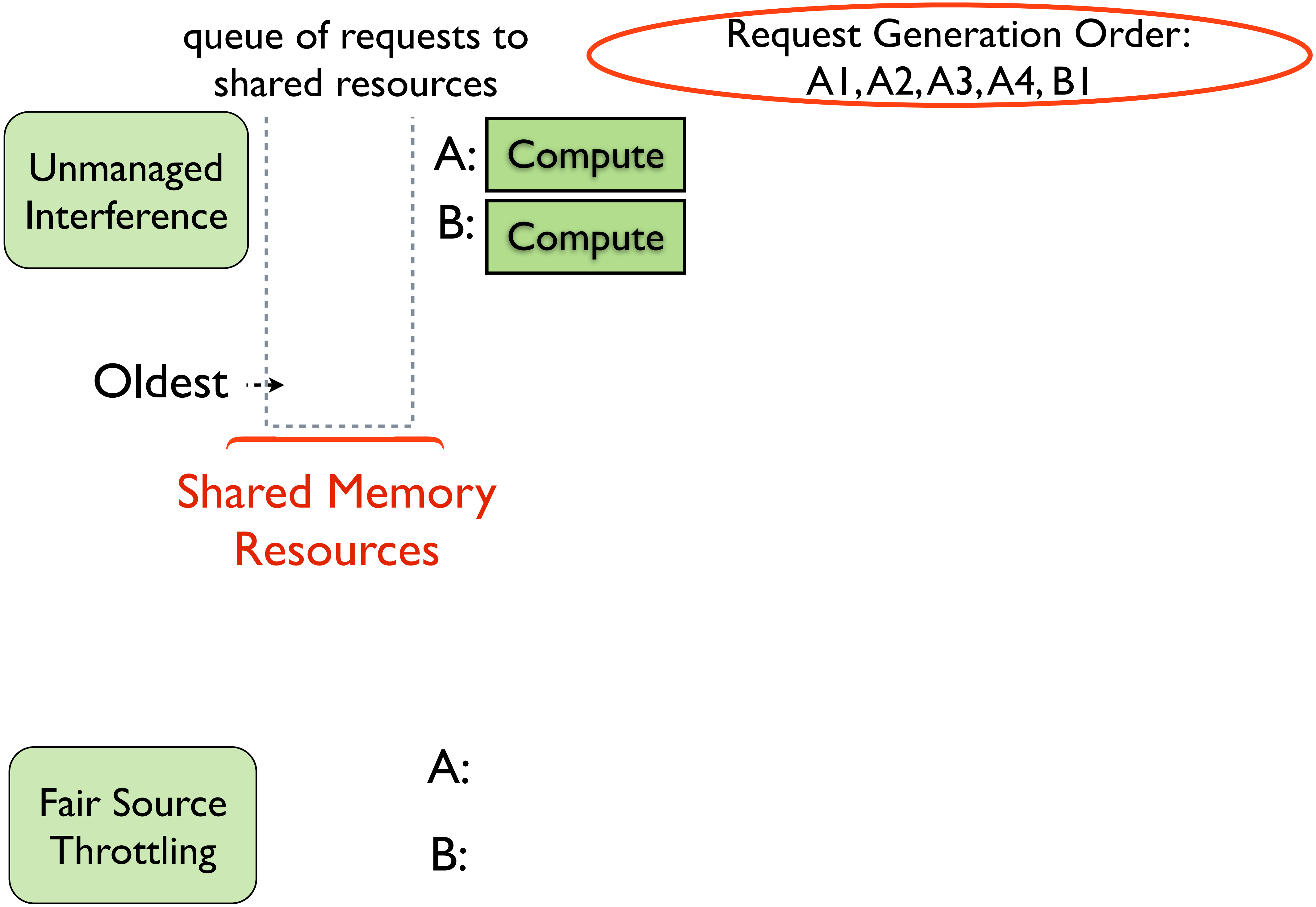

queue of requests to shared resources

Request Generation Order: A1, A2, A3, A4, B1

Unmanaged Interference

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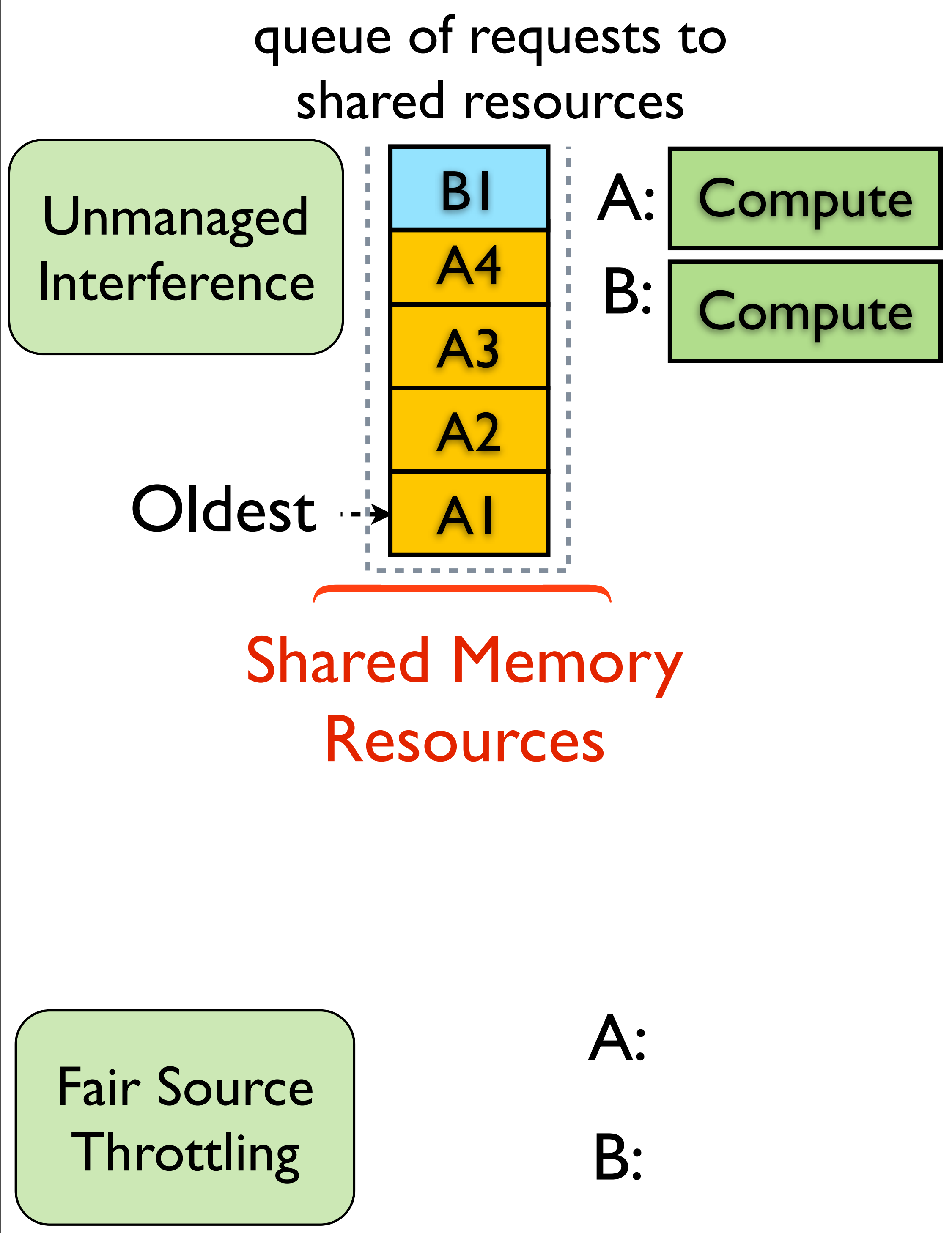

queue of requests to shared resources

Unmanaged Interference

B1

A4

A3

A2

Oldest A1

A: Compute

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Shared Memory Resources

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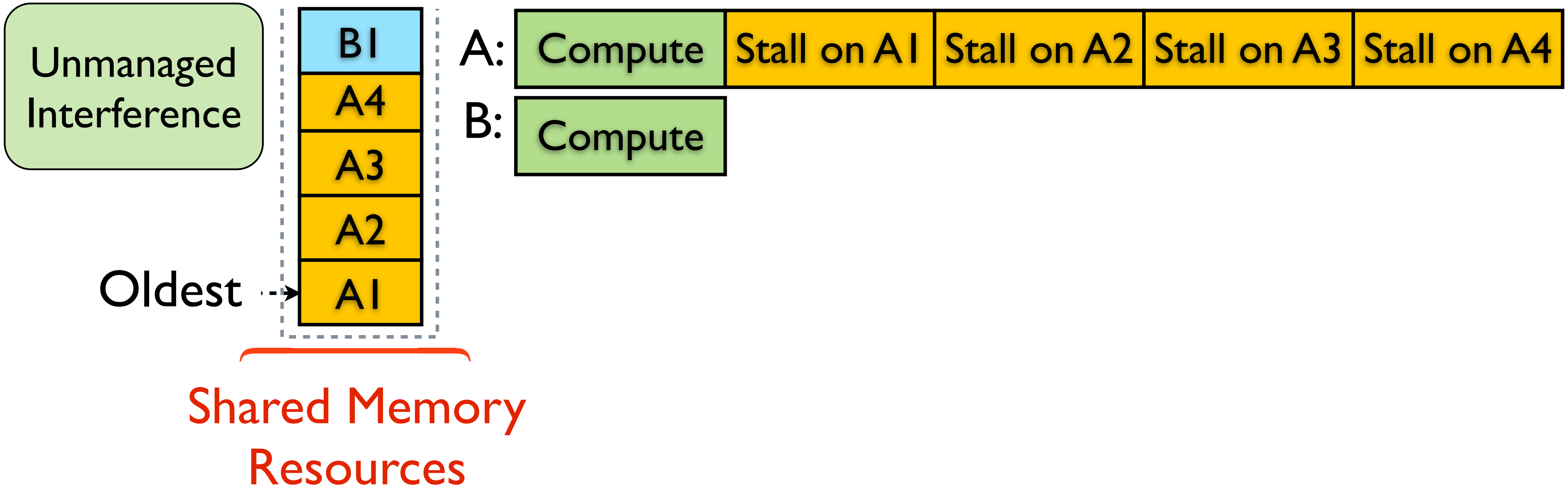

Unmanaged Interference

B1

A4

A3

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Oldest

A: Compute | Stall on A1 | Stall on A2 | Stall on A3 | Stall on A4

B: Compute

Shared Memory Resources

Fair Source Throttling

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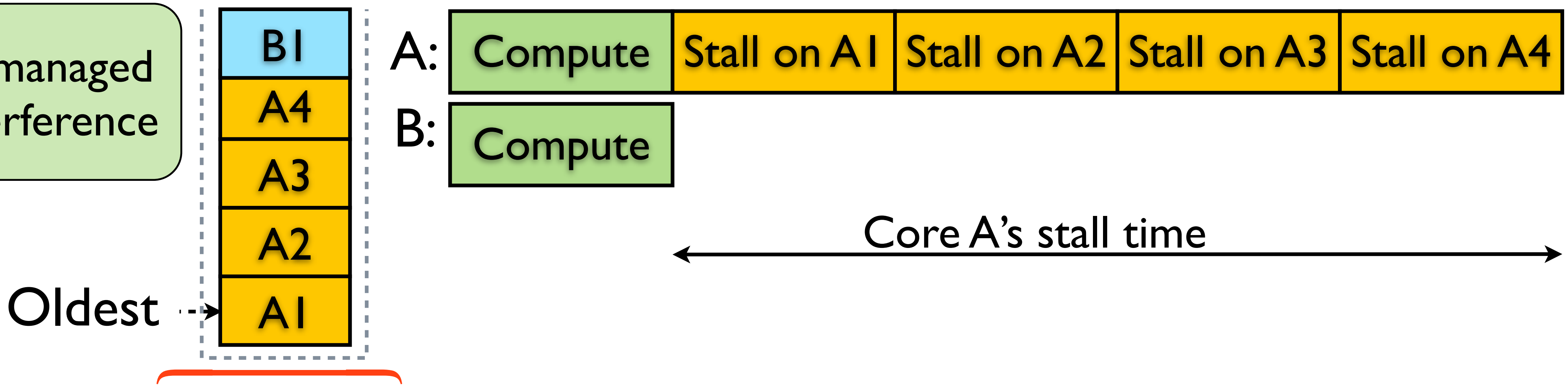

B1

A4

A3

A2

Oldest → A1

A: Compute | Stall on A1 | Stall on A2 | Stall on A3 | Stall on A4

B: Compute

Core A's stall time

Shared Memory Resources

Fair Source Throttling

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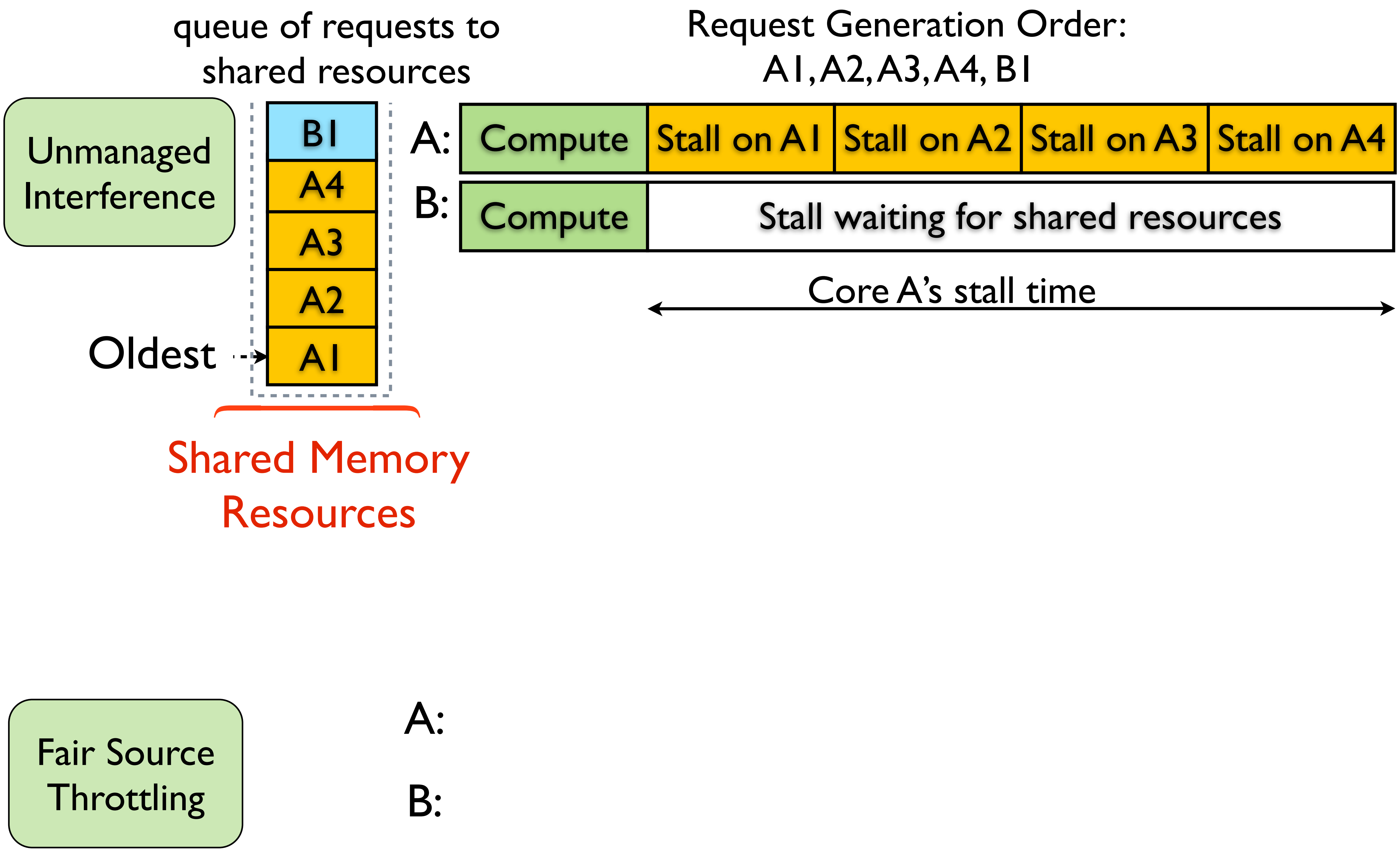

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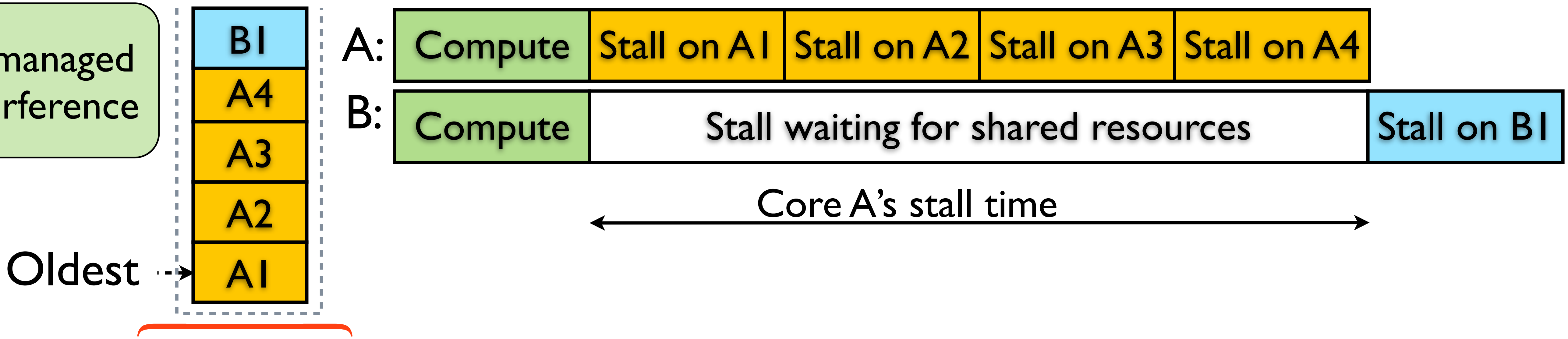

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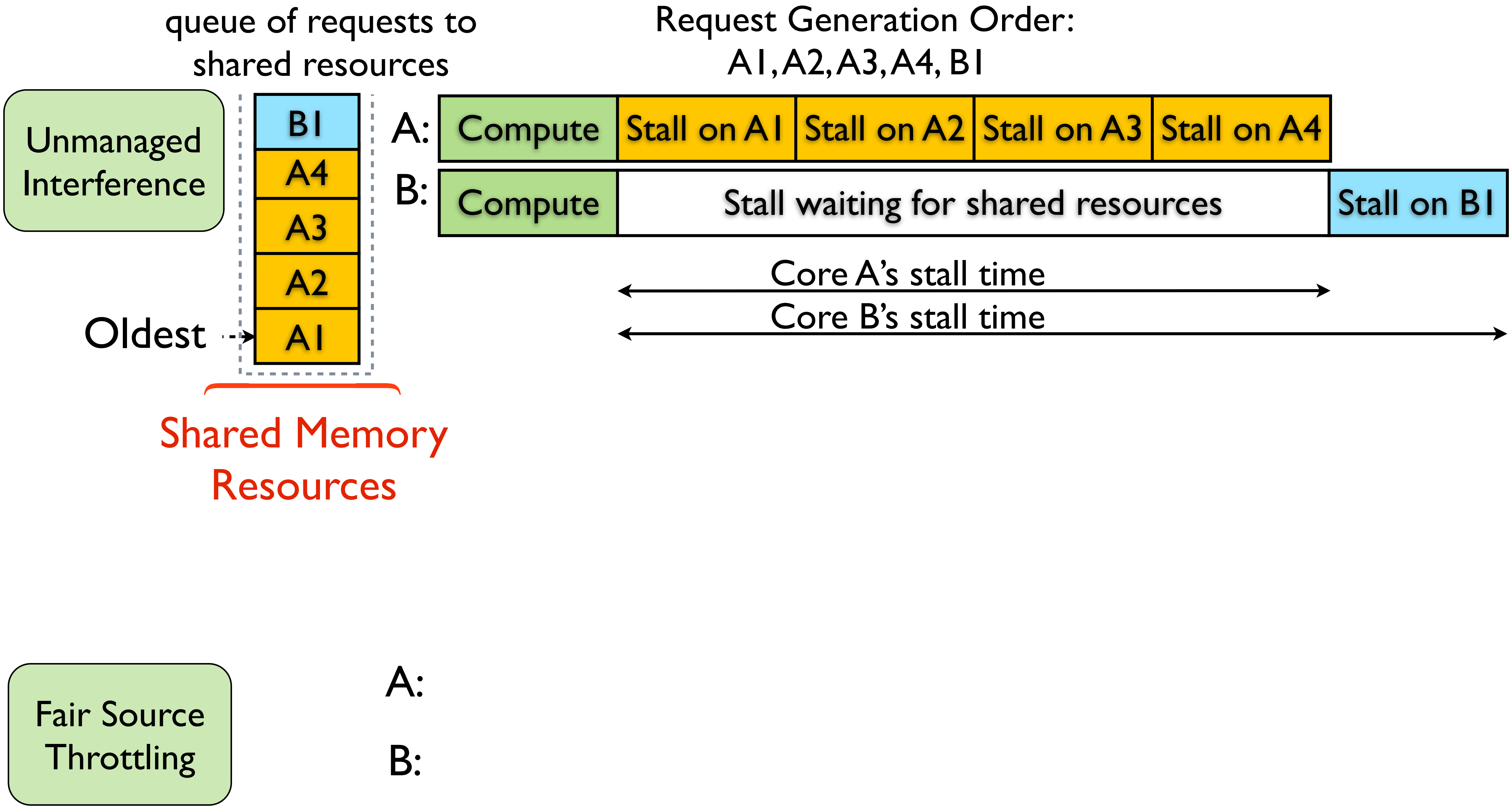

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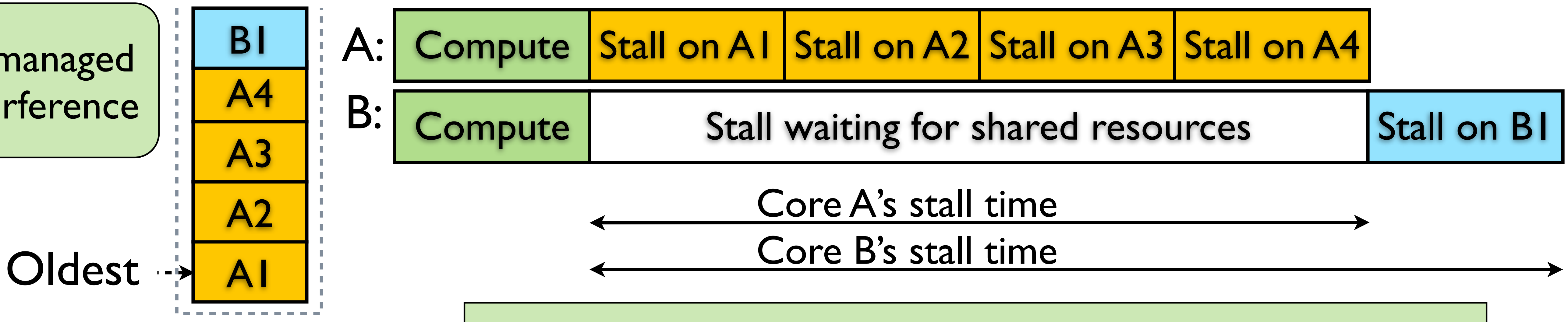

Shared Memory Resources

Intensive application A generates many requests and causes long stall times for less intensive application B

Fair Source Throttling

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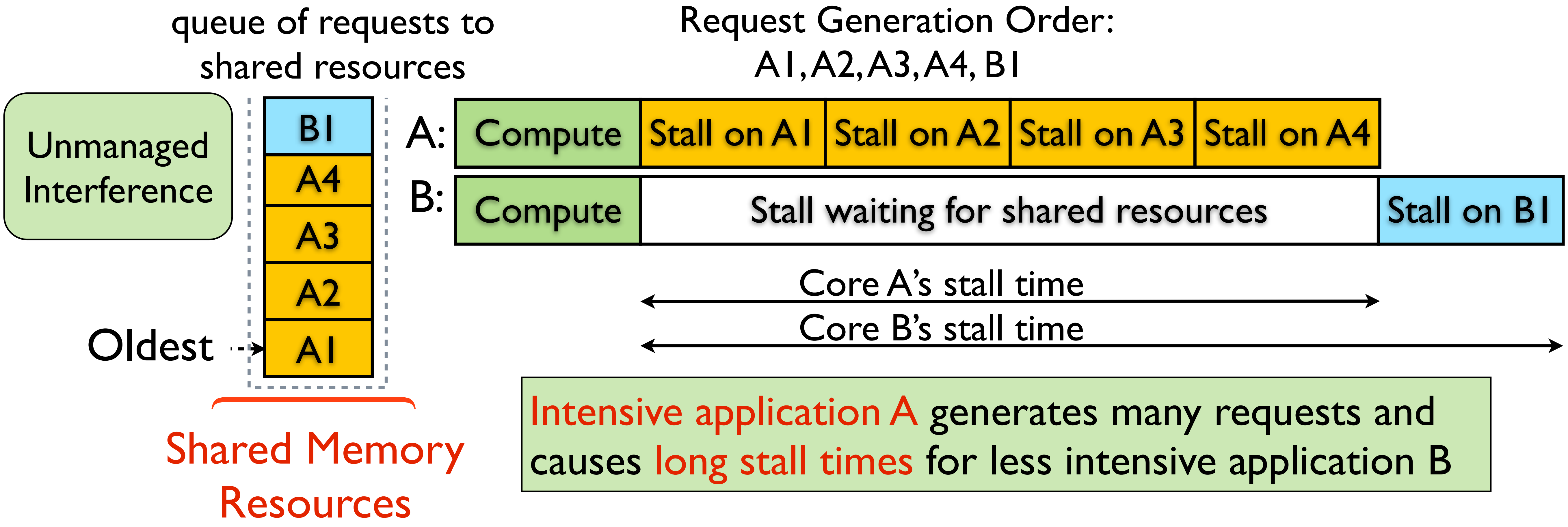
B:



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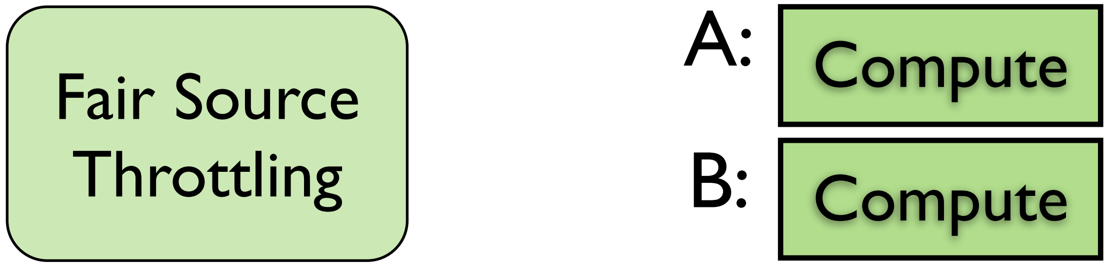

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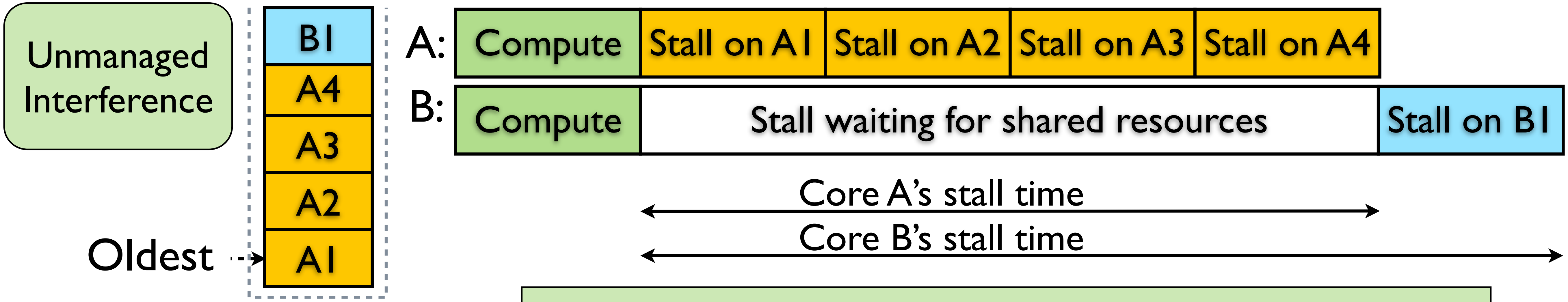

Shared Memory Resources

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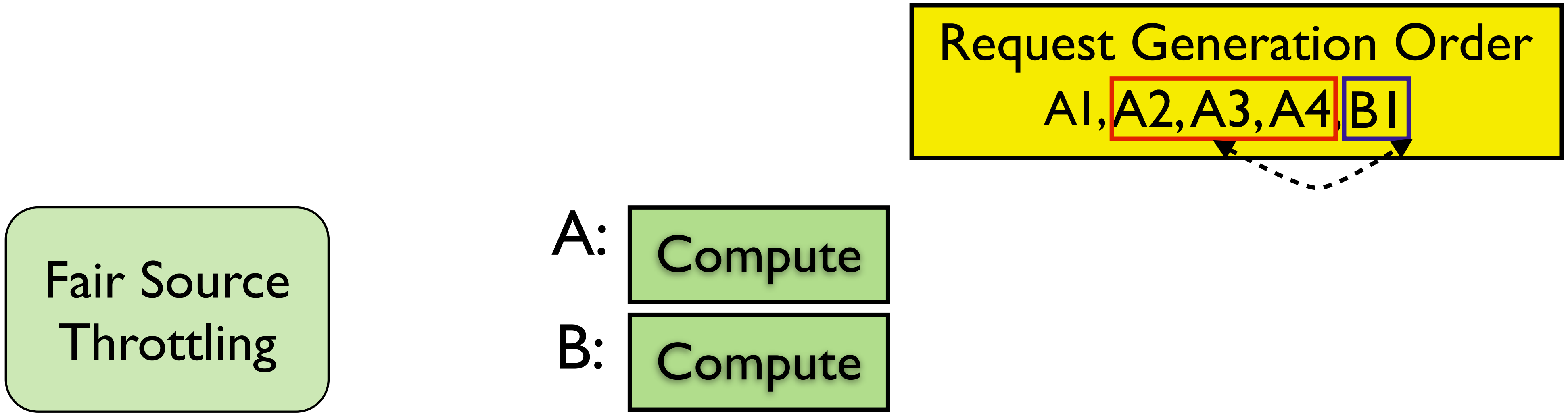

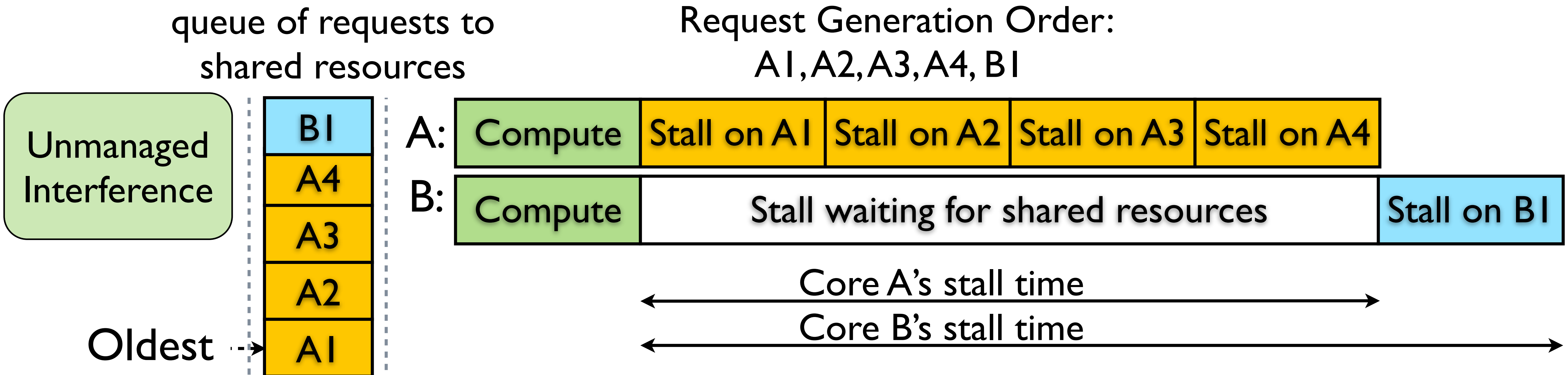

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A1, A2, A3, A4, B1

Unmanaged Interference

B1
A4
A3
A2
A1

Oldest

A: Compute | Stall on A1 | Stall on A2 | Stall on A3 | Stall on A4

B: Compute | Stall waiting for shared resources | Stall on B1

Core A's stall time

Core B's stall time

Shared Memory Resources

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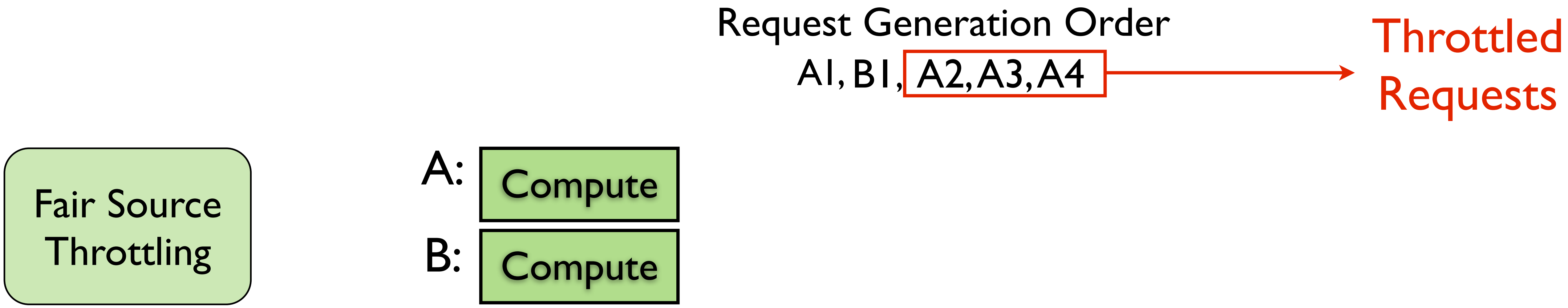


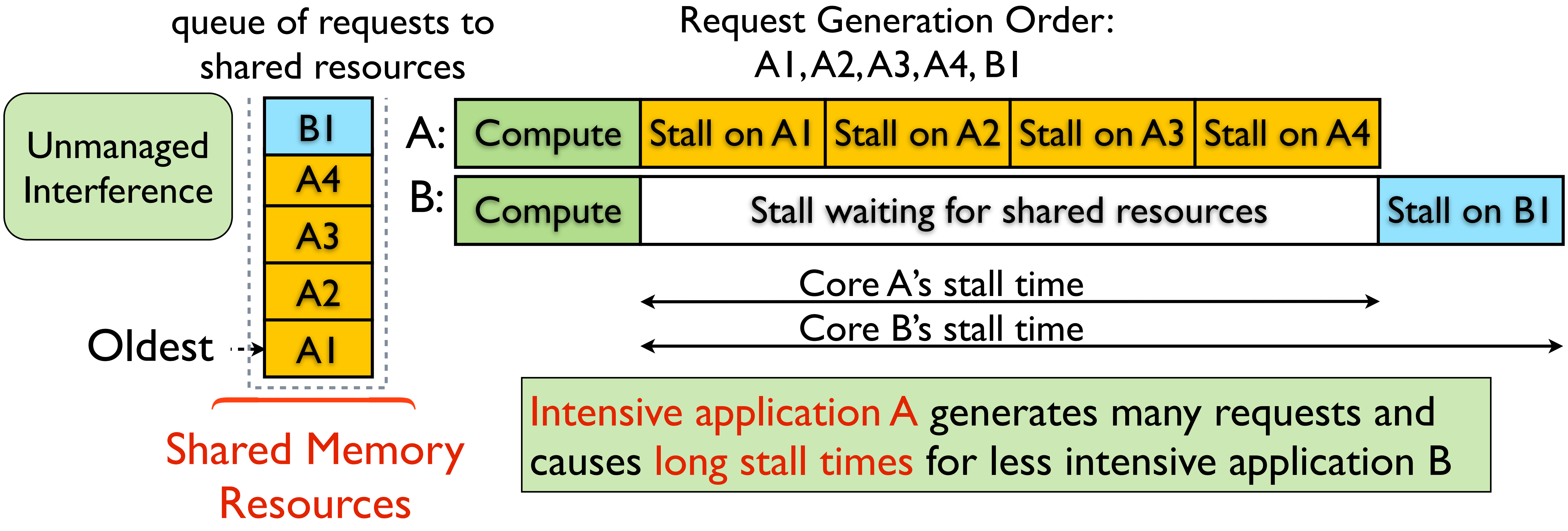
Request Generation Order
A1, B1, A2, A3, A4

Throttled Requests

Fair Source Throttling

A: Compute

B: Compute



Unmanaged Interference

queue of requests to shared resources

B1

A4

A3

A2

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Oldest

Shared Memory Resources

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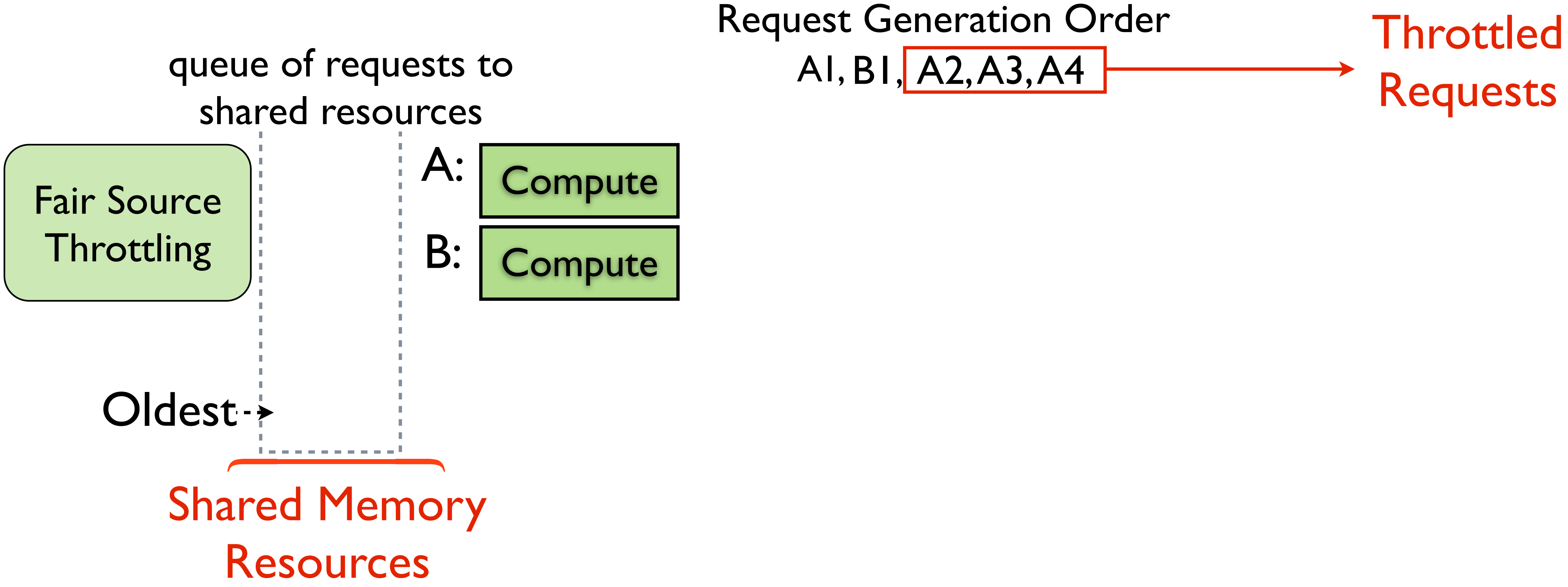

Fair Source Throttling

queue of requests to shared resources

Oldest

Shared Memory Resources

Request Generation Order

A1, B1, A2, A3, A4

Throttled Requests

A: Compute

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queue of requests to shared resources

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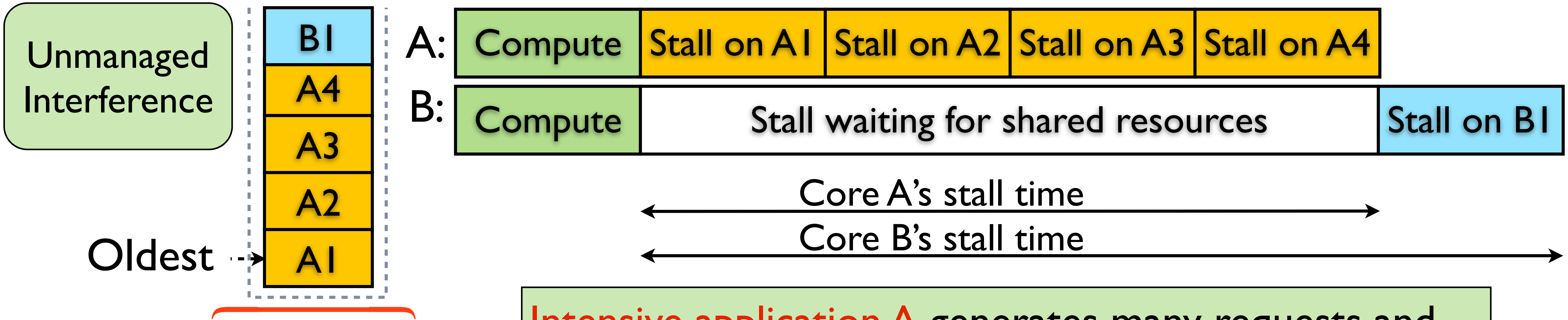

Shared Memory Resources

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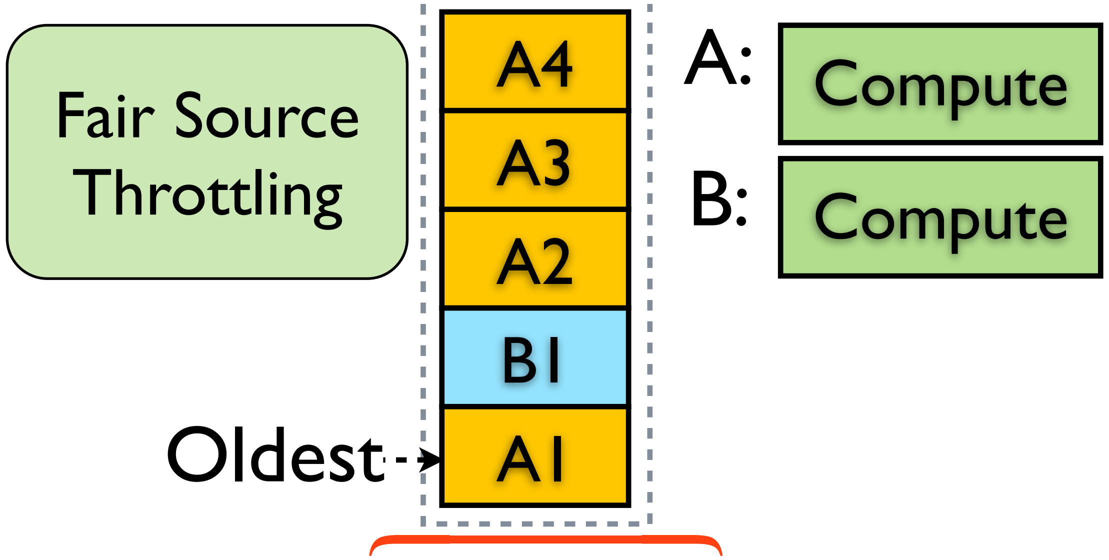
Request Generation Order
A1, B1, A2, A3, A4 → Throttled Requests

queue of requests to shared resources



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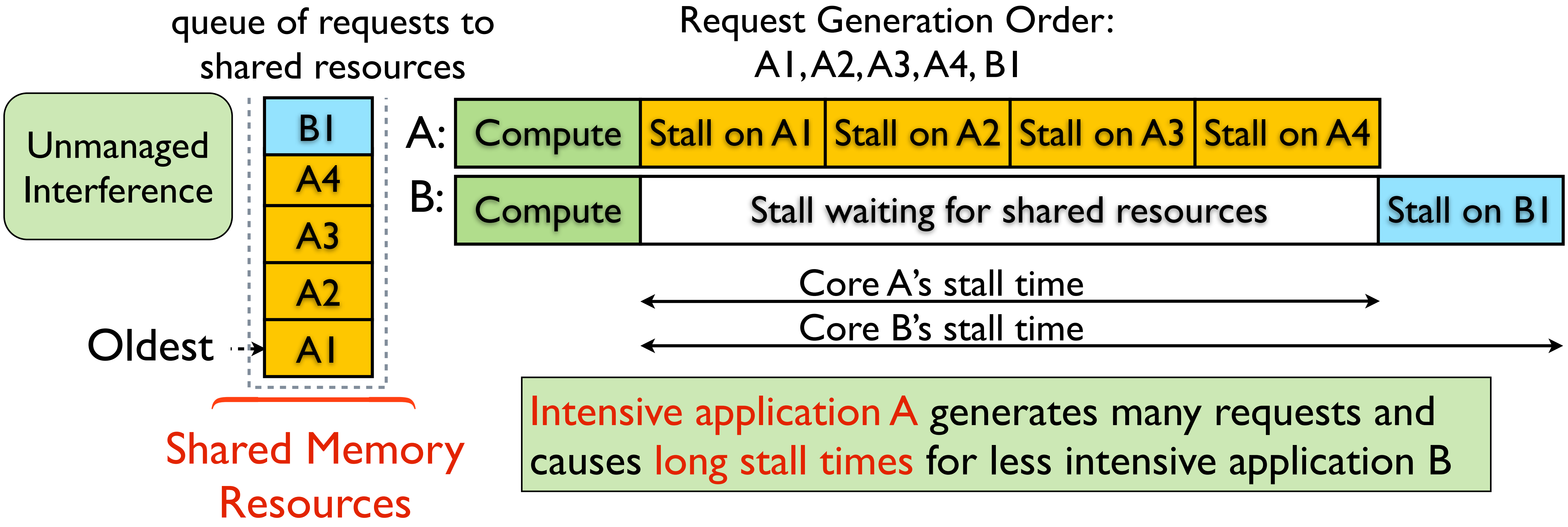

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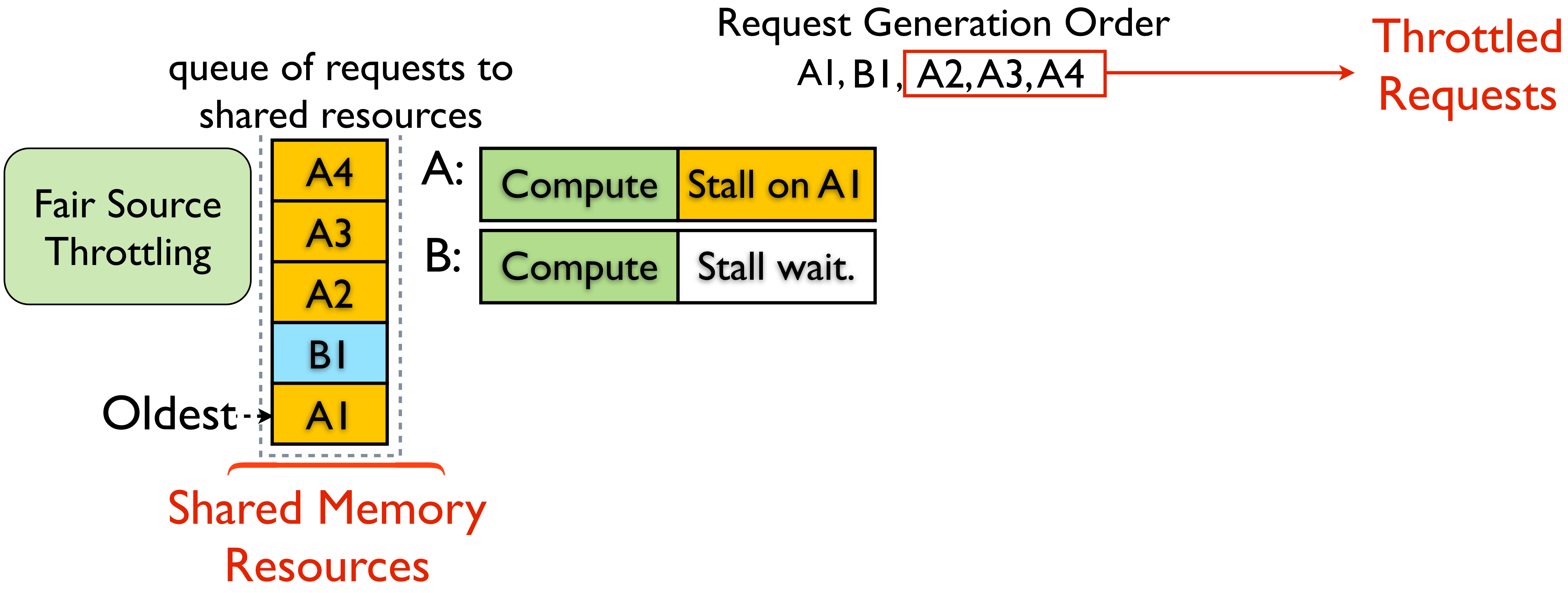

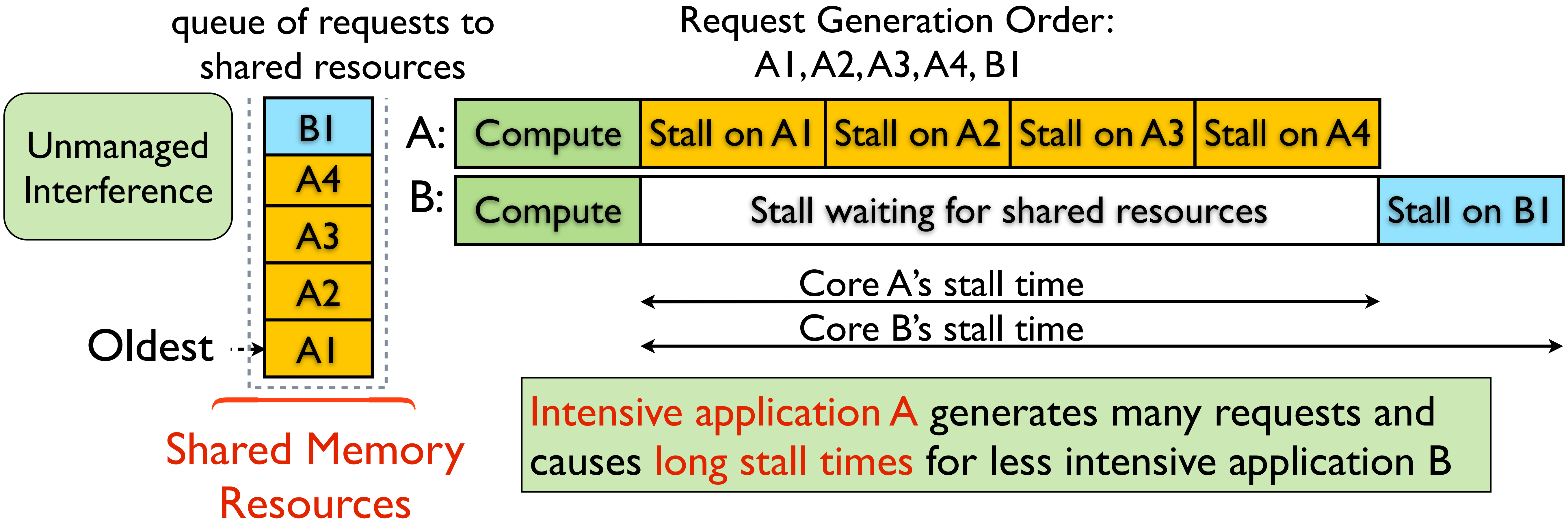

queue of requests to shared resources

Request Generation Order: A1, A2, A3, A4, B1

Unmanaged Interference

B1

A4

A3

A2

Oldest → A1

A: Compute | Stall on A1 | Stall on A2 | Stall on A3 | Stall on A4

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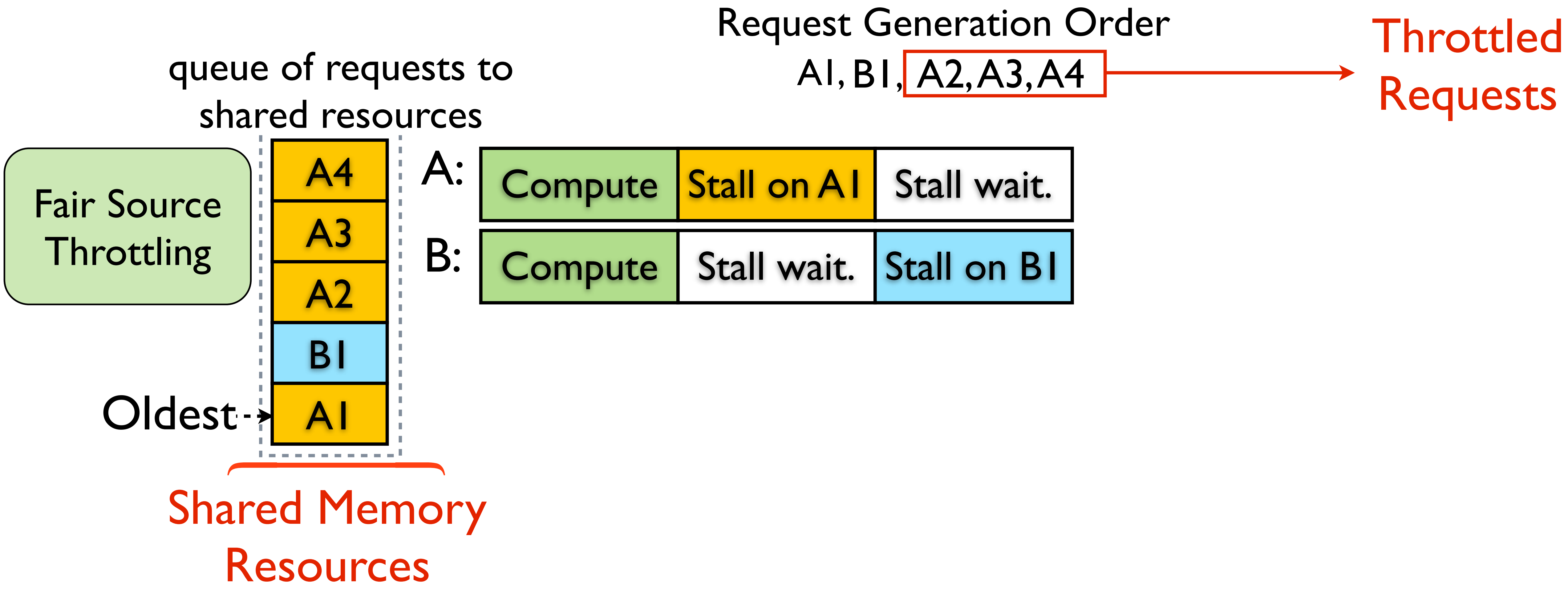
Core A's stall time

Core B's stall time

Shared Memory Resources

Intensive application A generates many requests and causes long stall times for less intensive application B



Request Generation Order

A1, B1, A2, A3, A4 → Throttled Requests

queue of requests to shared resources

Fair Source Throttling

A4

A3

A2

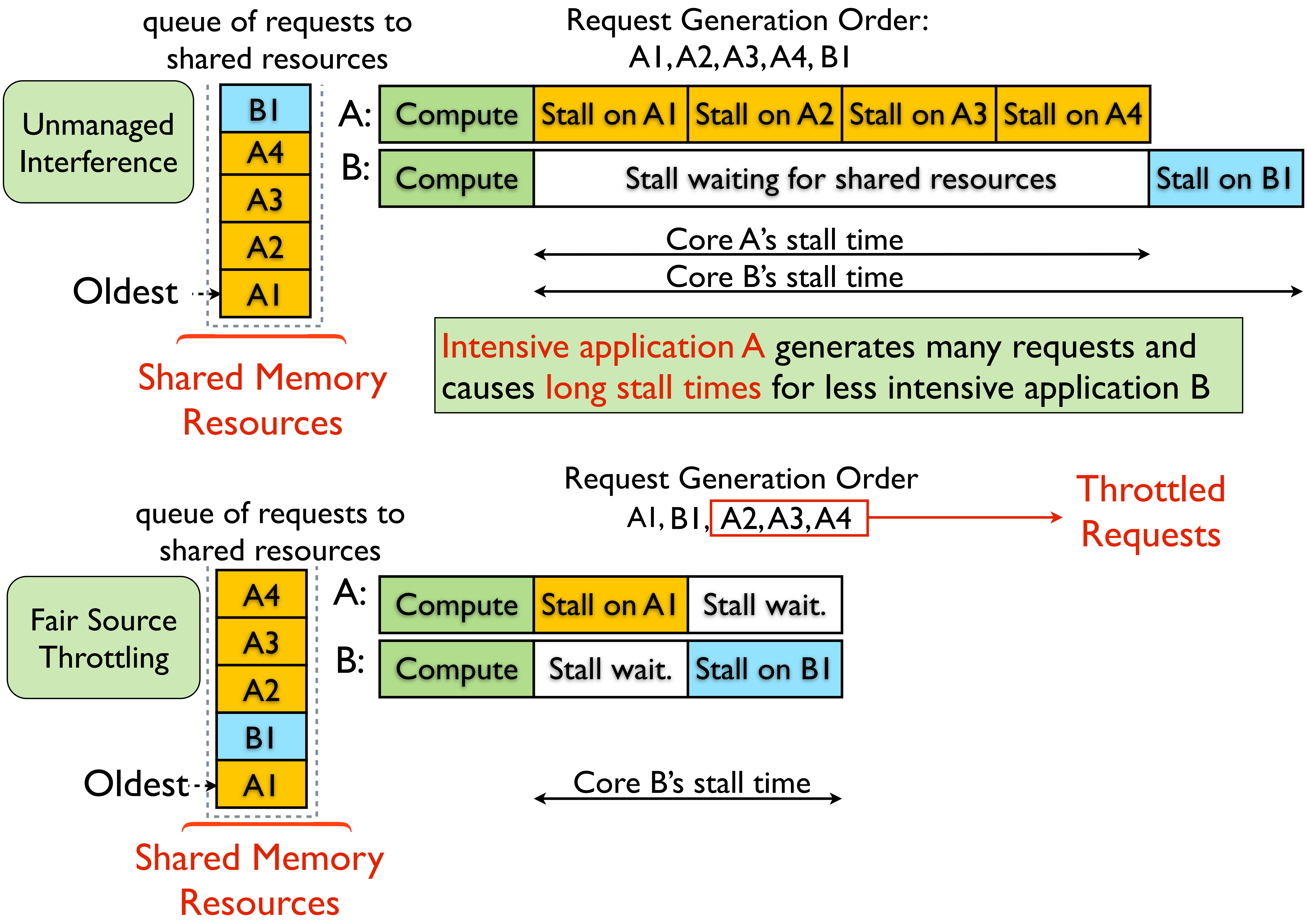
B1

Oldest → A1

A: Compute | Stall on A1 | Stall wait.

B: Compute | Stall wait. | Stall on B1

Shared Memory Resources



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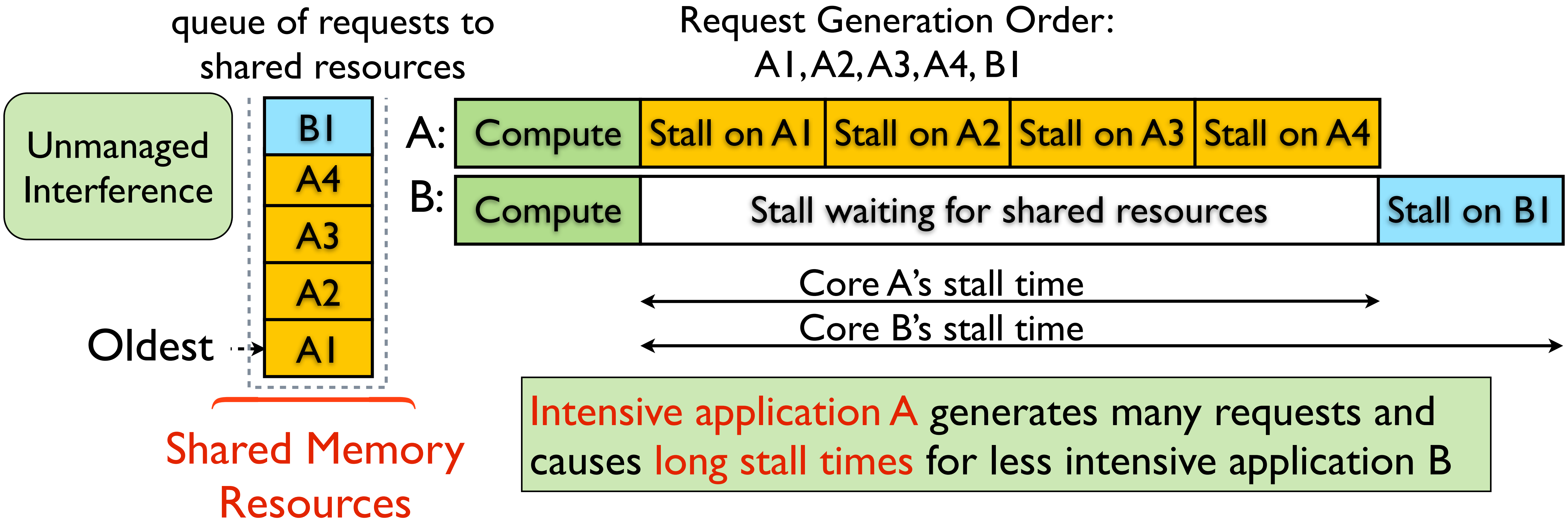

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Unmanaged Interference

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Shared Memory Resources

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Core A's stall time

Core B's stall time

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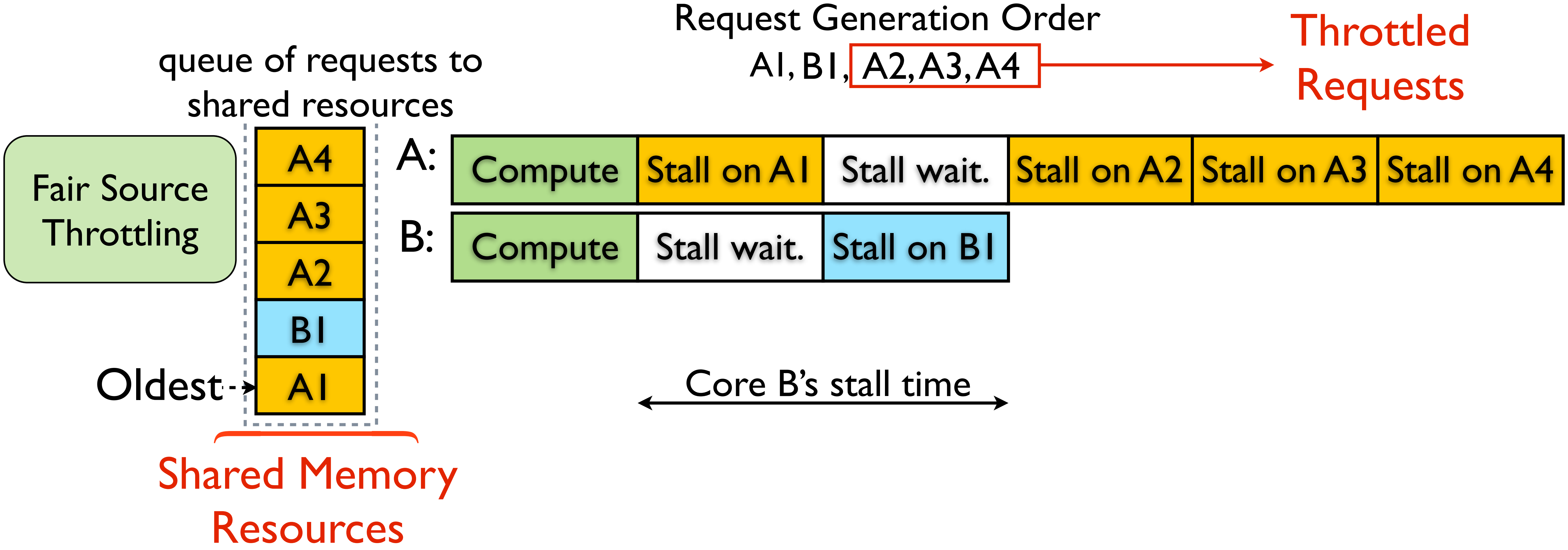

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queue of requests to shared resources

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Oldest A1

Shared Memory Resources

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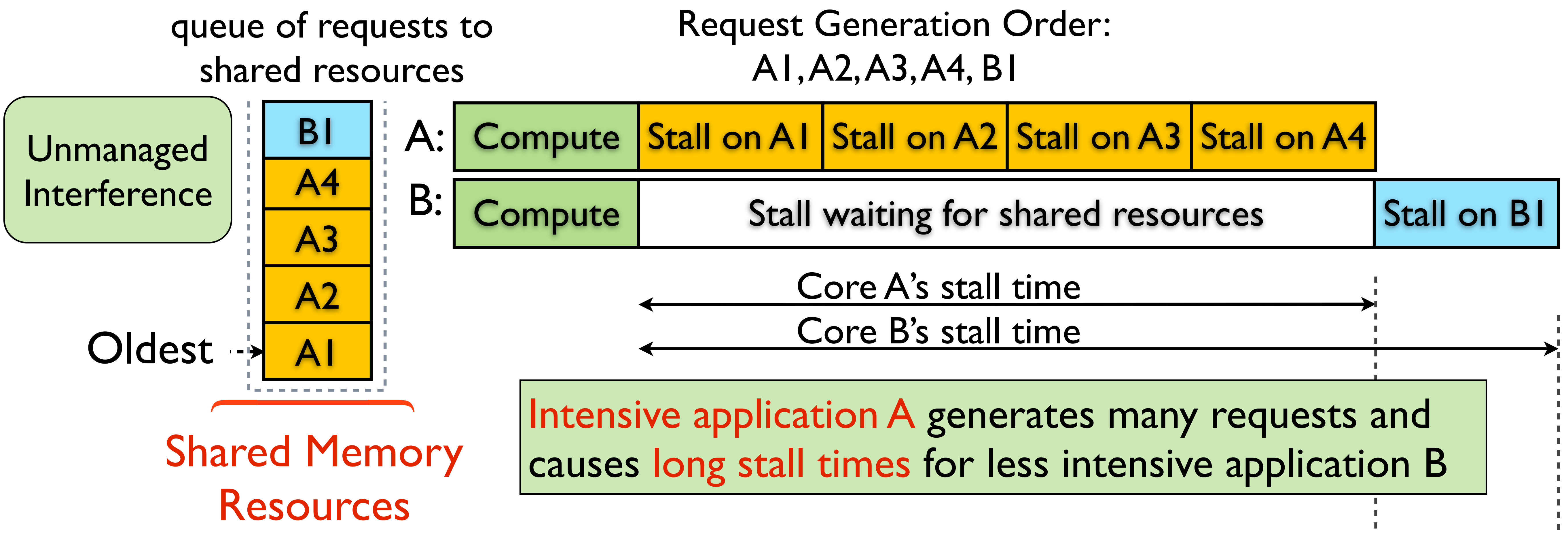
B: Compute | Stall wait. | Stall on B1

Core B's stall time



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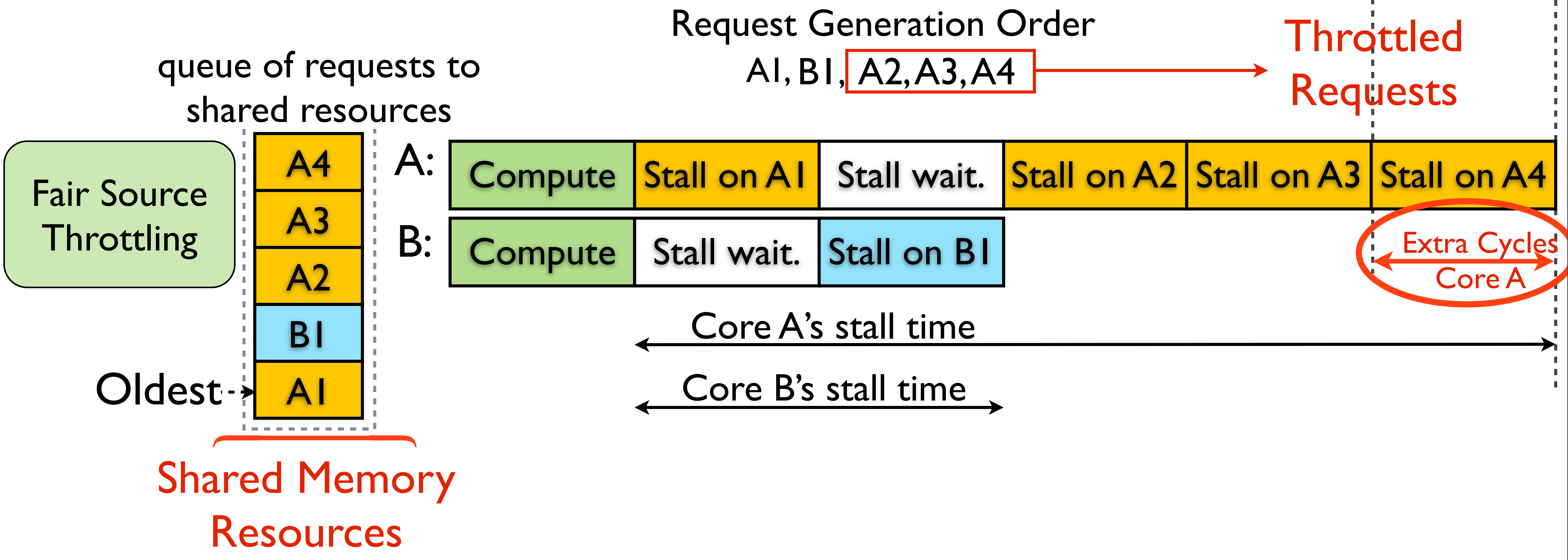

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queue of requests to shared resources

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Oldest → A1

A: Compute | Stall on A1 | Stall wait. | Stall on A2 | Stall on A3 | Stall on A4

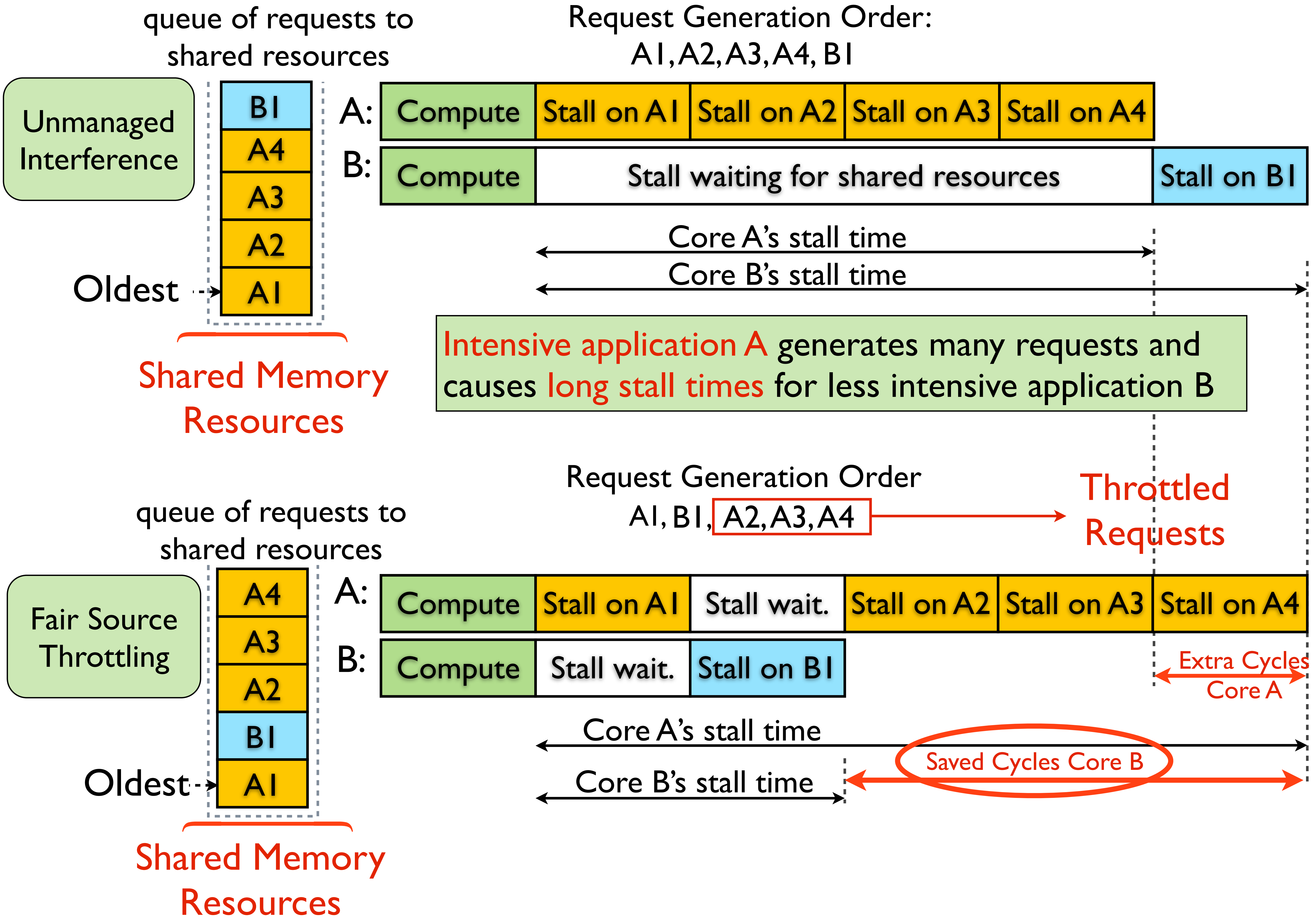
B: Compute | Stall wait. | Stall on B1

Extra Cycles Core A

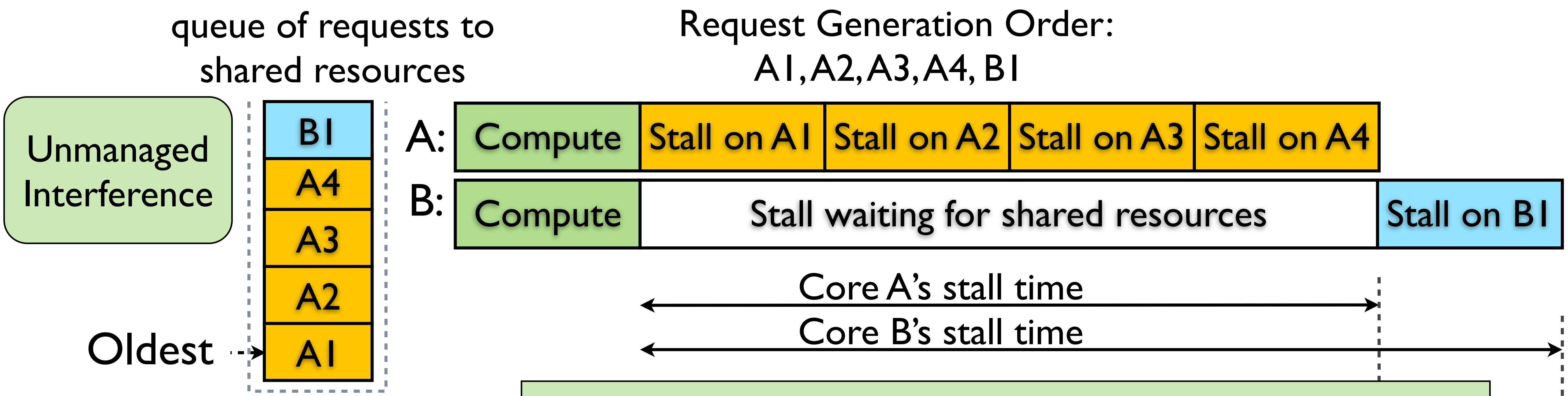
Core A's stall time

Core B's stall time

Shared Memory Resources

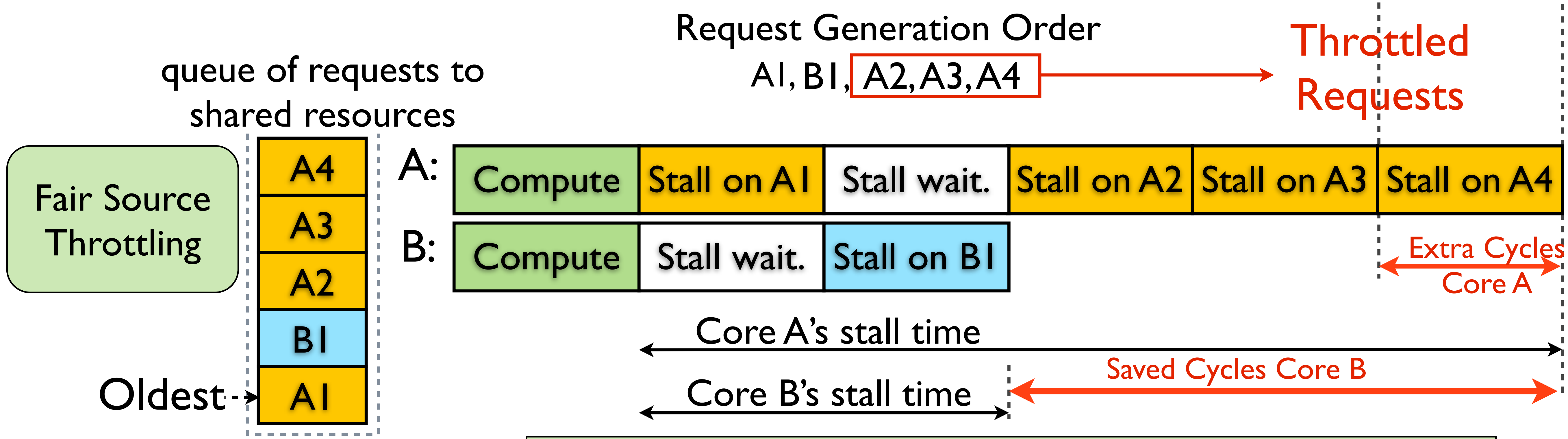


Intensive application A generates many requests and causes long stall times for less intensive application B



Shared Memory Resources

Intensive application A generates many requests and causes long stall times for less intensive application B



Shared Memory Resources

Dynamically detect application A's interference for application B and throttle down application A

Outline

- Background and Problem
- Motivation for Source Throttling
- Fairness via Source Throttling (FST)
- Evaluation
- Conclusion

Fairness via Source Throttling (FST)

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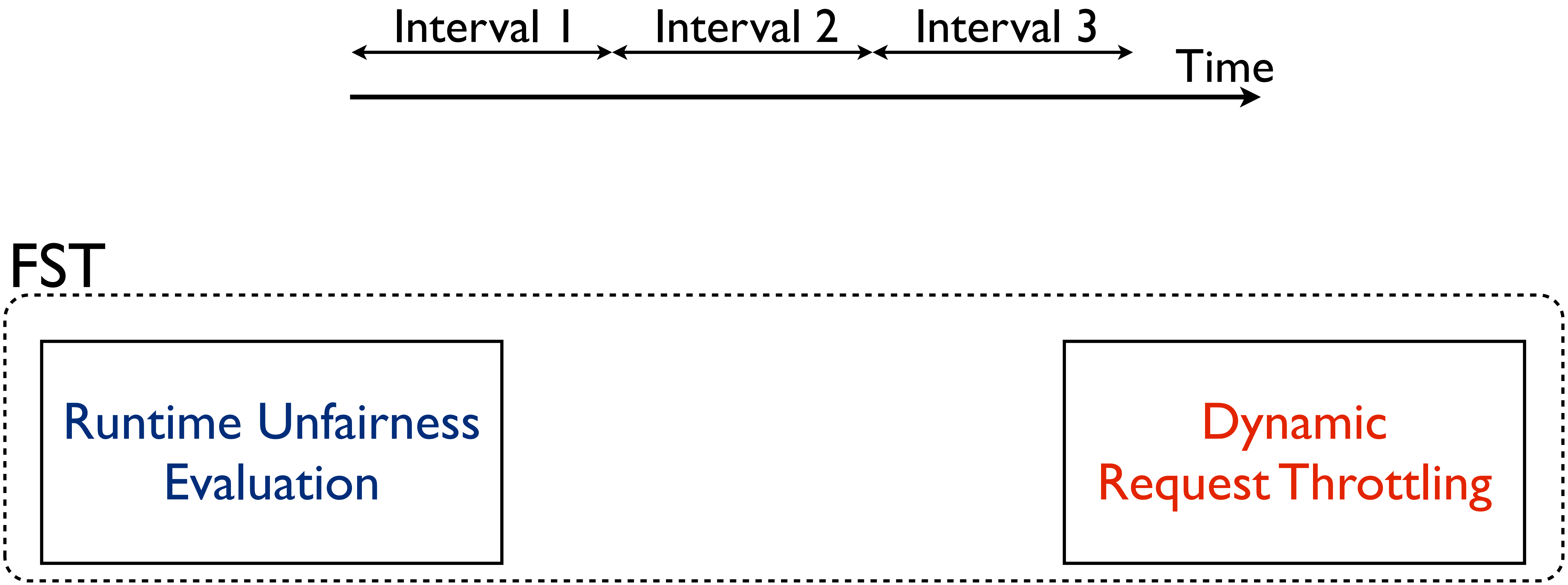
- Runtime Unfairness Evaluation
  - Dynamically estimates the unfairness in the memory system

Fairness via Source Throttling (FST)

- Runtime Unfairness Evaluation
  - Dynamically estimates the unfairness in the memory system

- Dynamic Request Throttling
  - Adjusts how aggressively each core makes requests to the shared resources

Fairness via Source Throttling (FST)



Interval 1

Interval 2

Interval 3

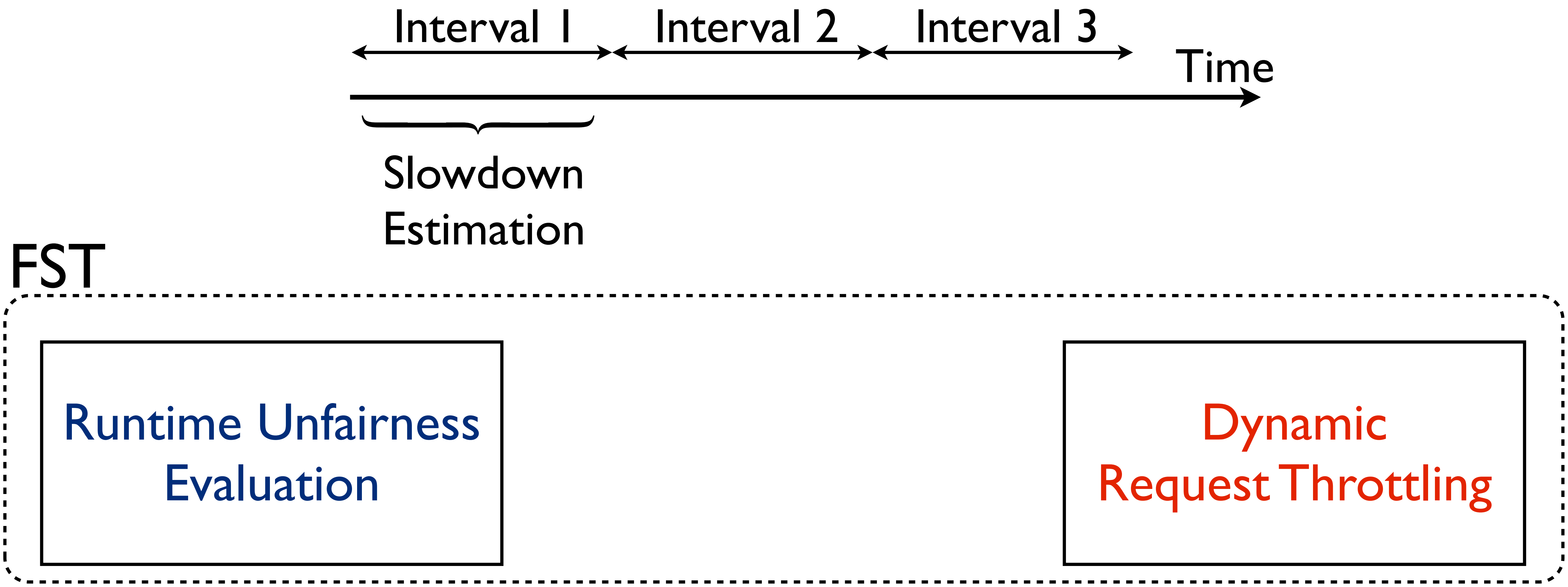
Time

FST

Runtime Unfairness Evaluation

Dynamic Request Throttling

Fairness via Source Throttling (FST)



Interval 1

Interval 2

Interval 3

Time

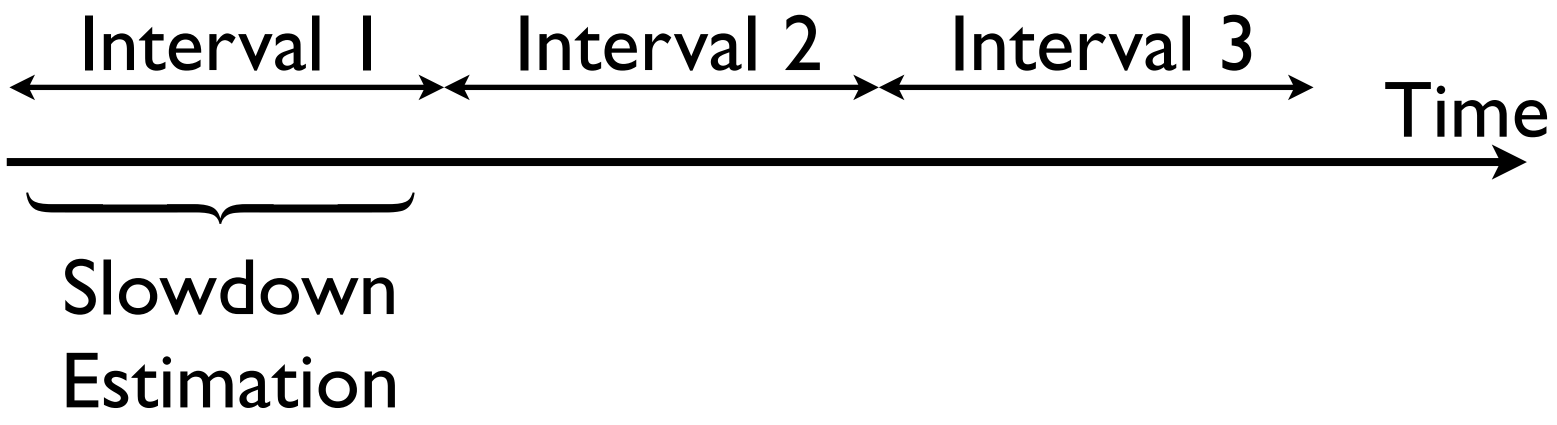
Slowdown Estimation

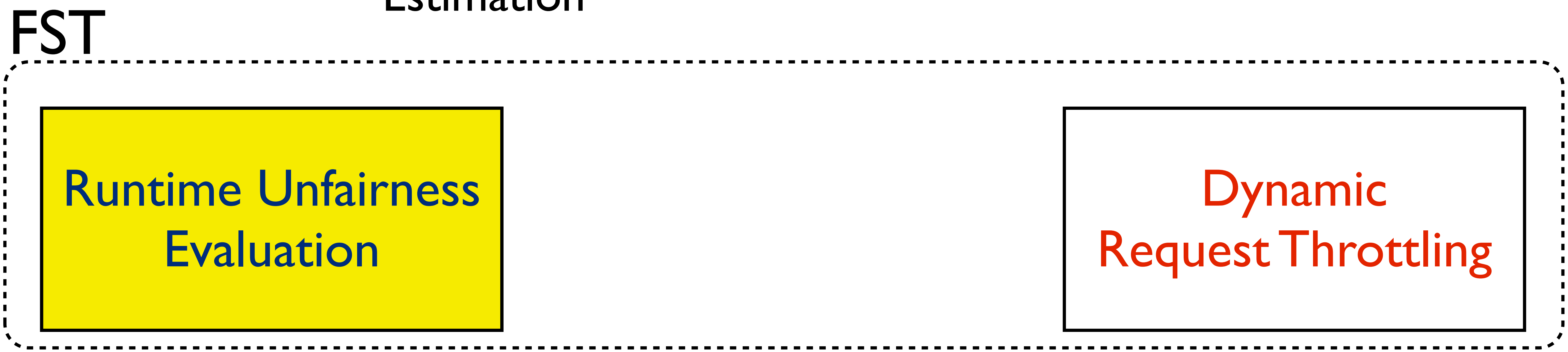
FST

Runtime Unfairness Evaluation

Dynamic Request Throttling

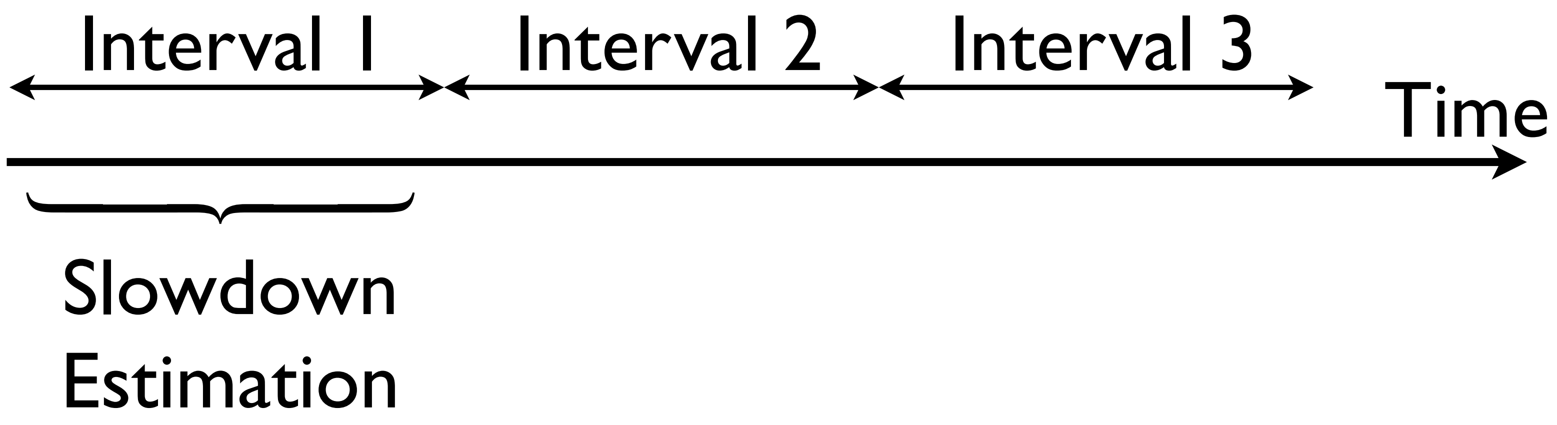
Fairness via Source Throttling (FST)

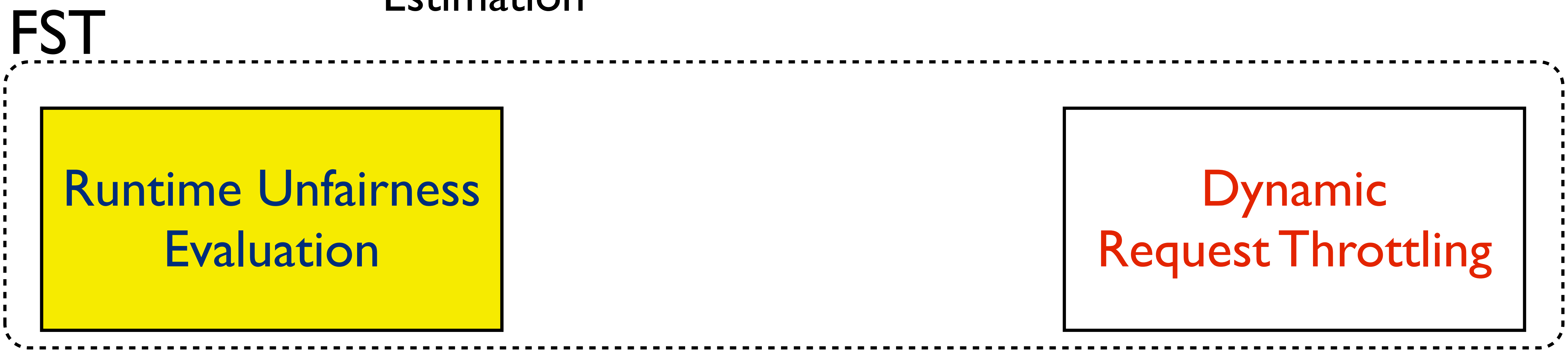




1- Estimating system unfairness

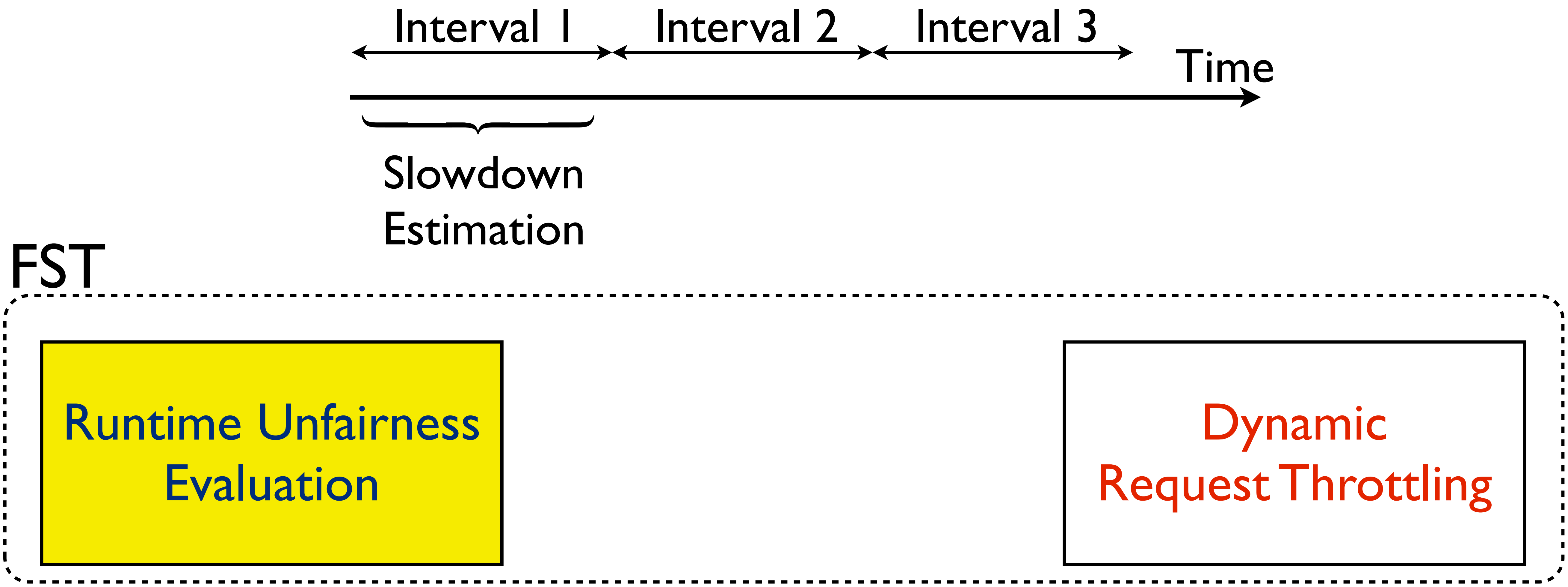
Fairness via Source Throttling (FST)





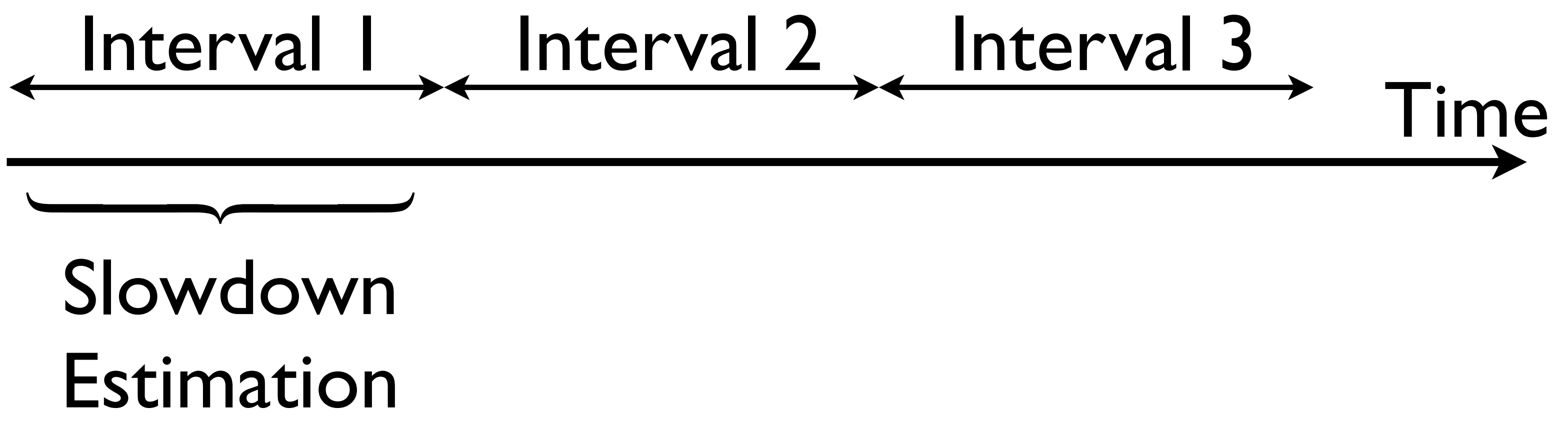
1- Estimating system unfairness
2- Find app. with the highest slowdown (App-slowest)

Fairness via Source Throttling (FST)



1- Estimating system unfairness
2- Find app. with the highest slowdown (App-slowest)
3- Find app. causing most interference for App-slowest (App-interfering)

Fairness via Source Throttling (FST)



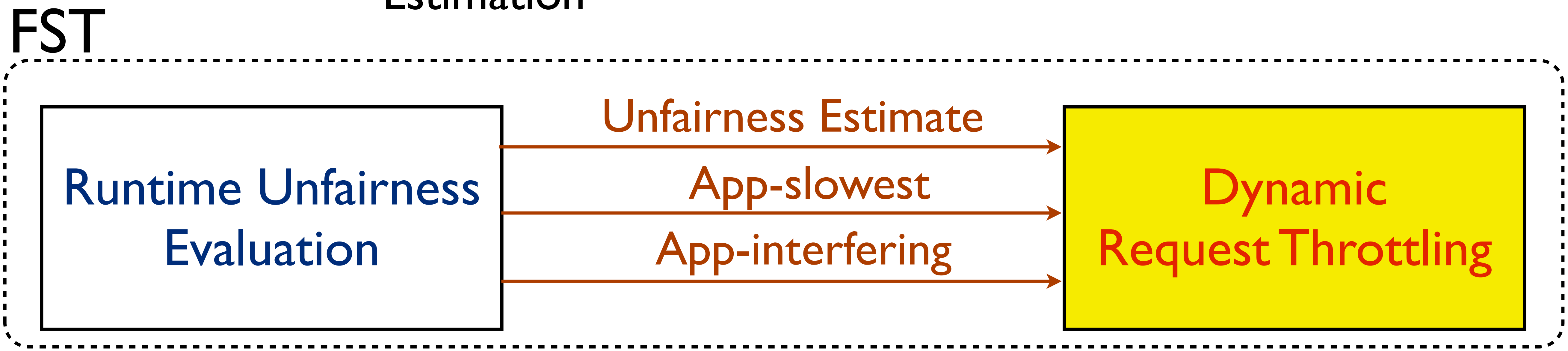
Interval 1

Interval 2

Interval 3

Time

Slowdown Estimation



FST

Runtime Unfairness Evaluation

Unfairness Estimate

App-slowest

App-interfering

Dynamic Request Throttling

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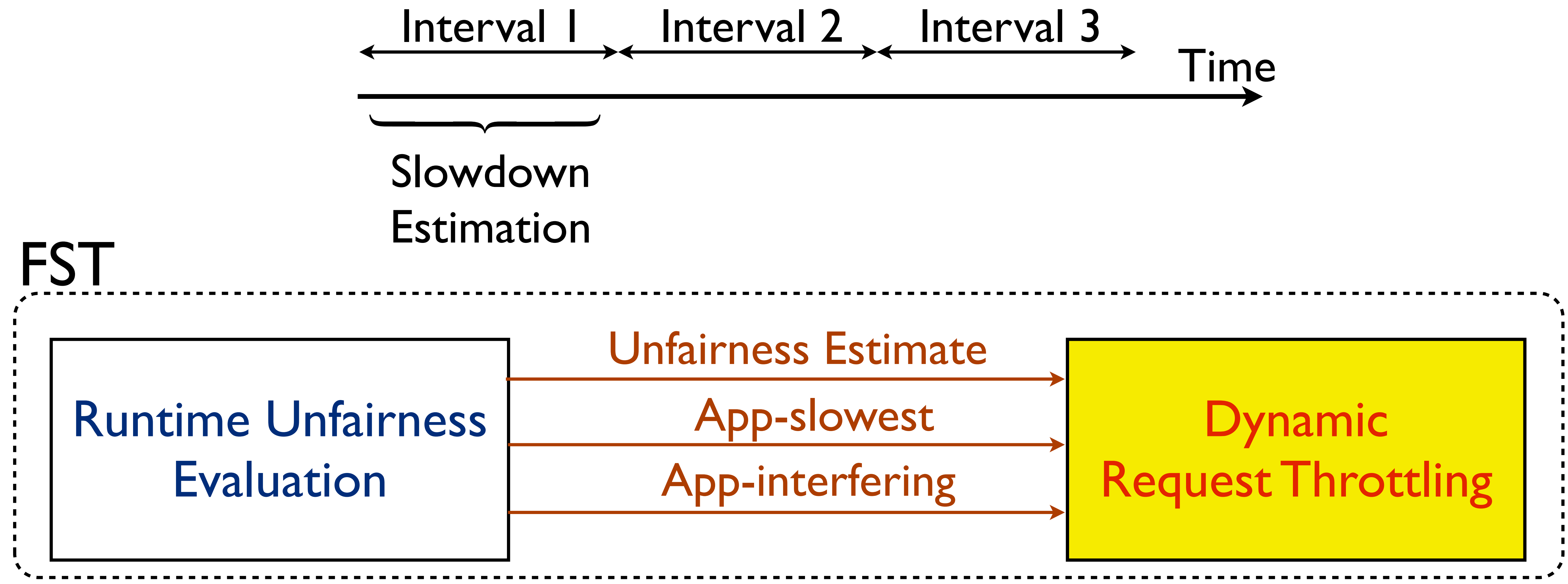
Fairness via Source Throttling (FST)



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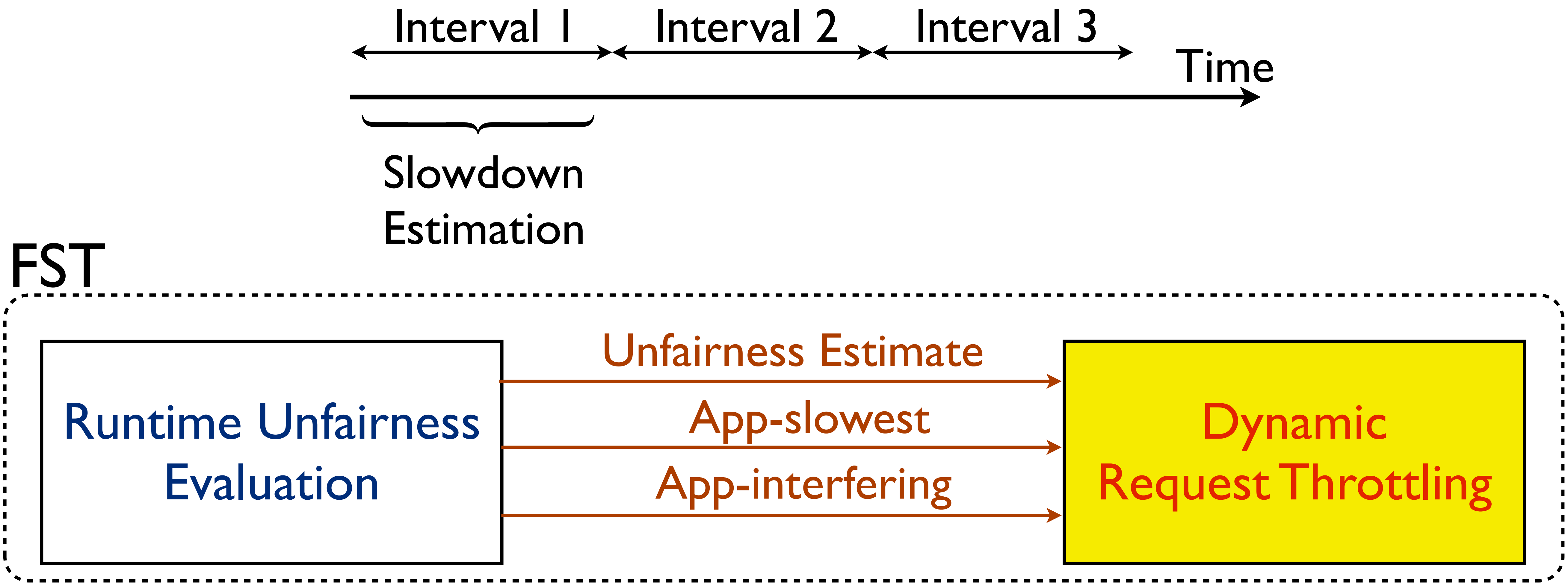
```
if (Unfairness Estimate >Target)
{
```

Fairness via Source Throttling (FST)



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 1-Throttle down App-interfering
```

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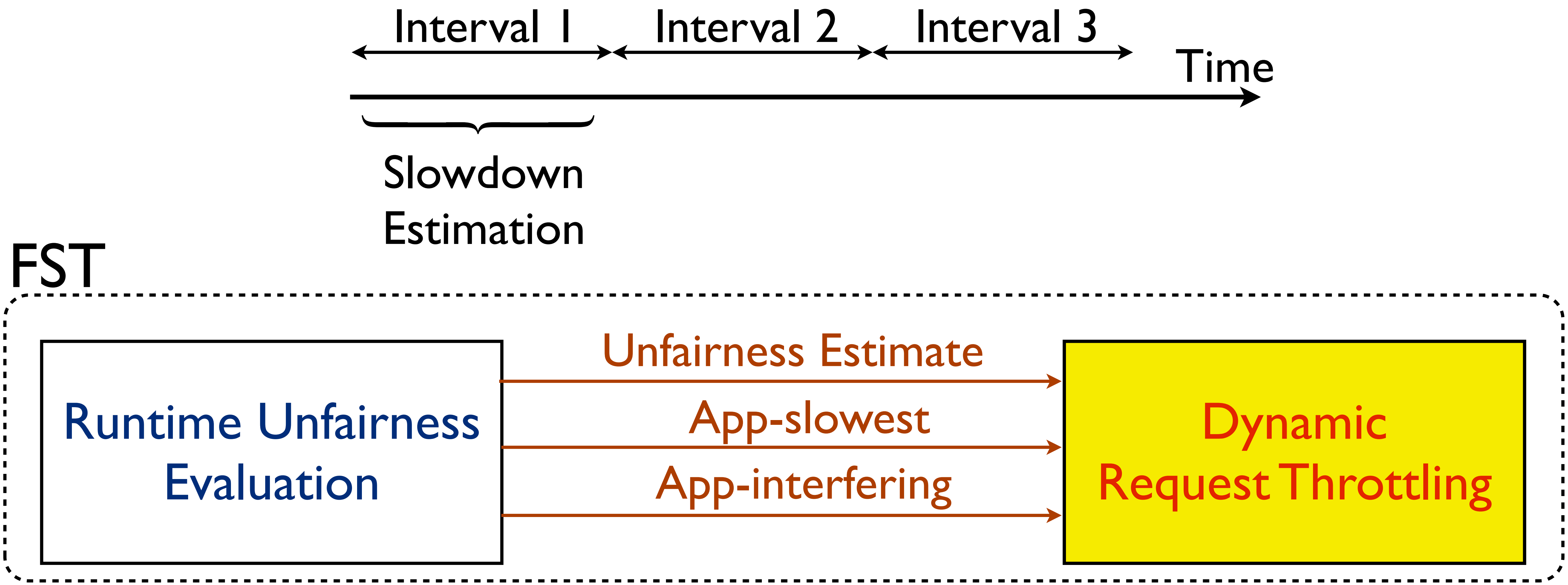

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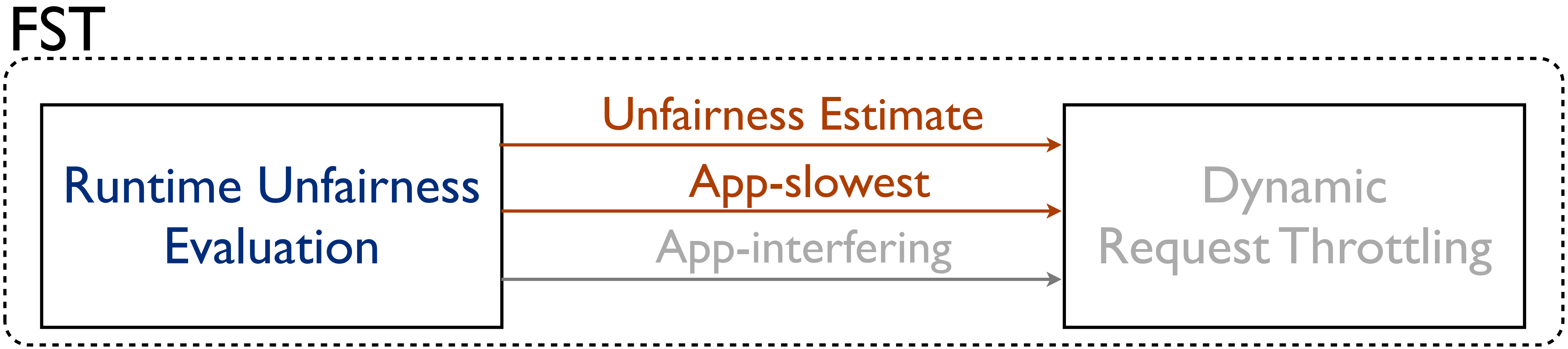

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Estimating System Unfairness

- Unfairness = $\dfrac{\text{Max}\{\text{Slowdown } i\} \text{ over all applications } i}{\text{Min}\{\text{Slowdown } i\} \text{ over all applications } i}$

- Slowdown of application *i* = $\dfrac{T_i^{\text{Shared}}}{T_i^{\text{Alone}}}$

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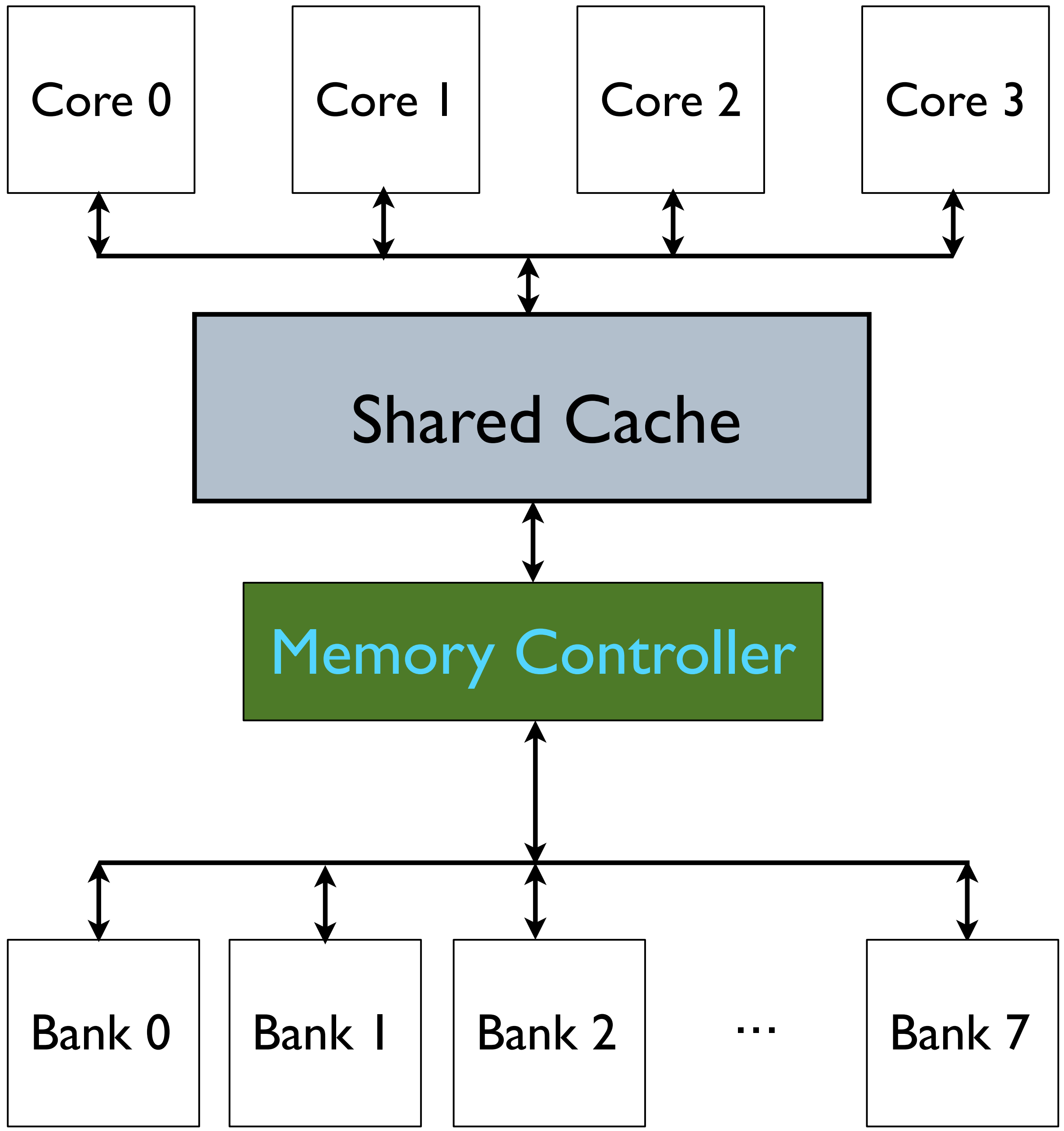
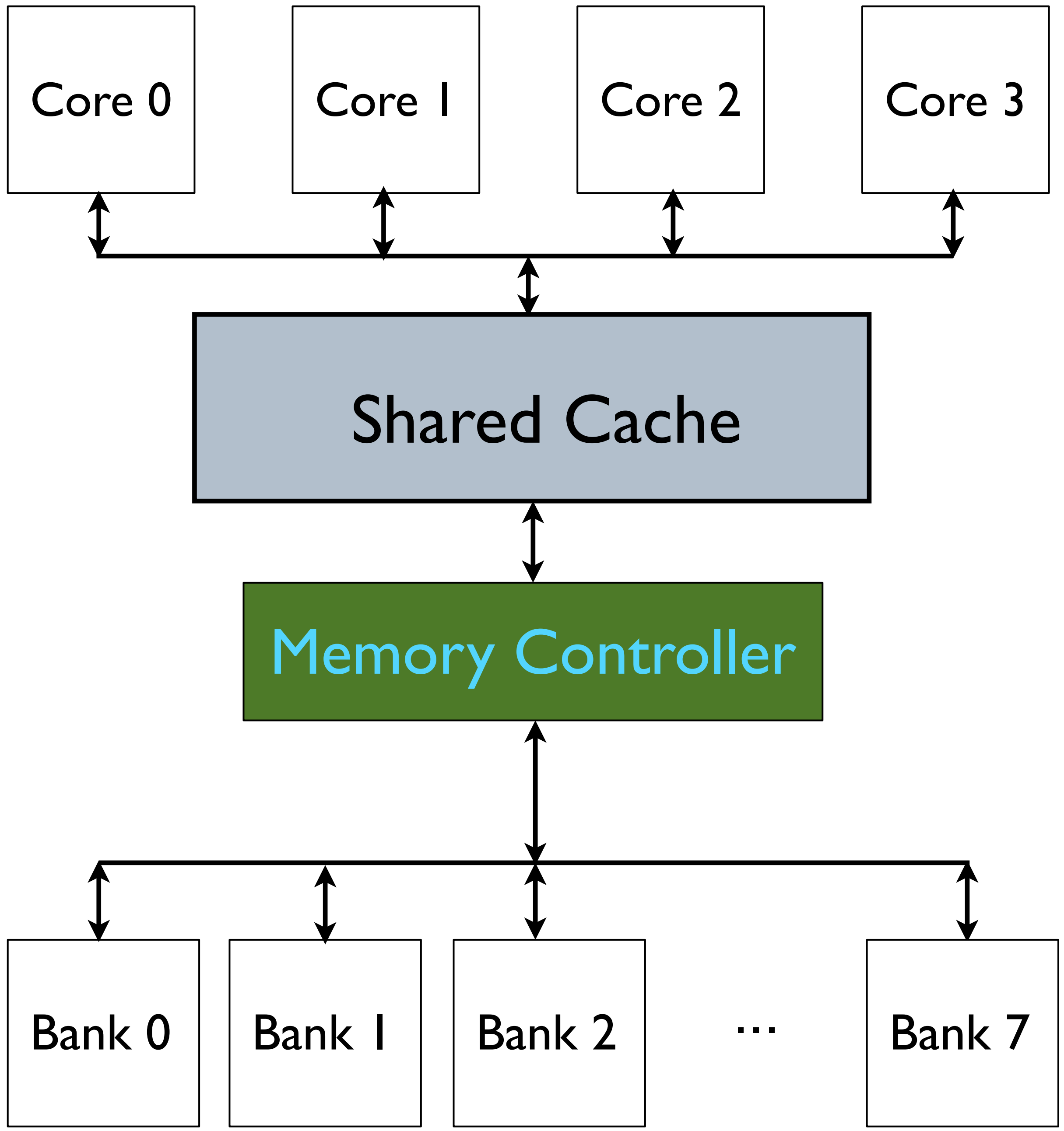
- $T_i^{\text{Alone}} = T_i^{\text{Shared}} - T_i^{\text{Excess}}$

Tracking Inter-Core Interference

Tracking Inter-Core Interference

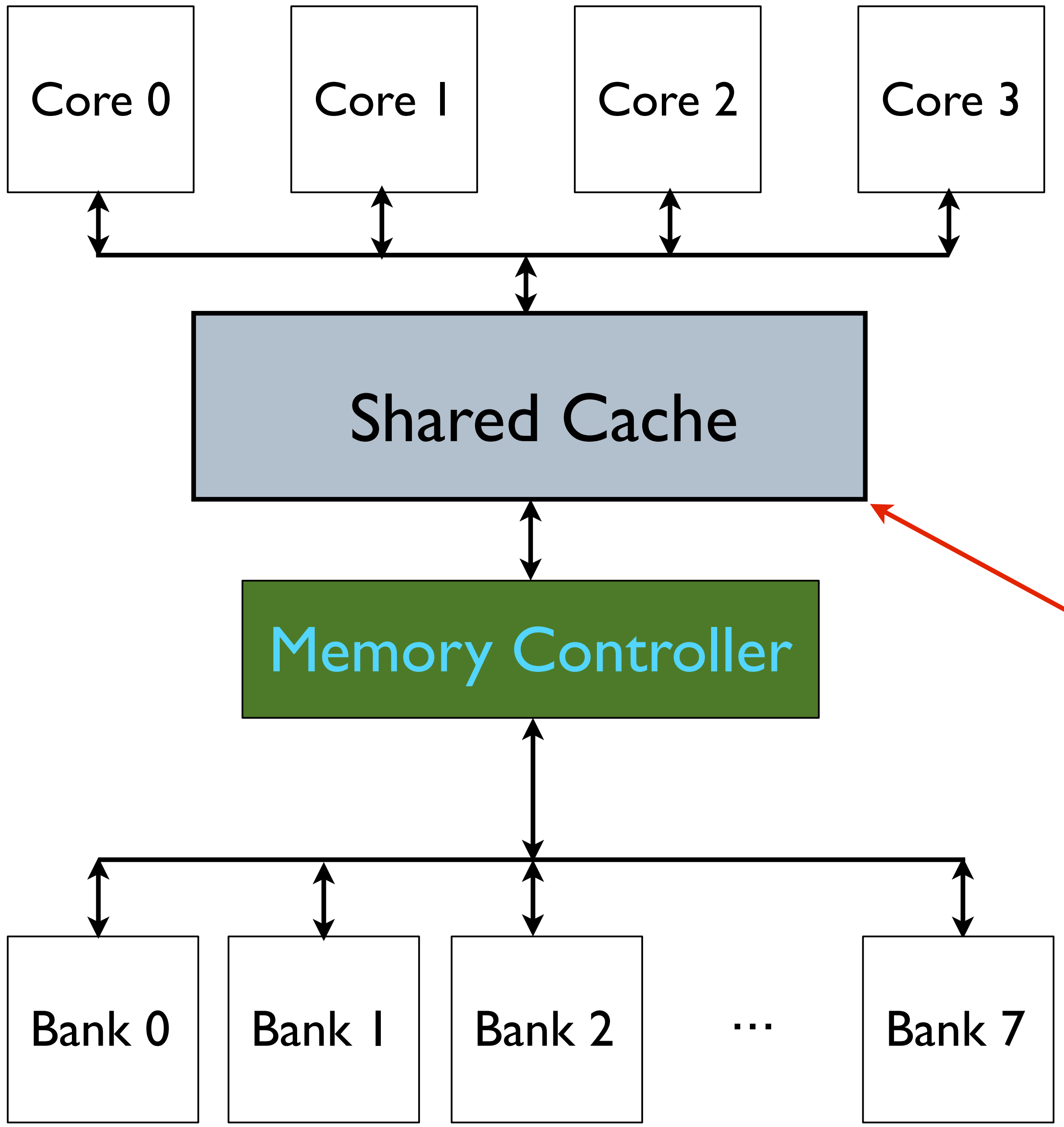


Tracking Inter-Core Interference



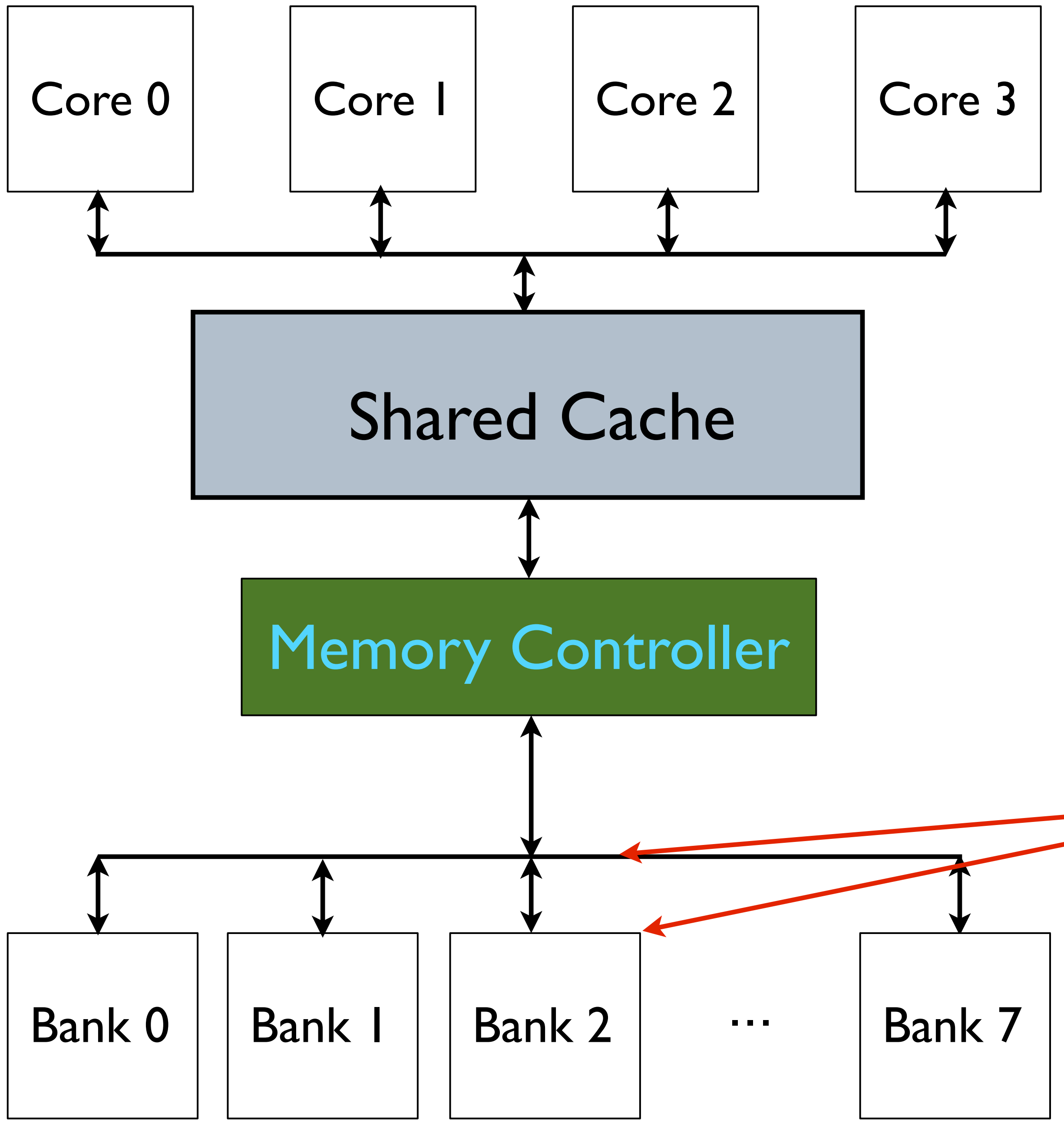
Three interference sources:

Tracking Inter-Core Interference



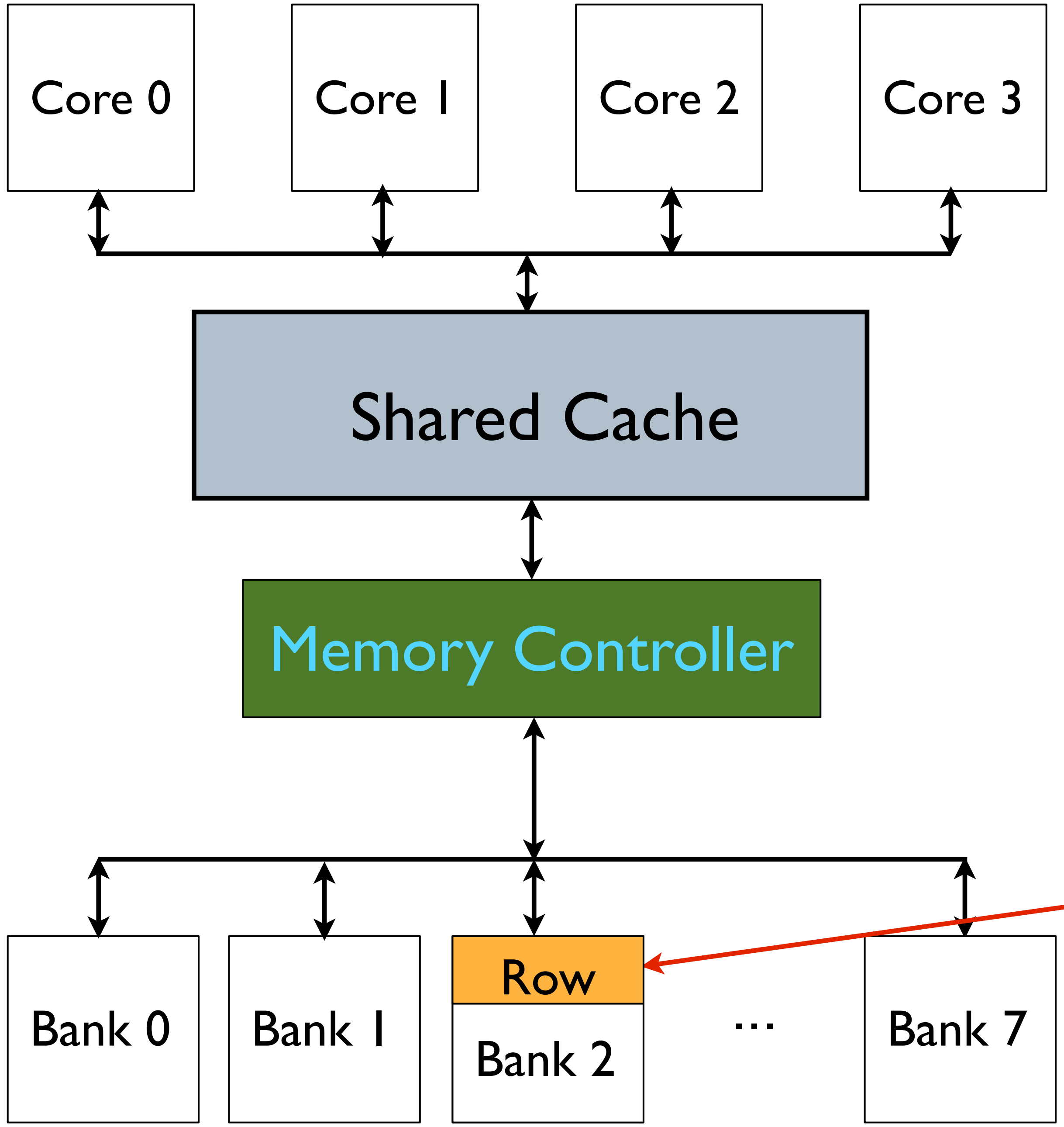
Three interference sources:
1. Shared Cache

Tracking Inter-Core Interference



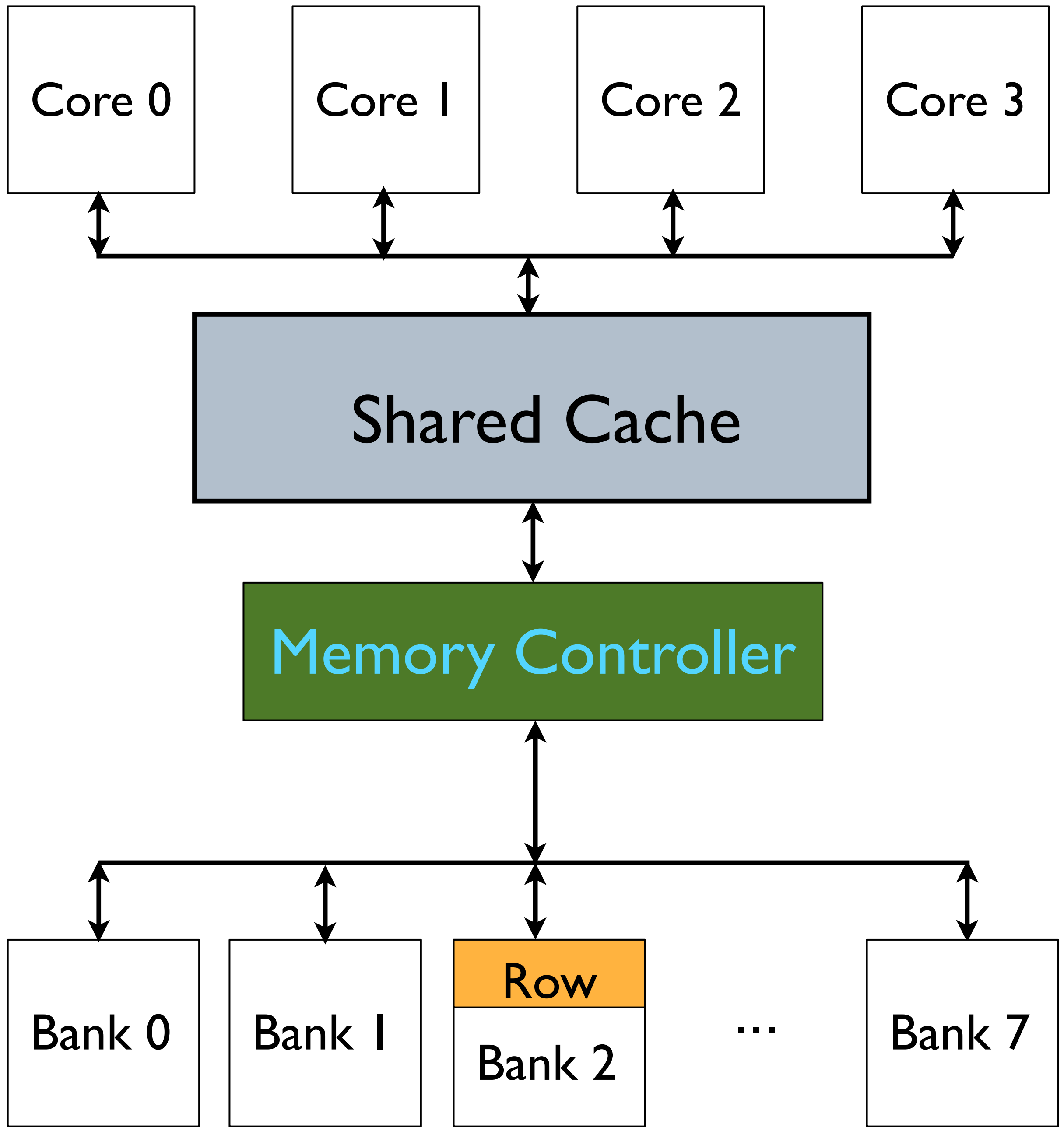
Three interference sources:
1. Shared Cache
2. DRAM bus and bank

Tracking Inter-Core Interference



Three interference sources:
1. Shared Cache
2. DRAM bus and bank
3. DRAM row-buffers

Tracking Inter-Core Interference



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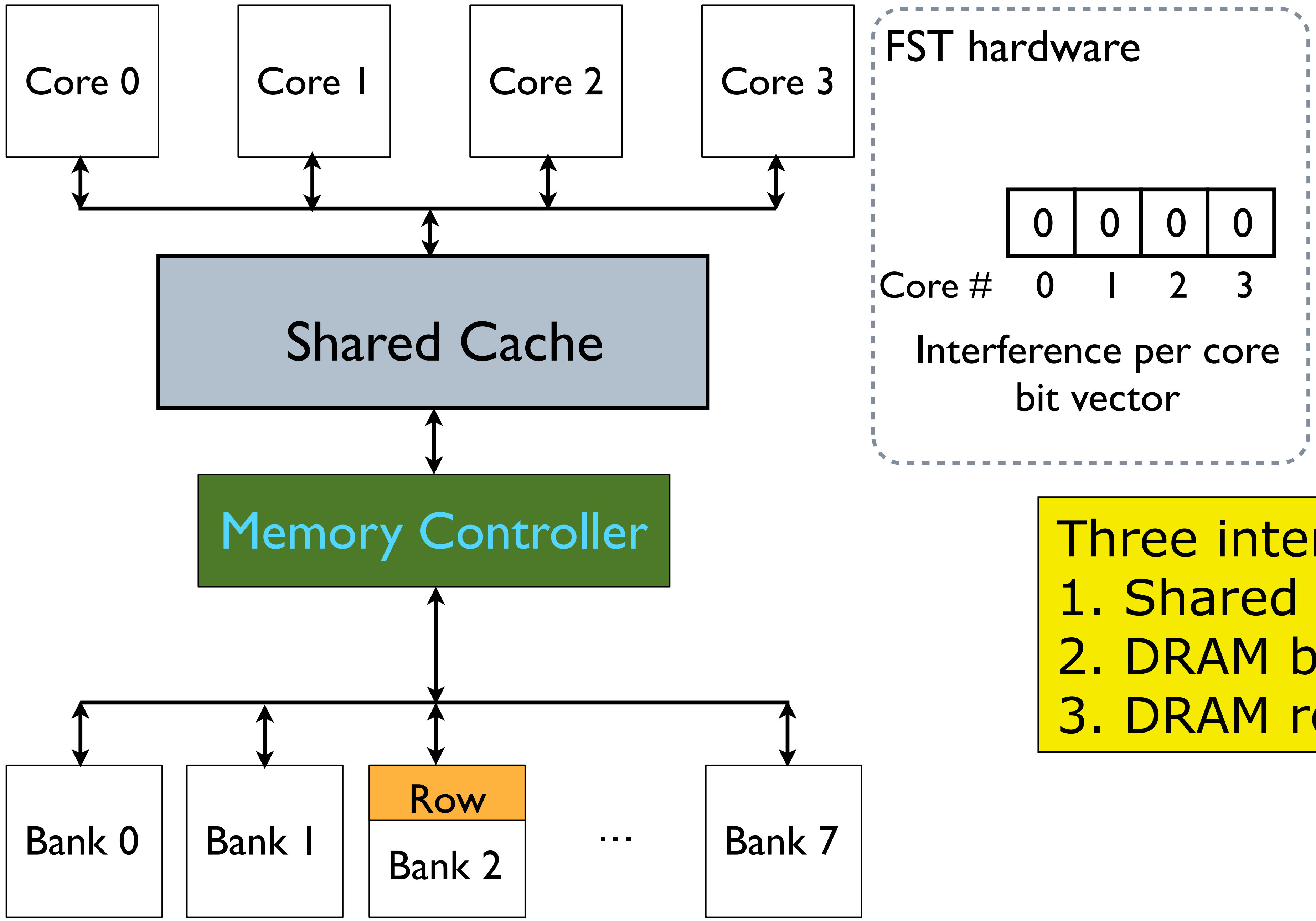

Core #	0	1	2	3
	0	0	0	0

Three interference sources:
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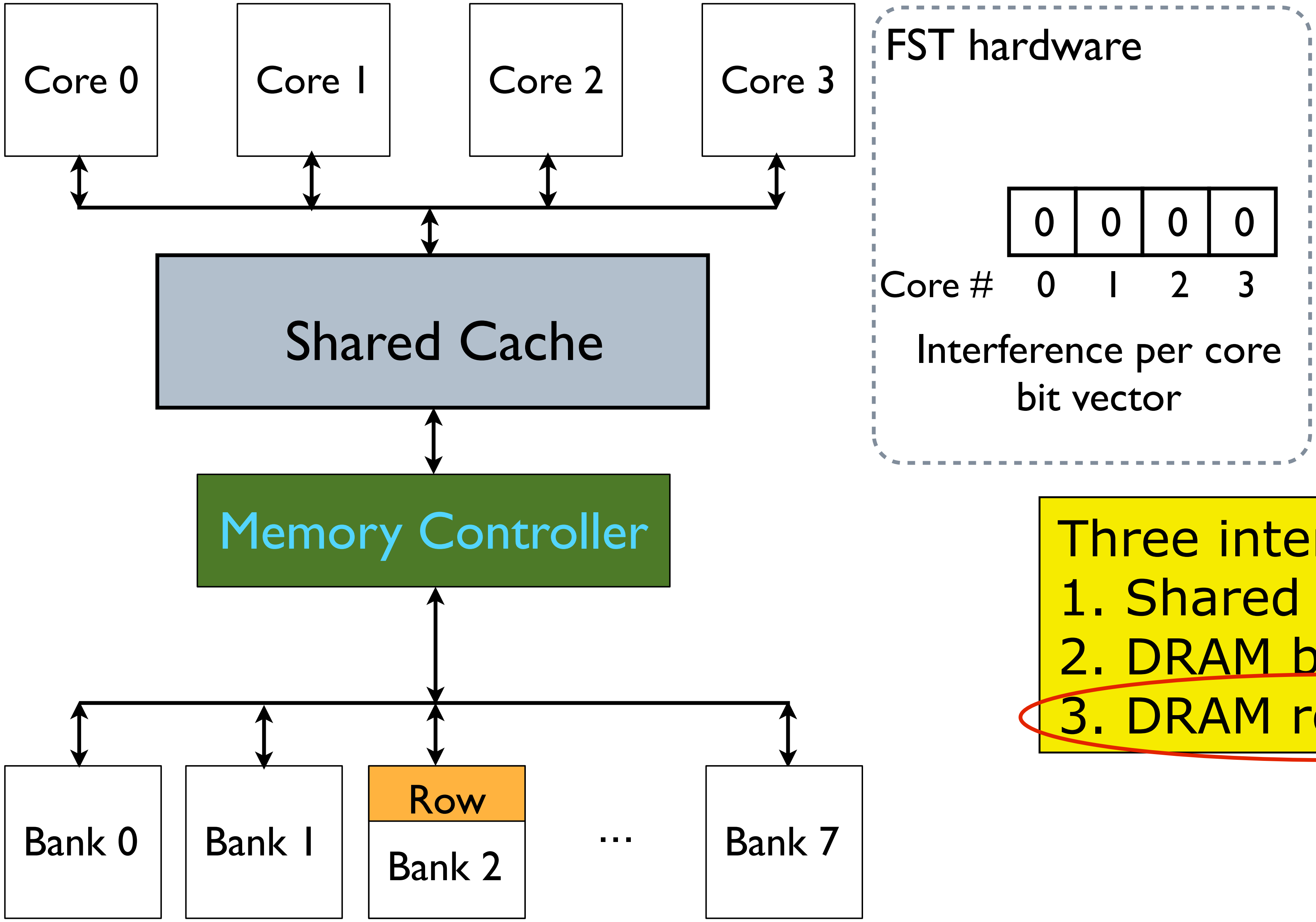
Tracking Inter-Core Interference



Core #	0	1	2	3
	0	0	0	0

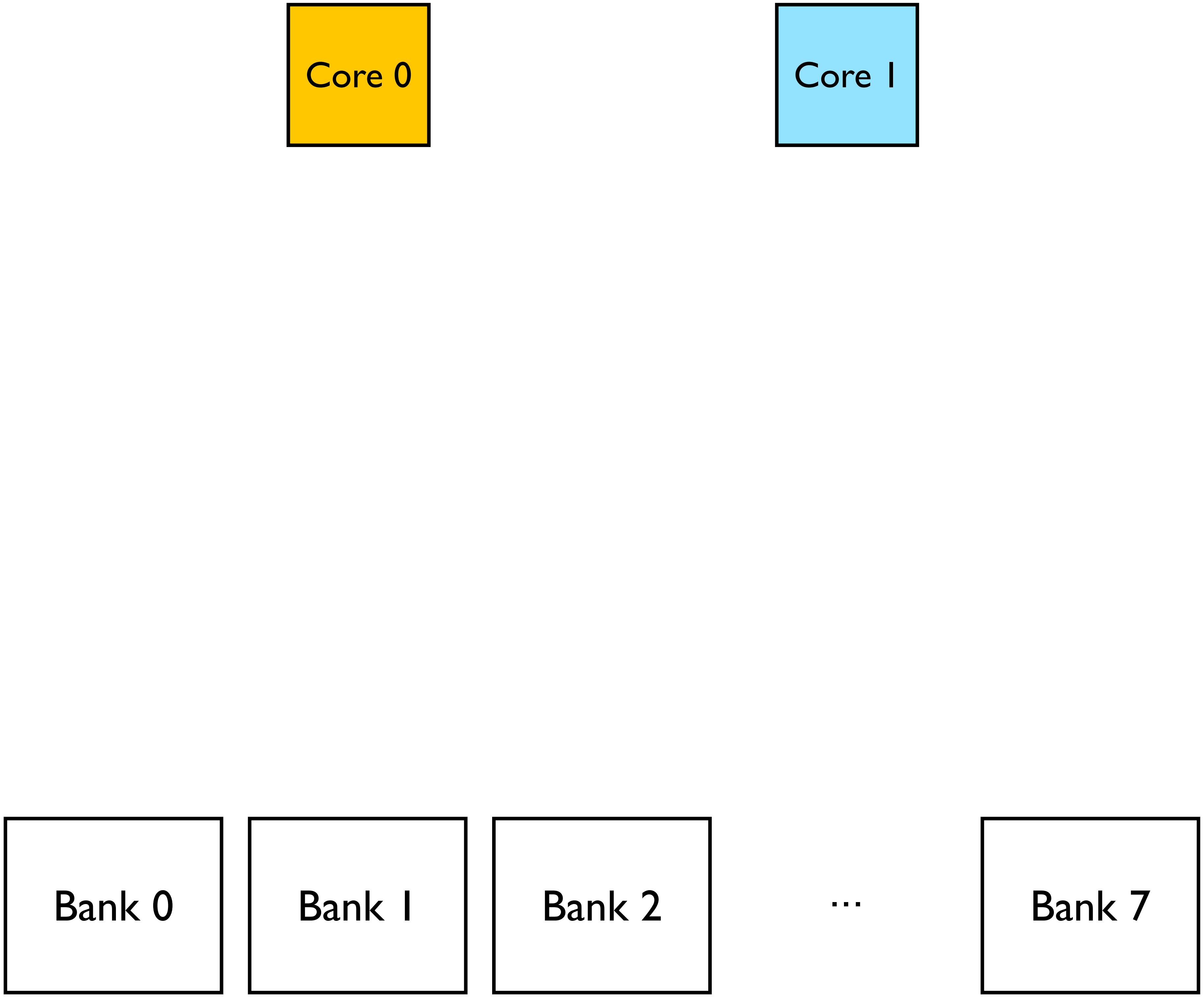
Three interference sources:
1. Shared Cache
2. DRAM bus and bank
3. DRAM row-buffers

Tracking DRAM Row-Buffer Interference

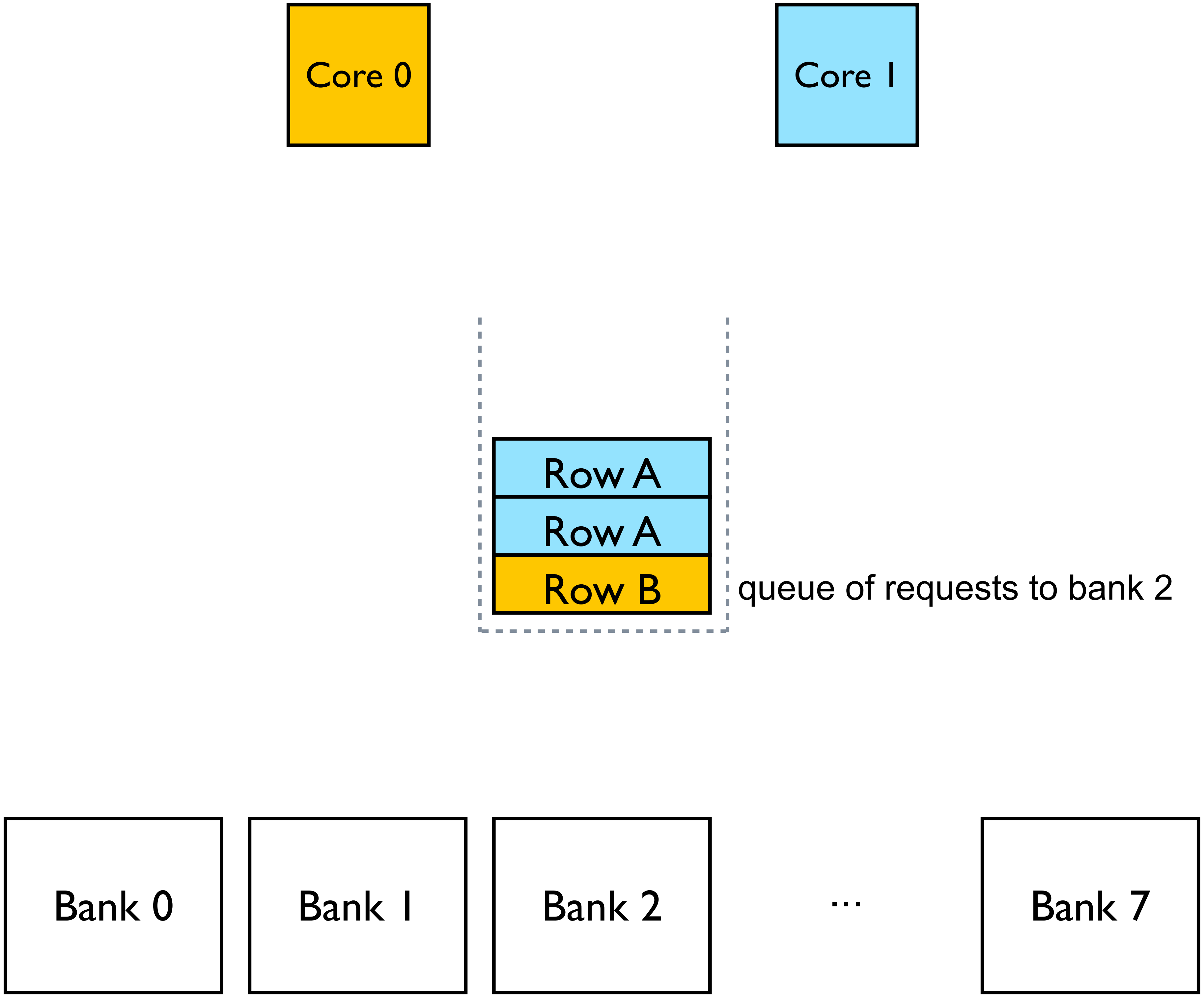
Core 0

Core 1

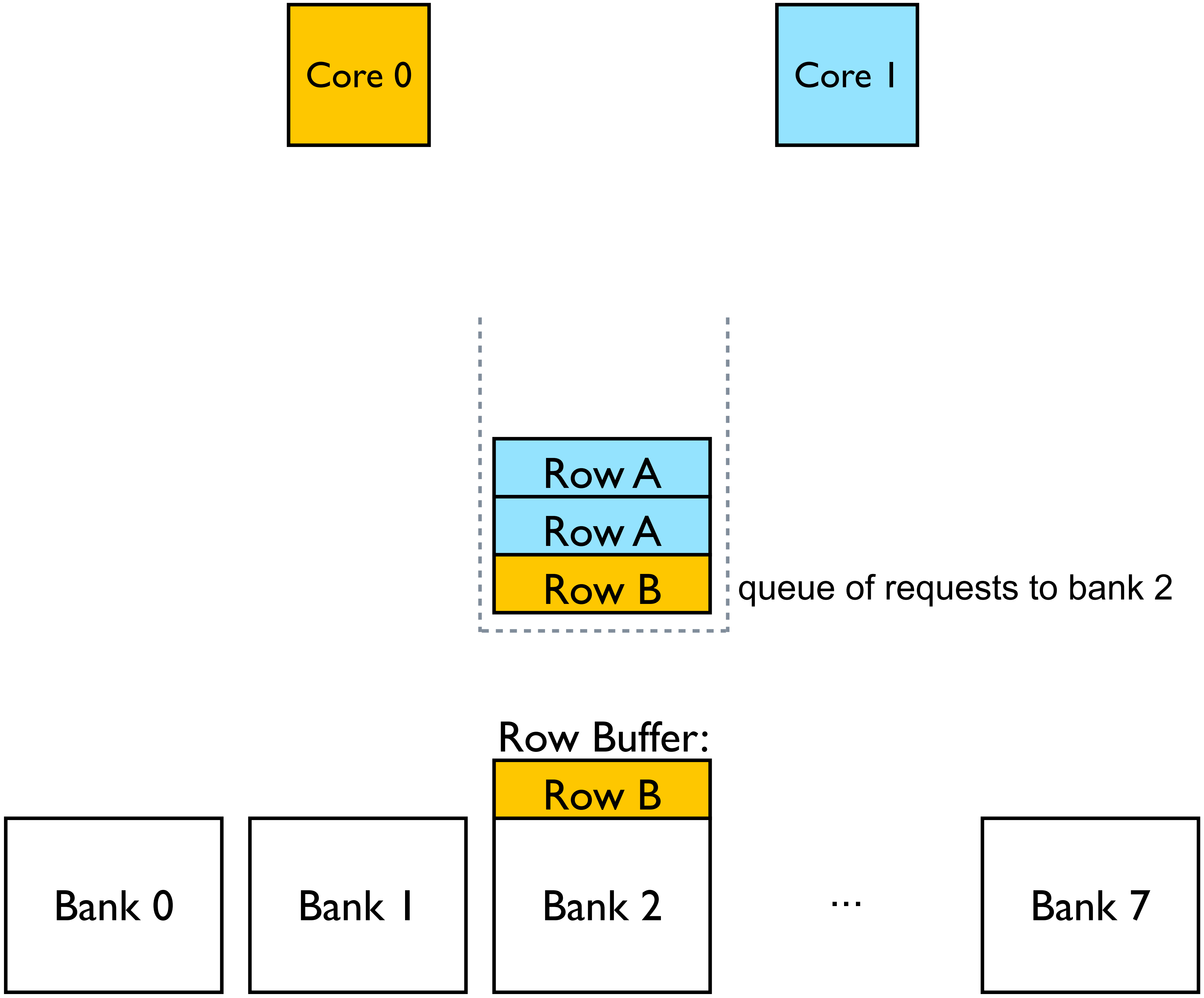
Tracking DRAM Row-Buffer Interference



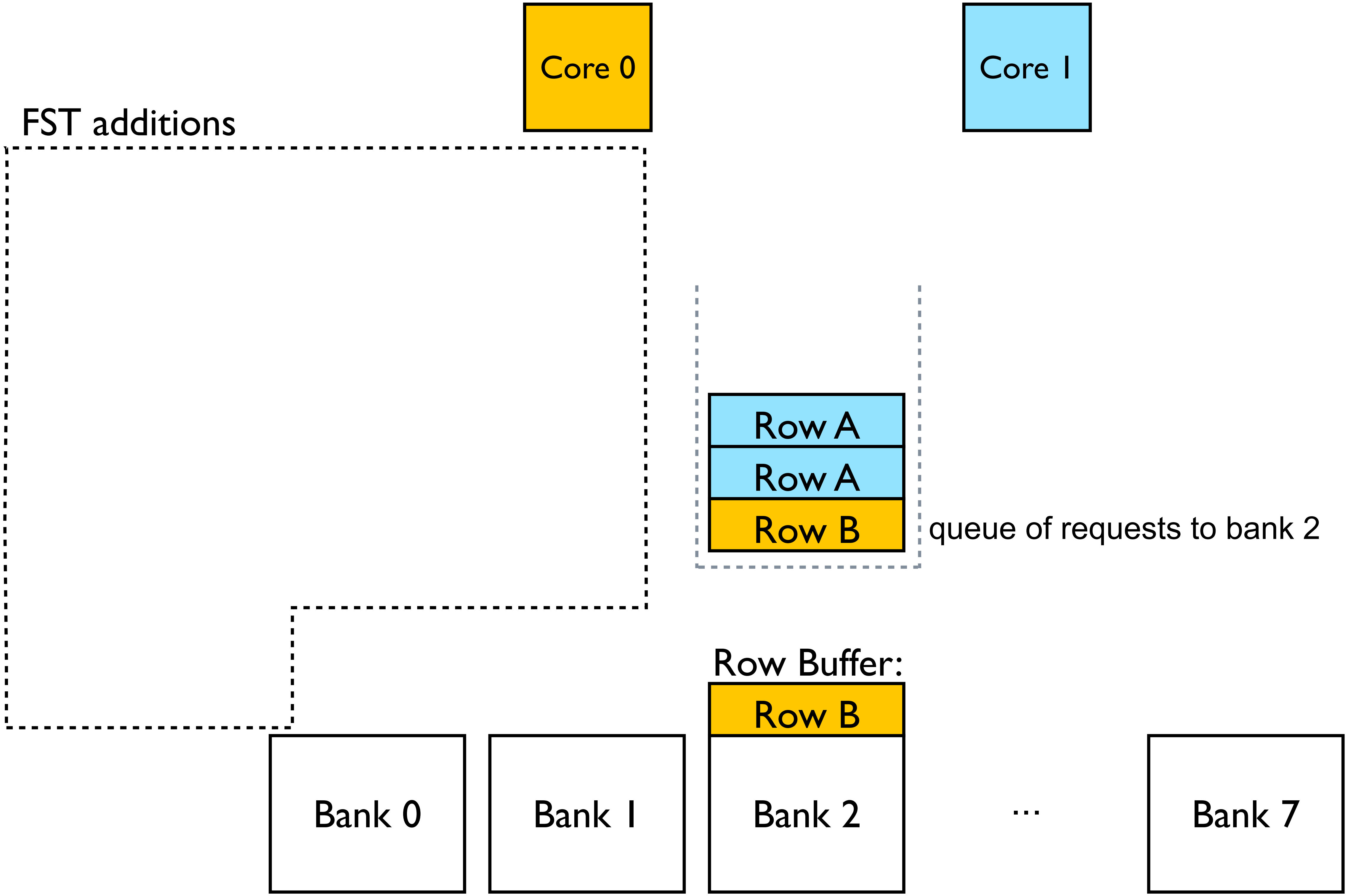
Tracking DRAM Row-Buffer Interference



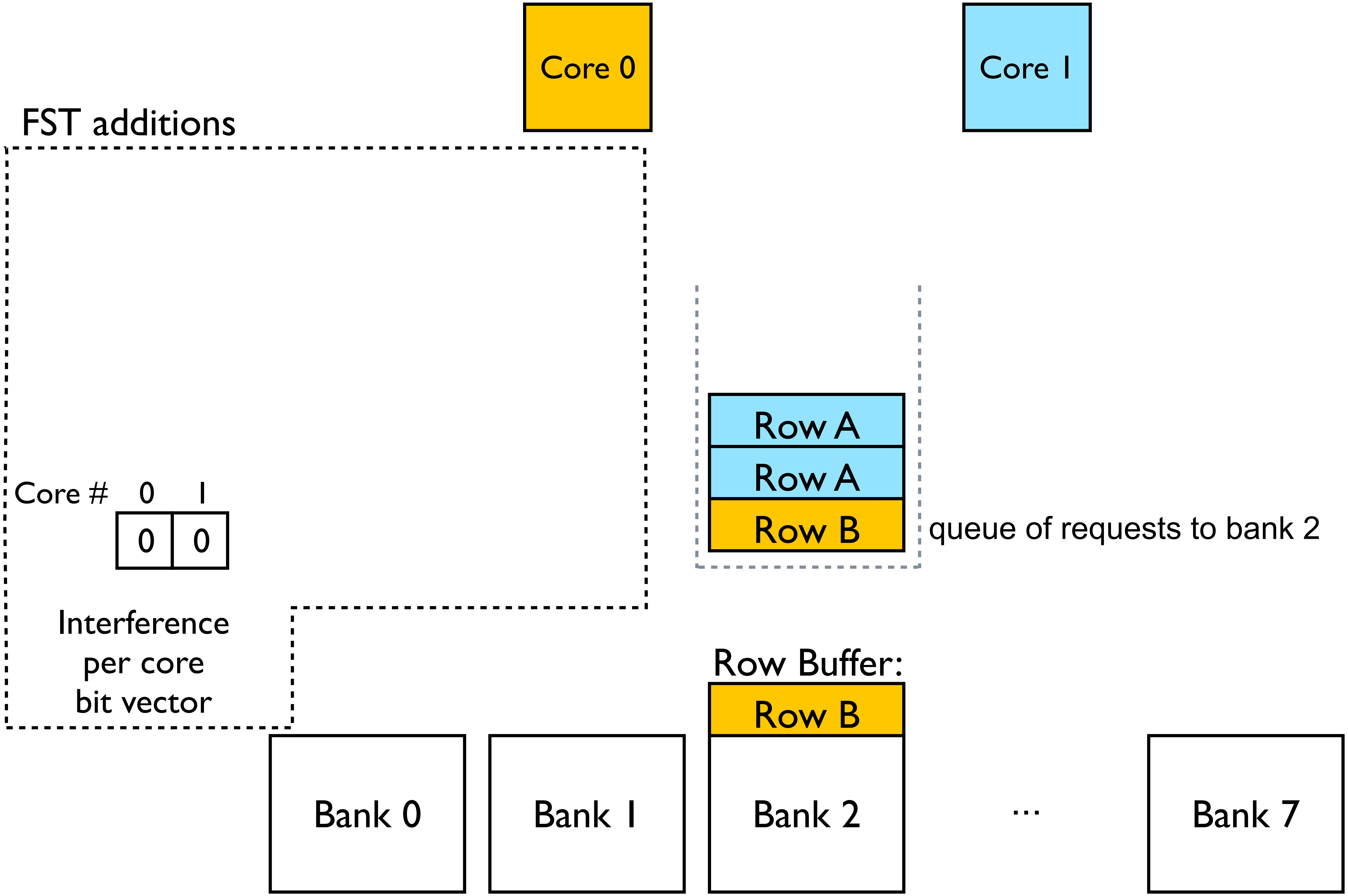
Tracking DRAM Row-Buffer Interference



Tracking DRAM Row-Buffer Interference



Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Core # 0 1

0	1
0	0

Interference
per core
bit vector

Row A

Row A

Row B

queue of requests to bank 2

Row Buffer:

Row B

Bank 0

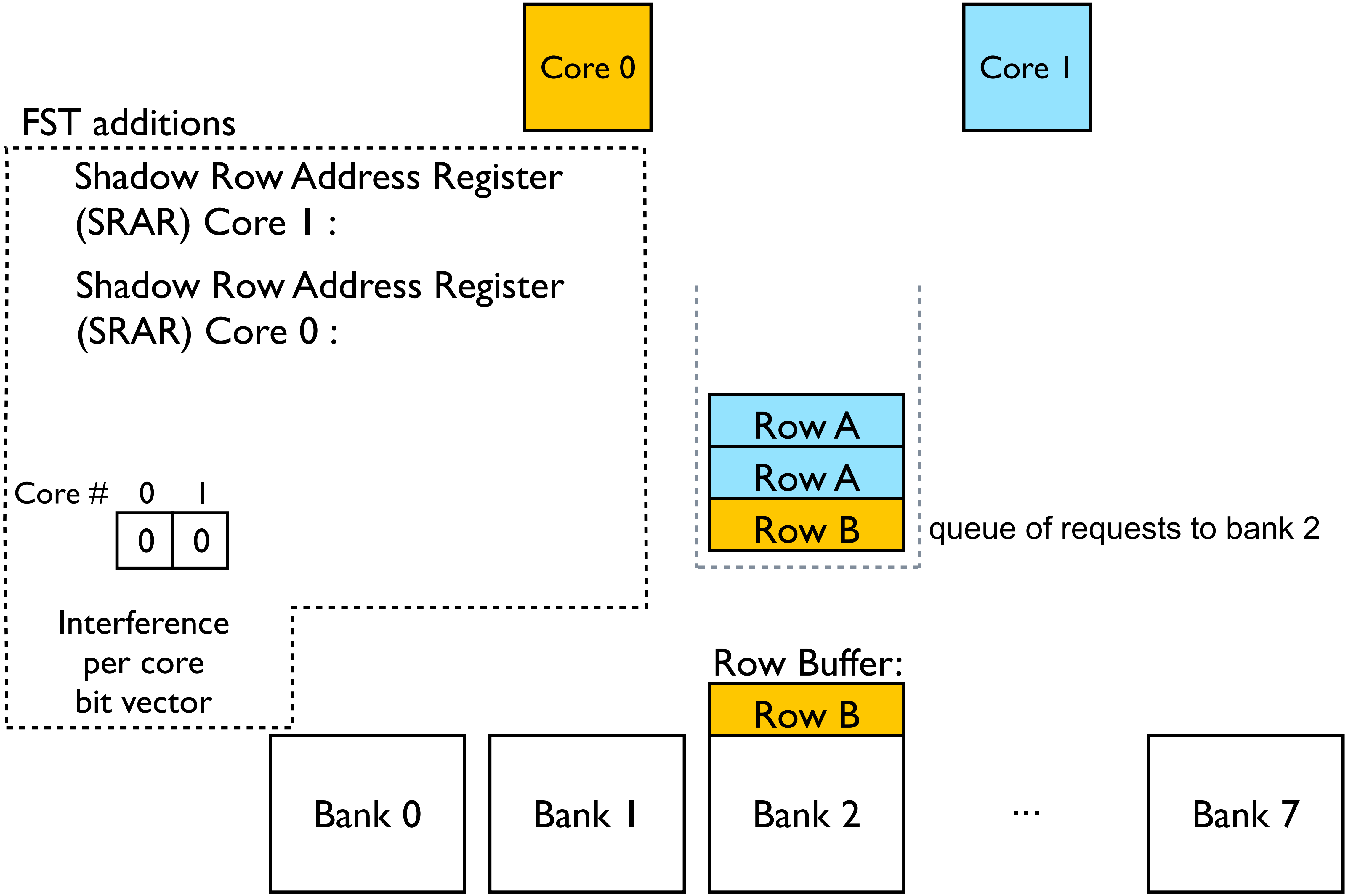
Bank 1

Bank 2

...

Bank 7

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 :

Shadow Row Address Register (SRAR) Core 0 :

Core #	0	1
	0	0

Interference per core bit vector

Row A

Row A

Row B

queue of requests to bank 2

Row Buffer:

Row B

Bank 0

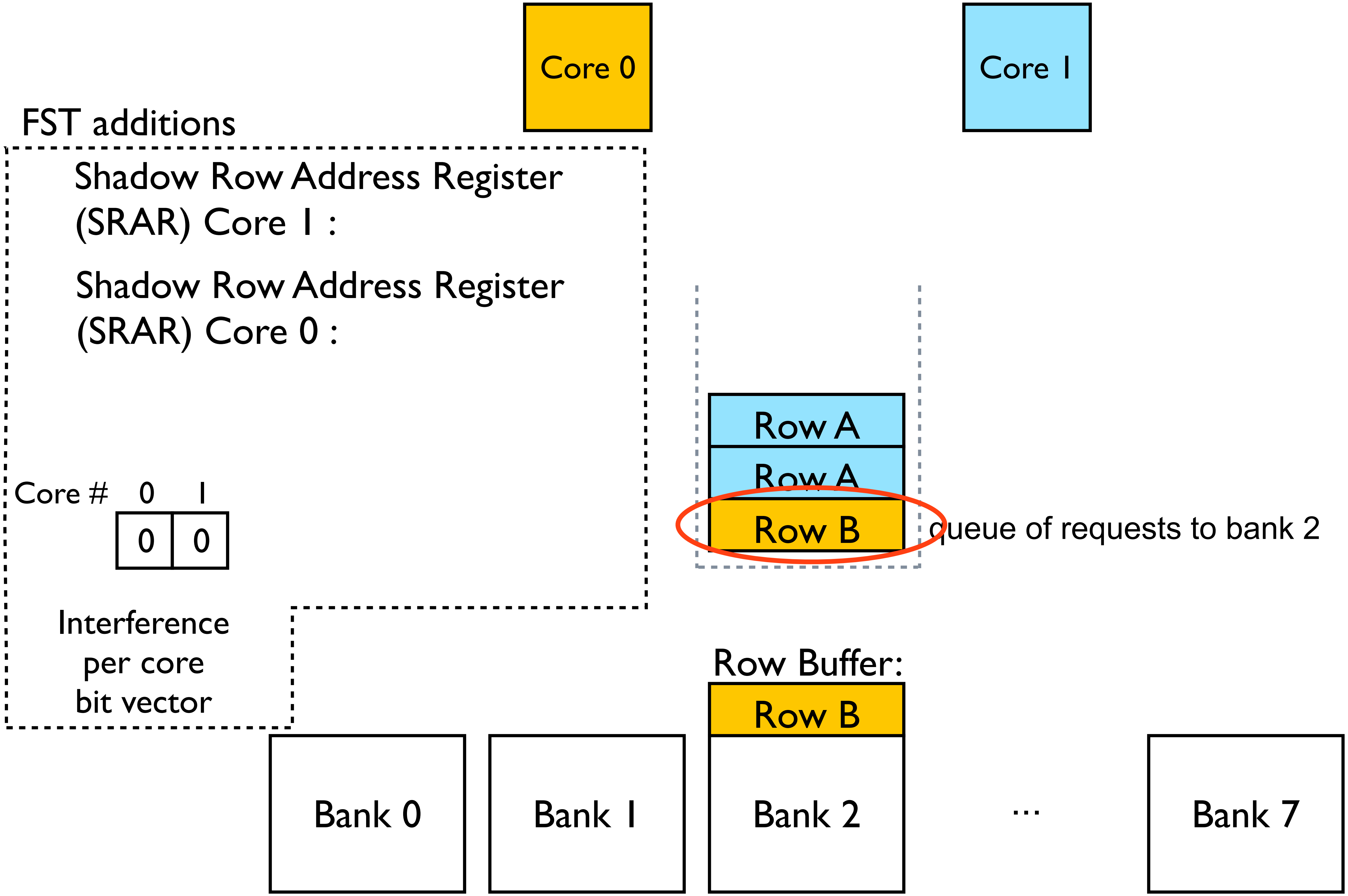
Bank 1

Bank 2

…

Bank 7

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 :

Shadow Row Address Register (SRAR) Core 0 :

Core #	0	1
	0	0

Interference per core bit vector

Row A

Row A

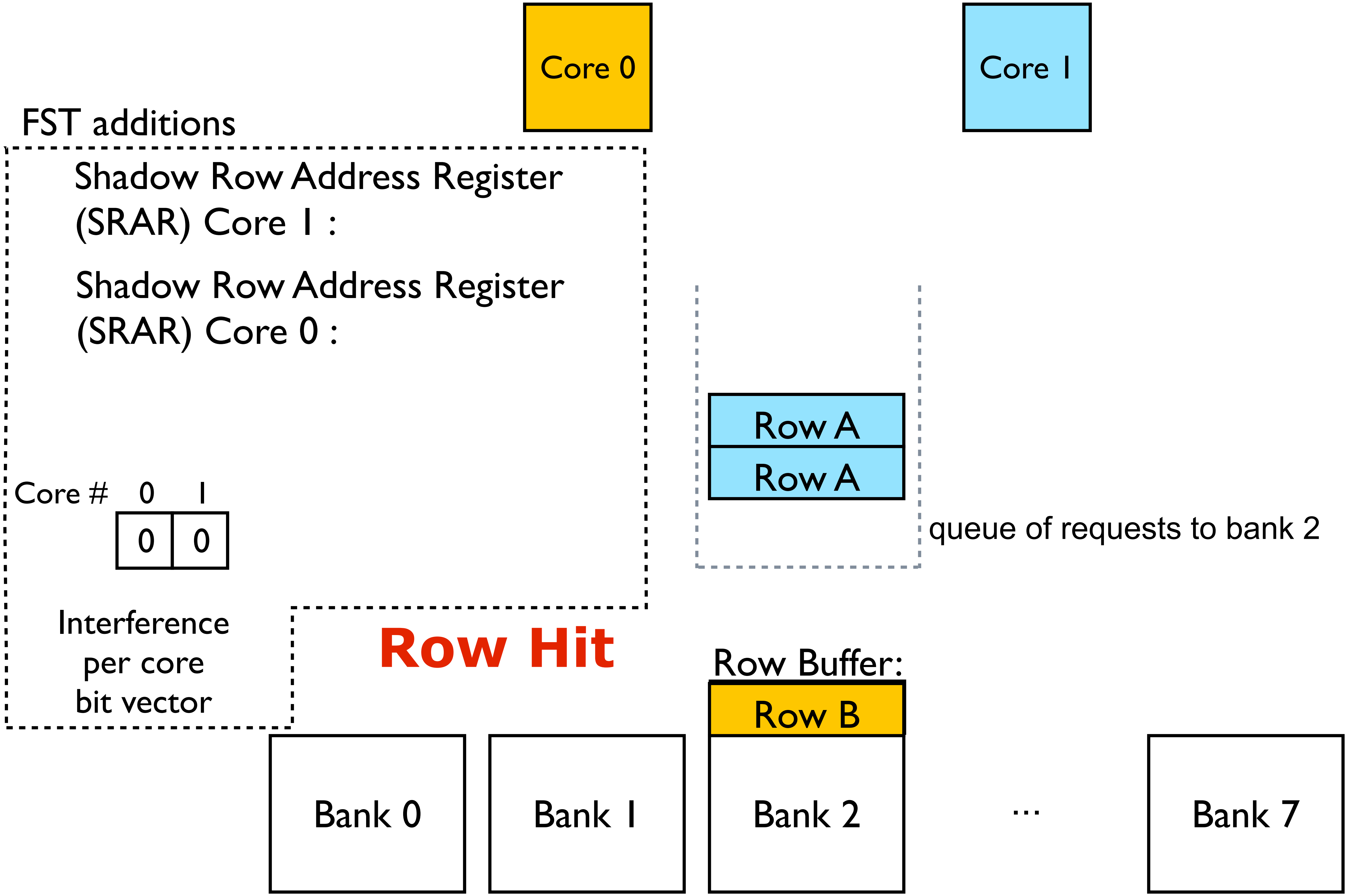
Row B

queue of requests to bank 2

Row Buffer:

Row B

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 :

Shadow Row Address Register (SRAR) Core 0 :

Core #	0	1
	0	0

Interference per core bit vector

Row Hit

Row A

Row A

queue of requests to bank 2

Row Buffer:

Row B

Bank 0

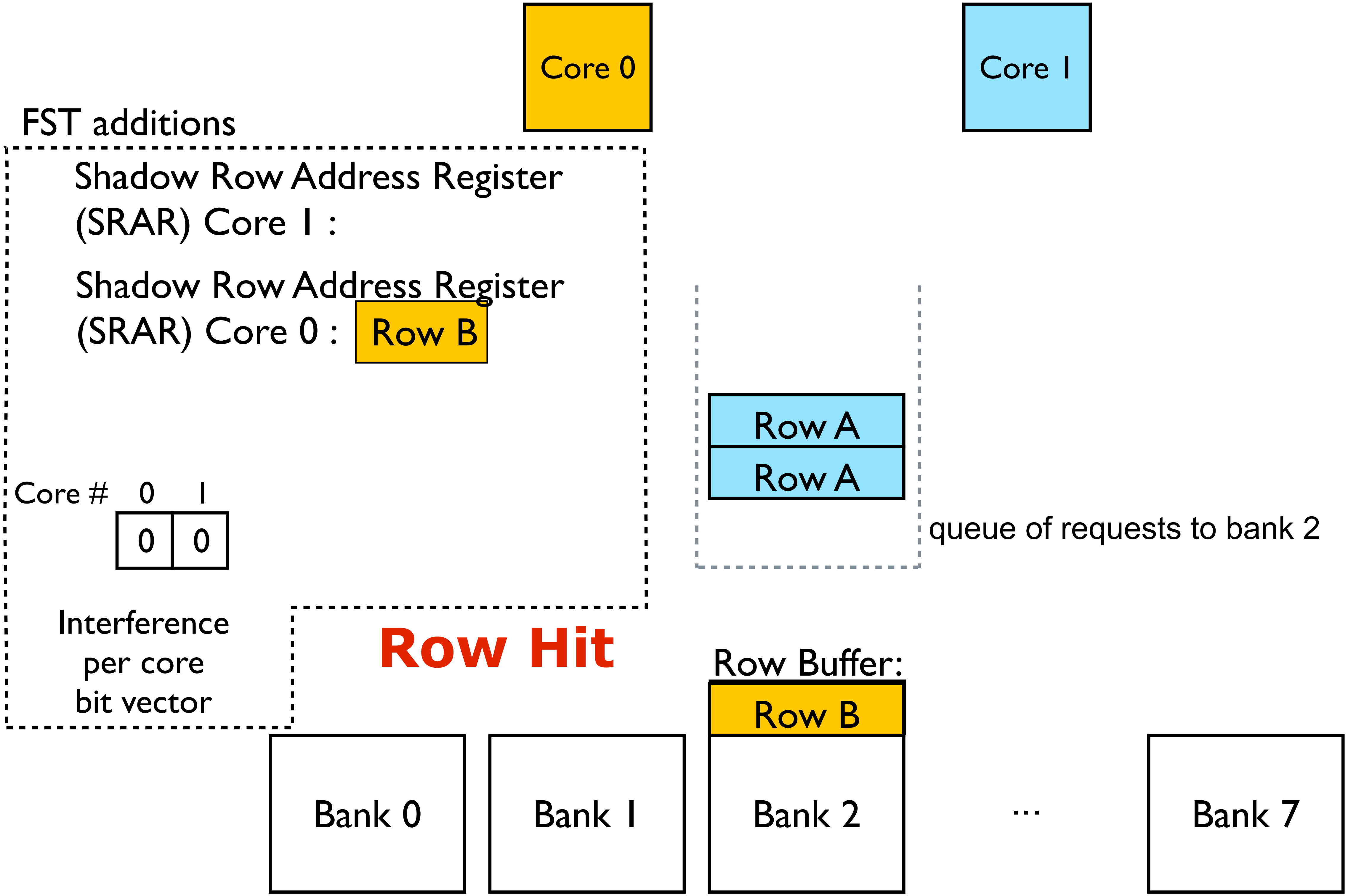
Bank 1

Bank 2

...

Bank 7

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 :

Shadow Row Address Register (SRAR) Core 0 : Row B

Core #	0	1
	0	0

Interference per core bit vector

Row Hit

Row A

Row A

queue of requests to bank 2

Row Buffer: Row B

Bank 0

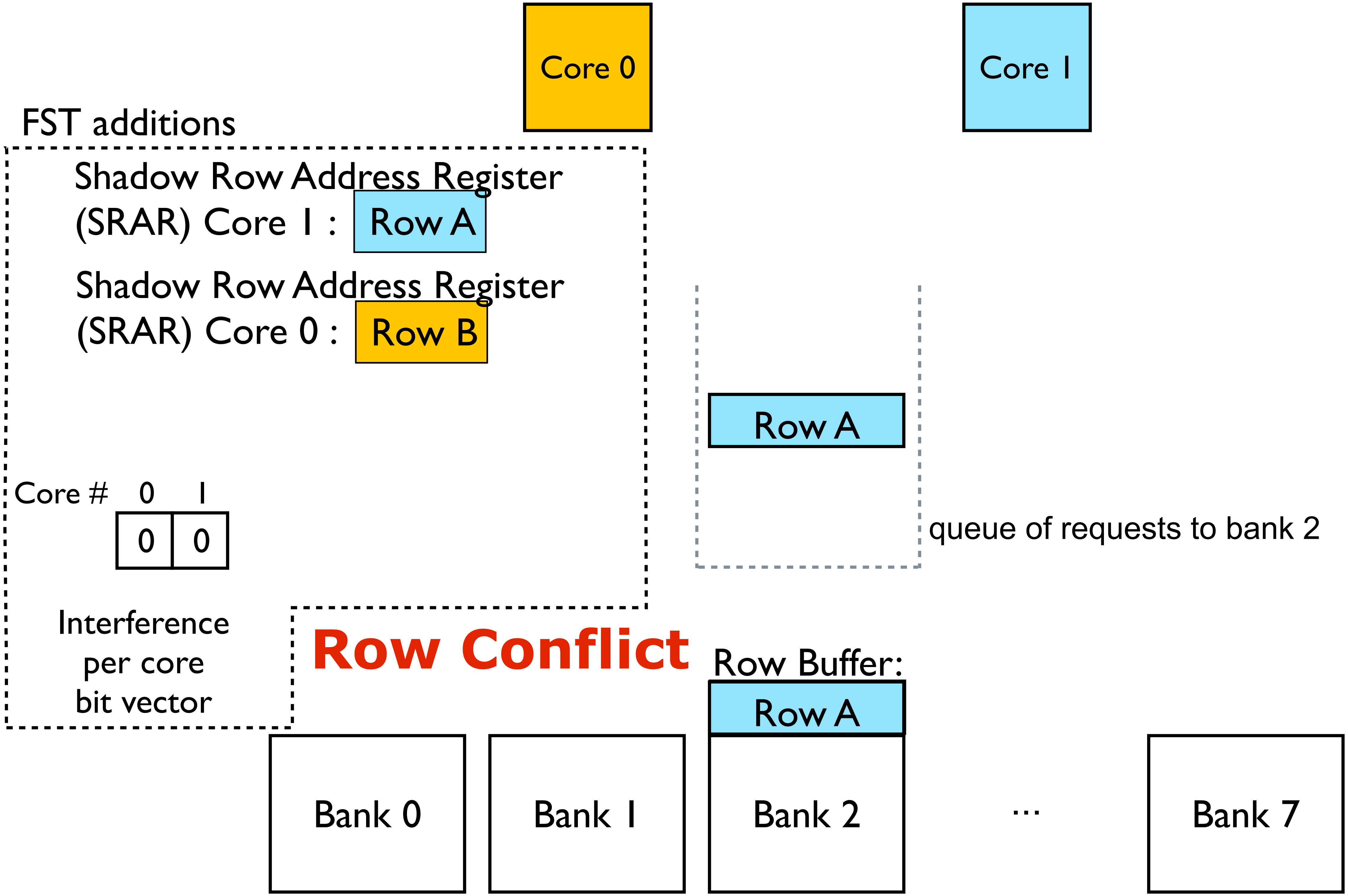
Bank 1

Bank 2

…

Bank 7

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 : Row A

Shadow Row Address Register (SRAR) Core 0 : Row B

Core #	0	1
	0	0

Interference per core bit vector

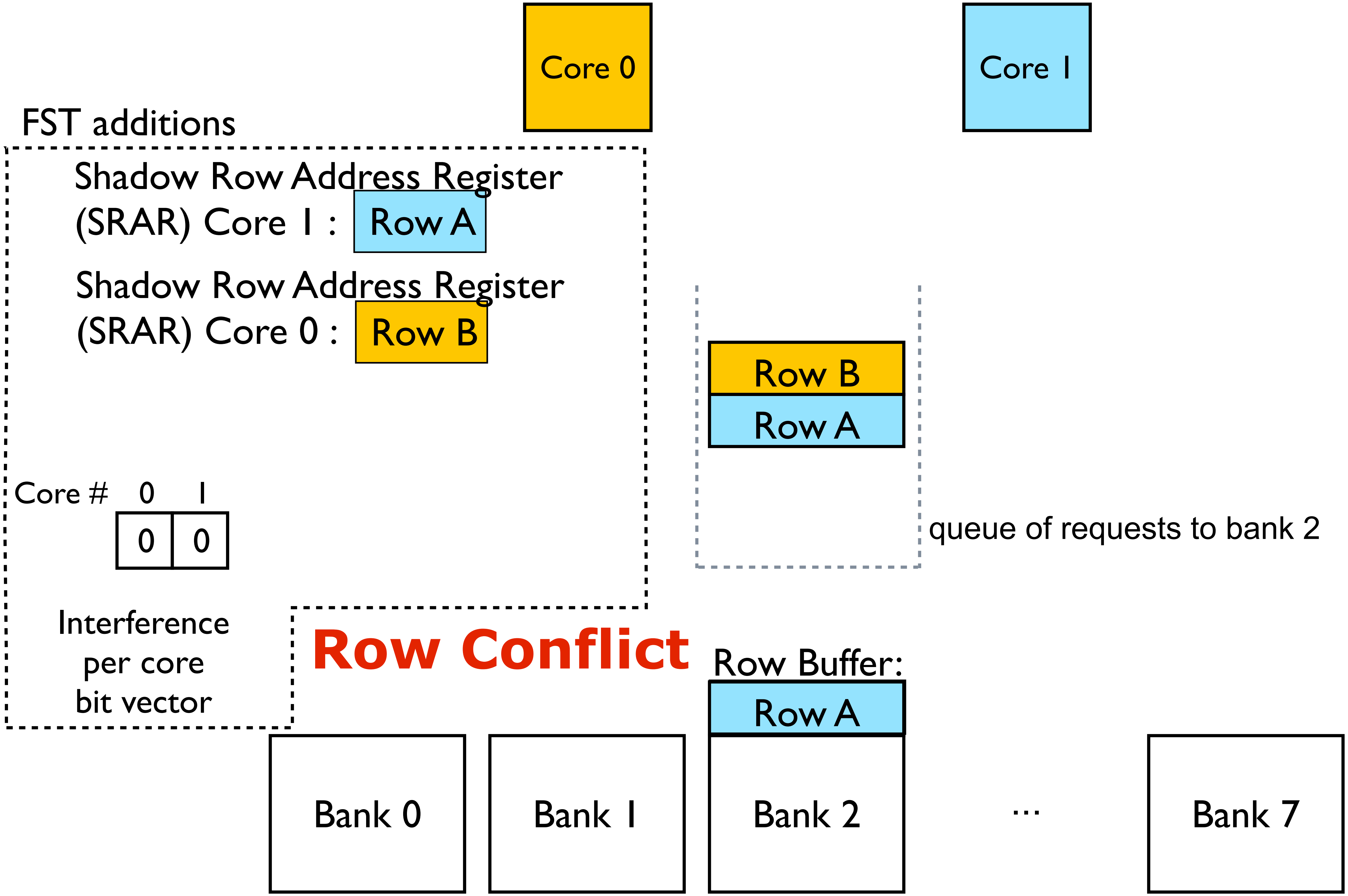
Row Conflict

Row A

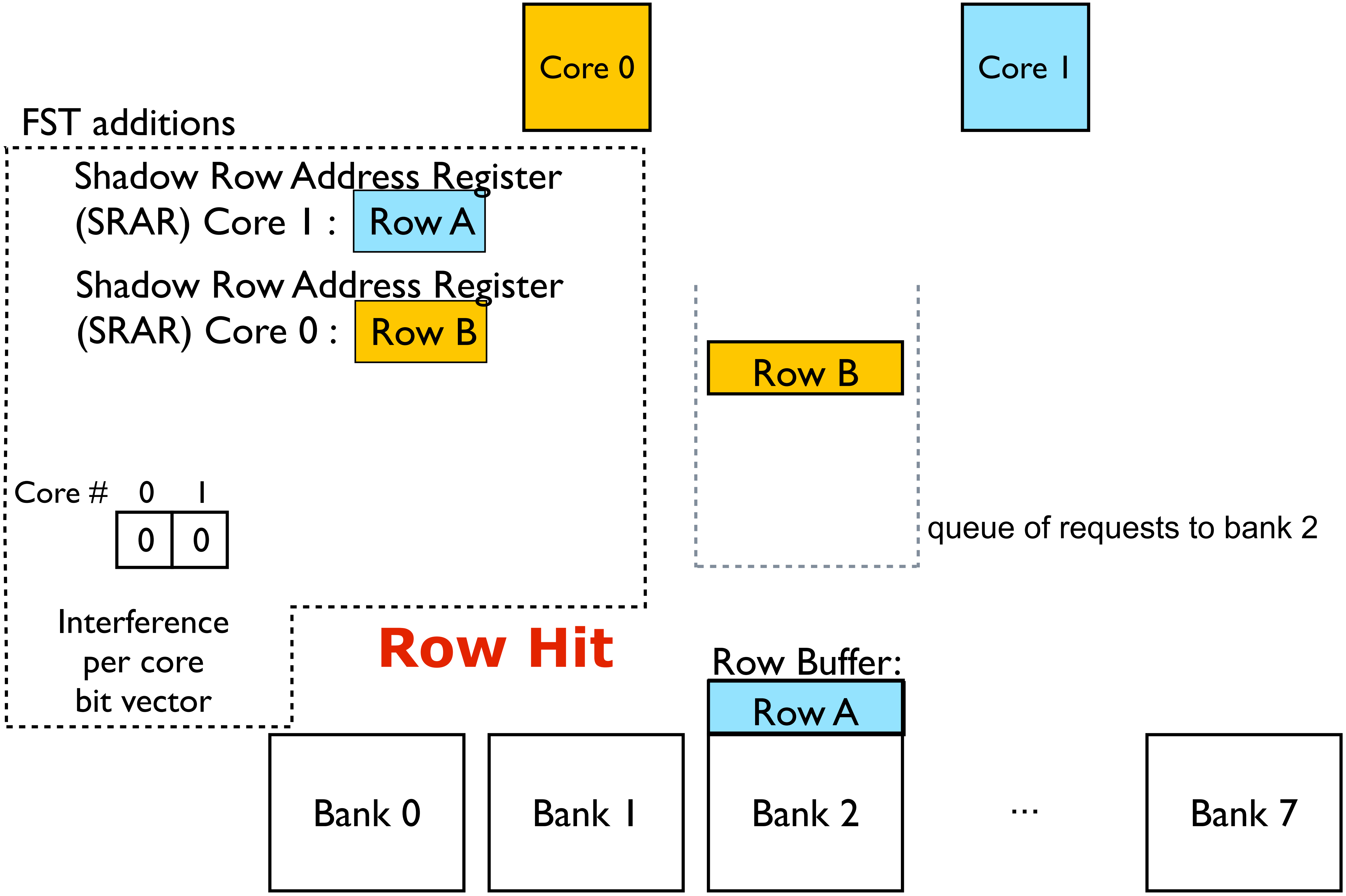
queue of requests to bank 2

Row Buffer: Row A

Tracking DRAM Row-Buffer Interference



Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 : Row A

Shadow Row Address Register (SRAR) Core 0 : Row B

Core #	0	1
	0	0

Interference per core bit vector

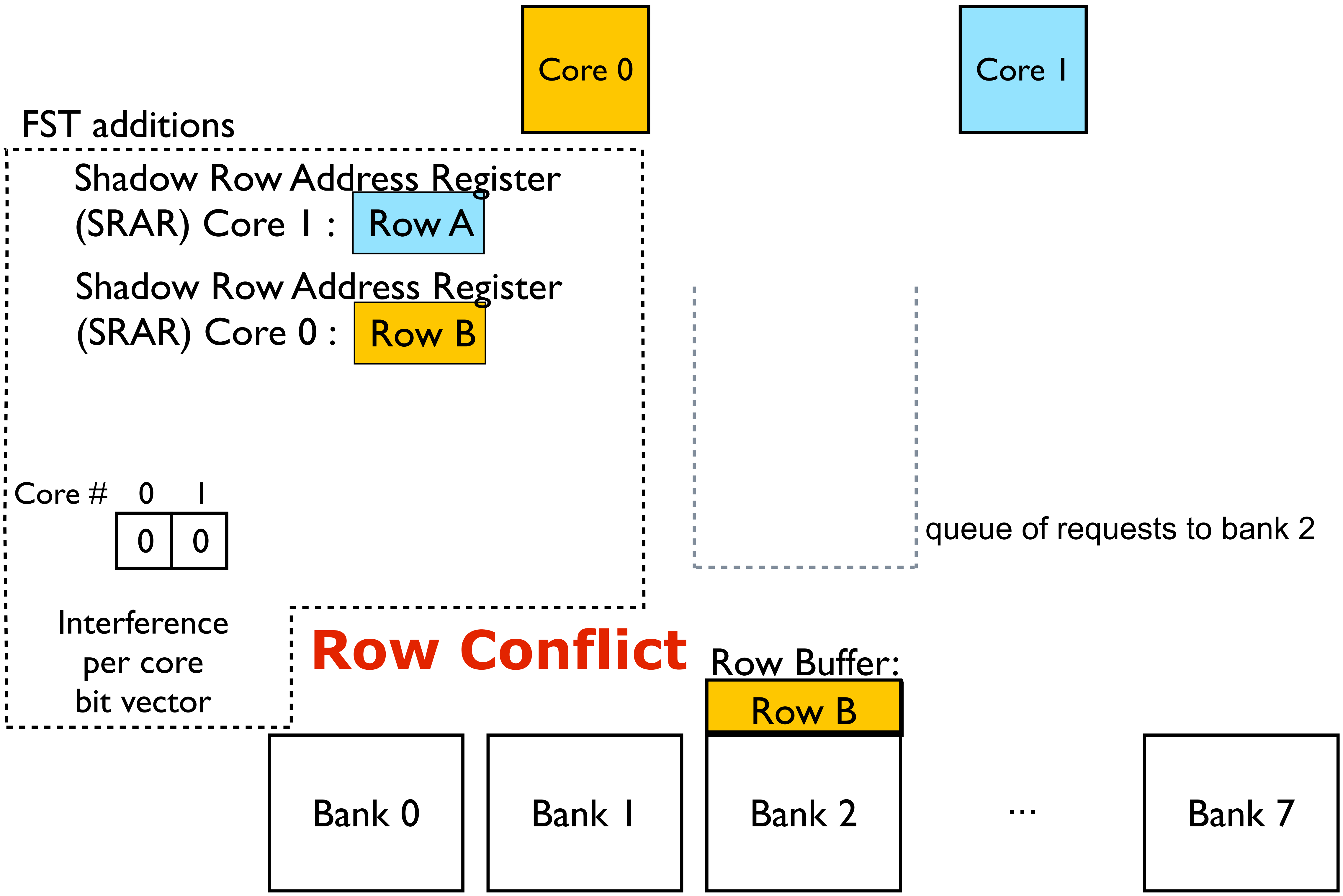
Row Hit

Row B

queue of requests to bank 2

Row Buffer: Row A

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 : Row A

Shadow Row Address Register (SRAR) Core 0 : Row B

Core # 0 1

0 0

Interference per core bit vector

queue of requests to bank 2

Row Conflict

Row Buffer: Row B

Bank 0

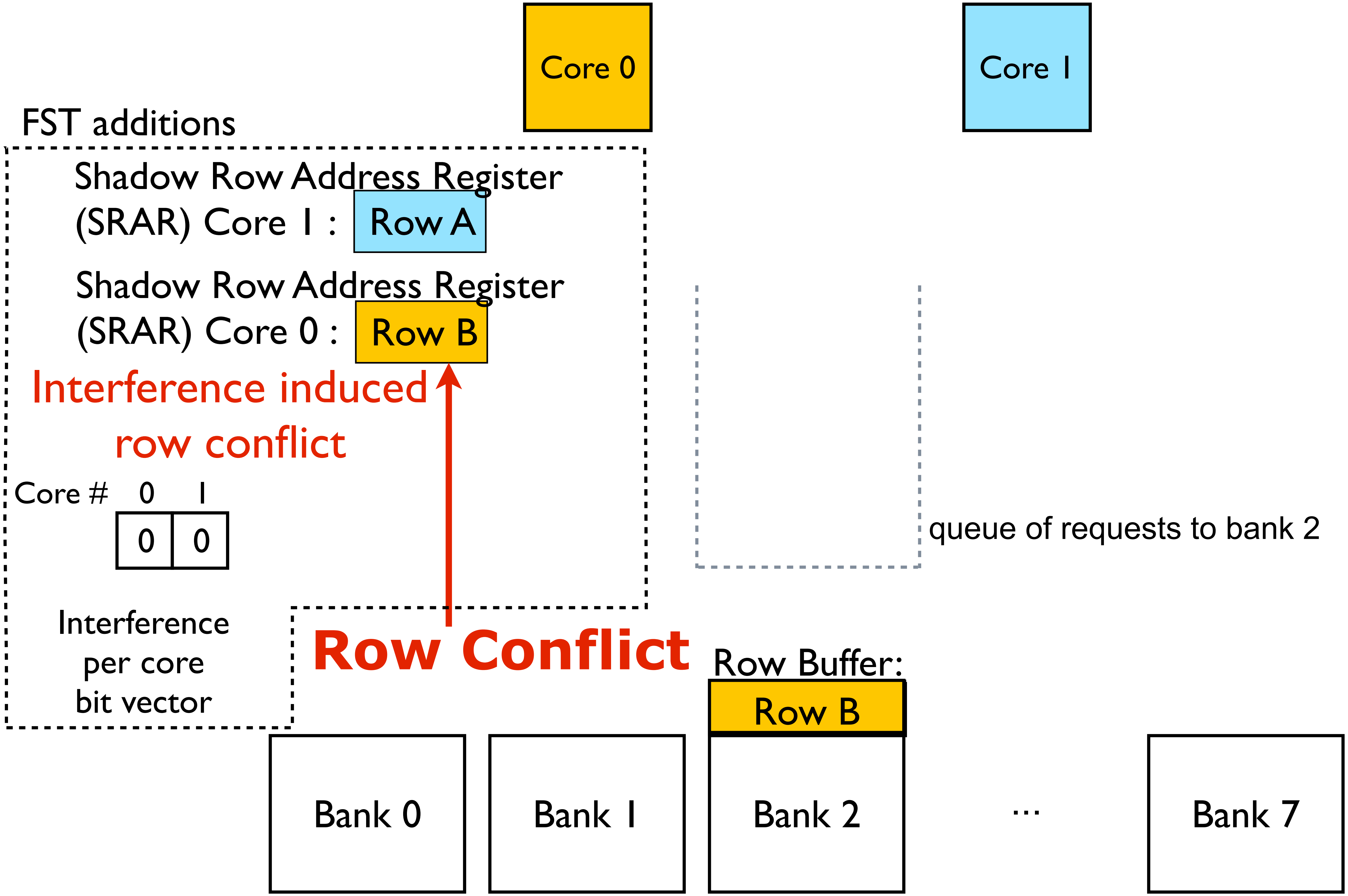
Bank 1

Bank 2

…

Bank 7

Tracking DRAM Row-Buffer Interference



Core 0

Core 1

FST additions

Shadow Row Address Register (SRAR) Core 1 : Row A

Shadow Row Address Register (SRAR) Core 0 : Row B

Interference induced row conflict

Core #	0	1
	0	0

Interference per core bit vector

Row Conflict

queue of requests to bank 2

Row Buffer: Row B

Bank 0

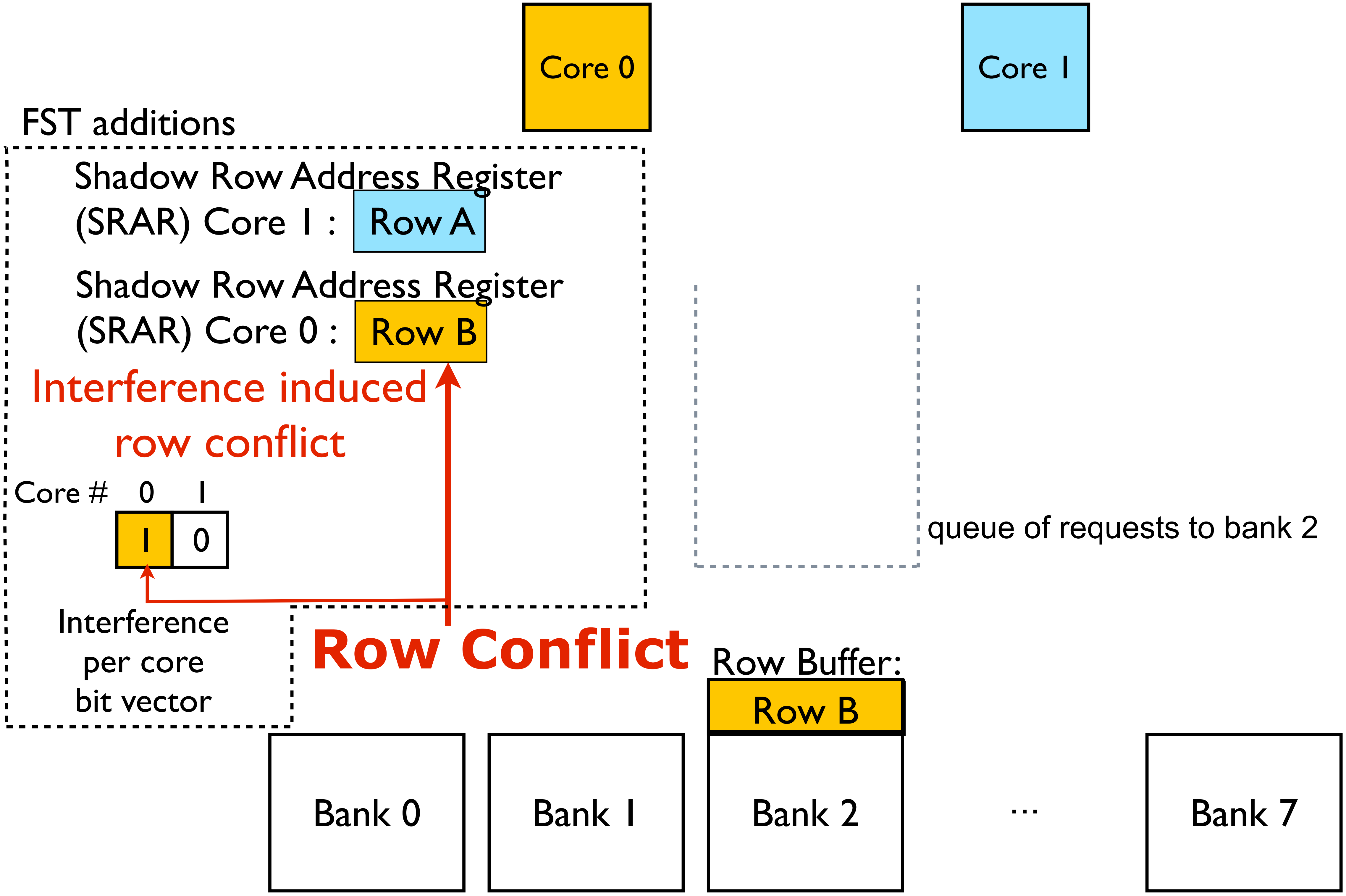
Bank 1

Bank 2

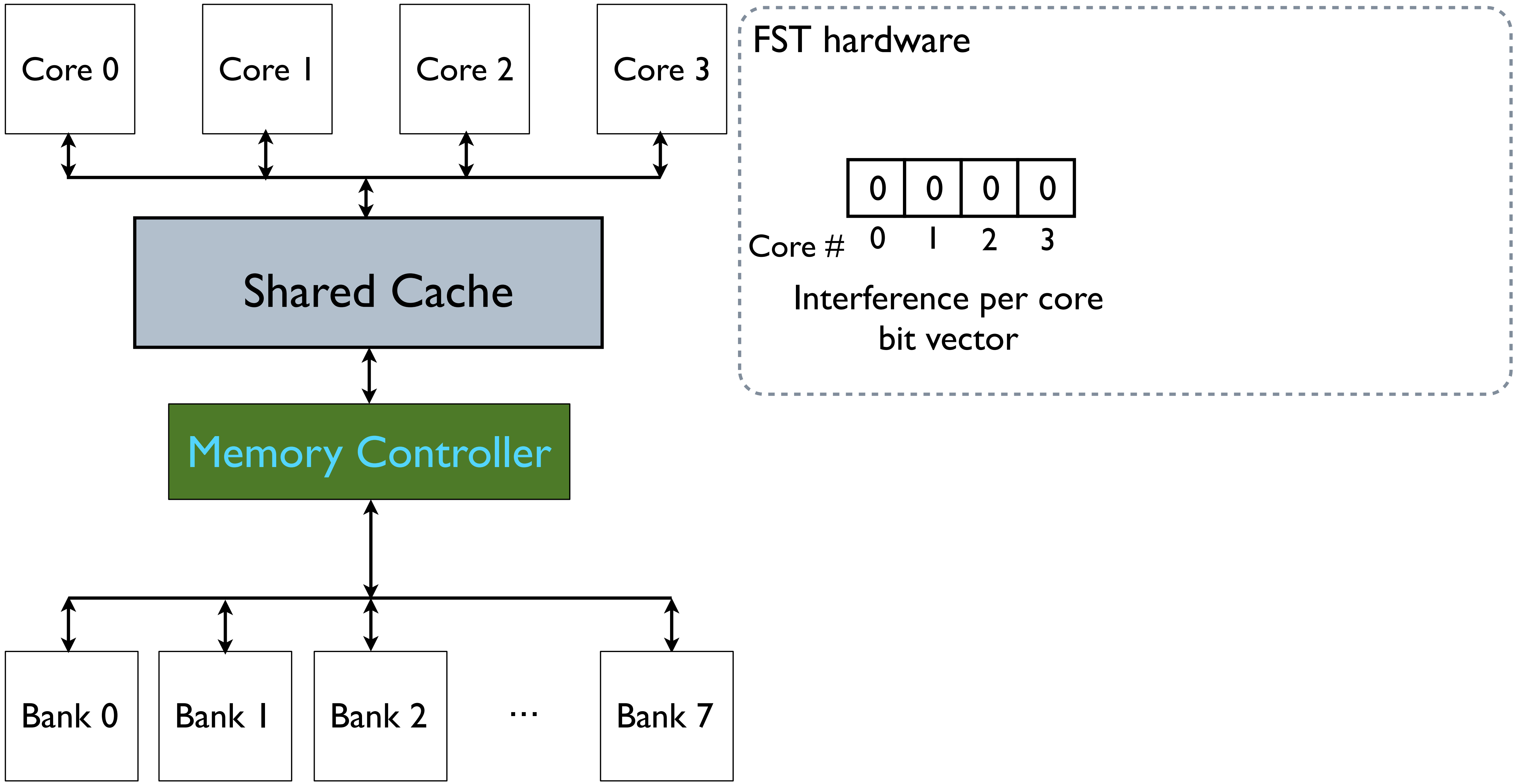
…

Bank 7

Tracking DRAM Row-Buffer Interference


Core 0
Core 1
FST additions
Shadow Row Address Register (SRAR) Core 1 :
Row A
Shadow Row Address Register (SRAR) Core 0 :
Row B
Interference induced row conflict
Core #
0
1
1
0
Interference per core bit vector
Row Conflict
queue of requests to bank 2
Row Buffer:
Row B
Bank 0
Bank 1
Bank 2
...
Bank 7

Tracking Inter-Core Interference



Core 0

Core 1

Core 2

Core 3

Shared Cache

Memory Controller

Bank 0

Bank 1

Bank 2

…

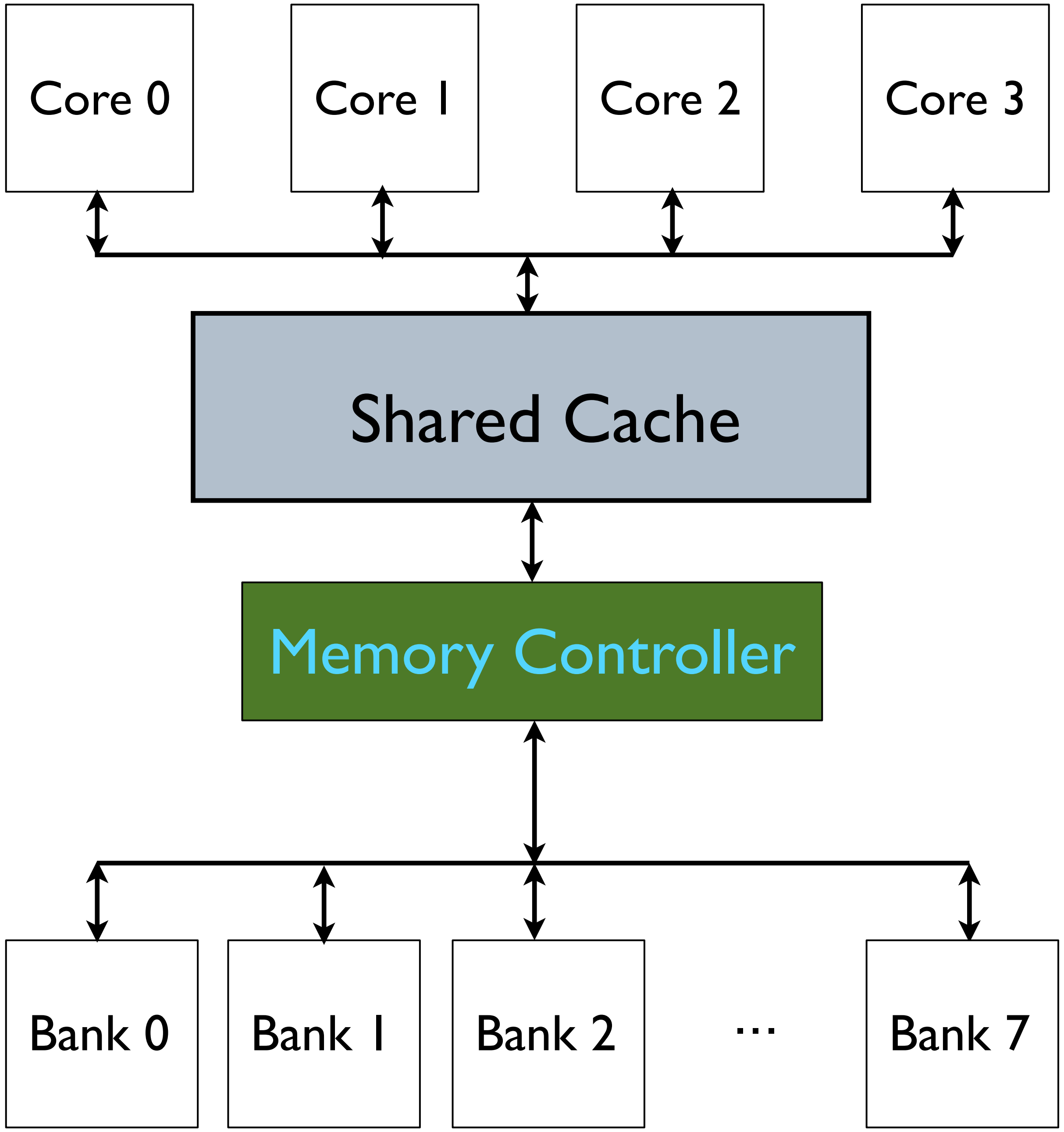
Bank 7

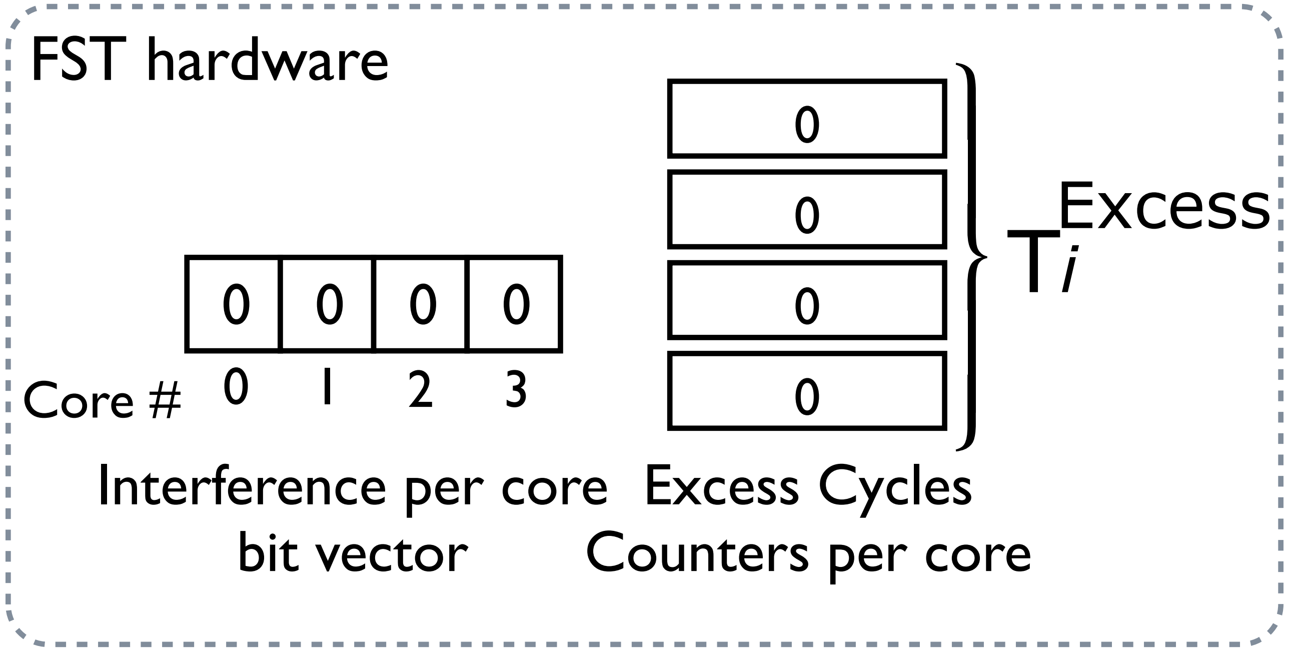
FST hardware

Core #	0	1	2	3
	0	0	0	0

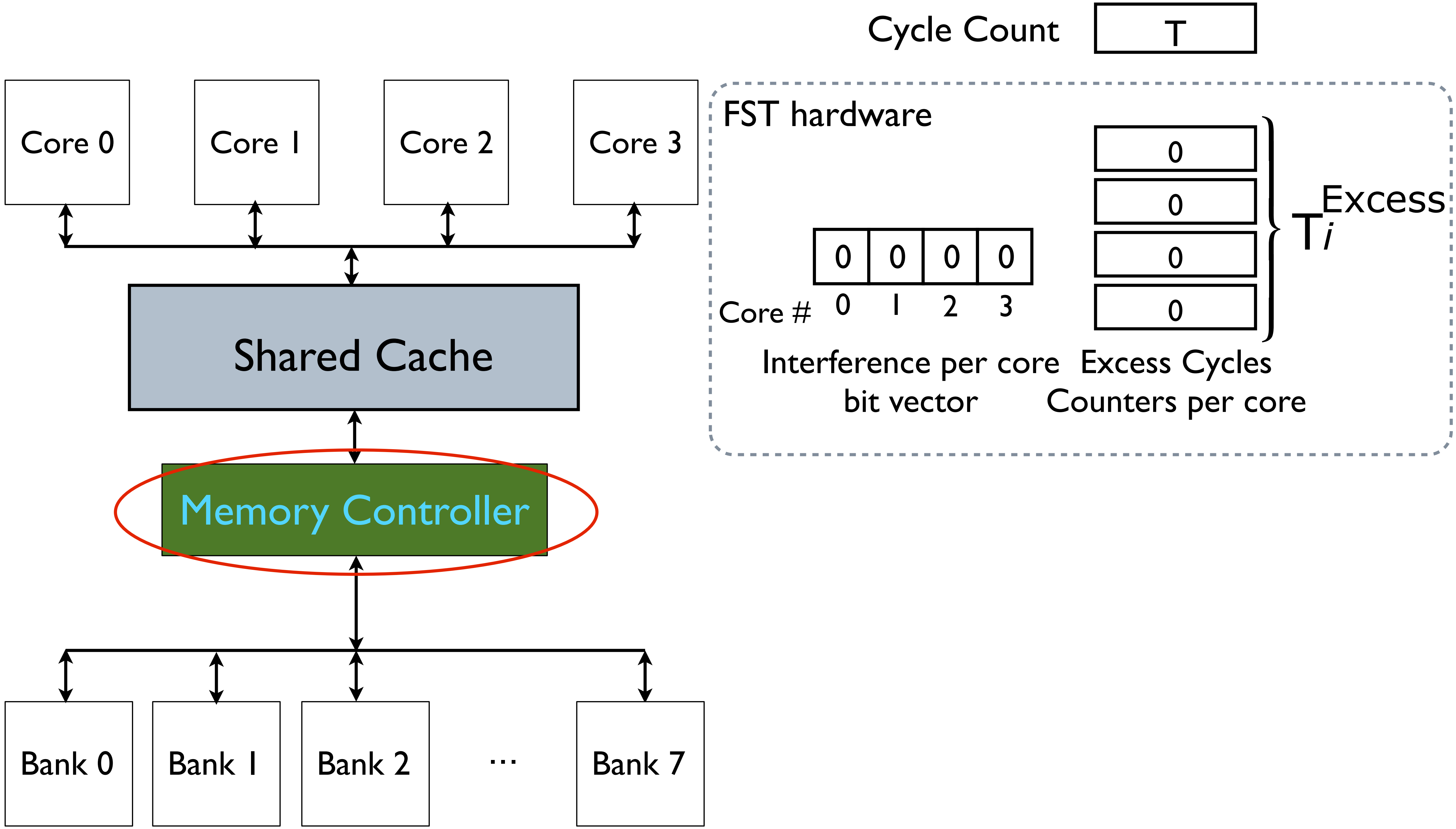
Interference per core bit vector

Tracking Inter-Core Interference

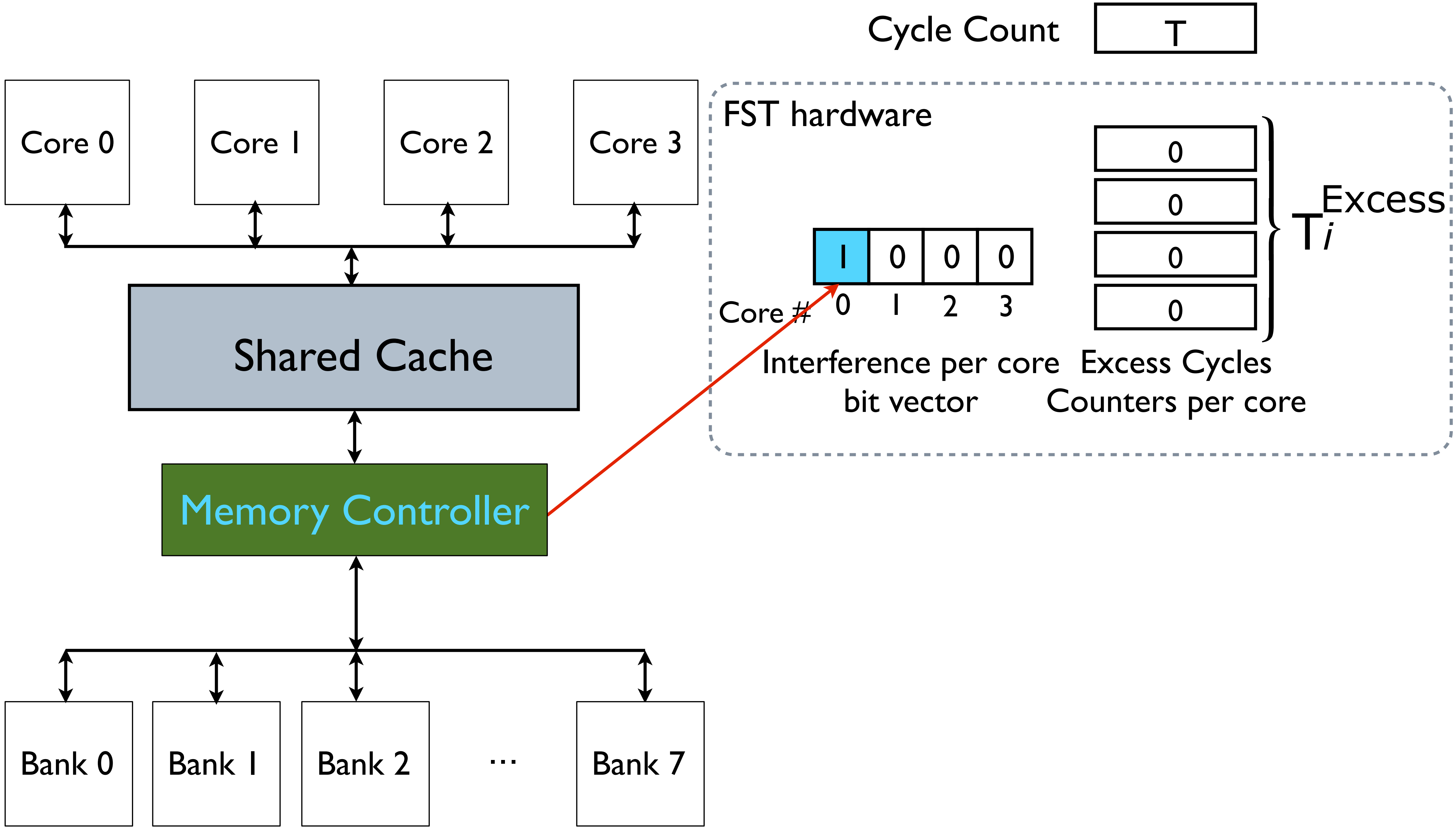



FST hardware
0 0 0 0
Core # 0 1 2 3
Interference per core bit vector
0
0
0
0
T_i^{Excess}
Excess Cycles Counters per core

Tracking Inter-Core Interference



Tracking Inter-Core Interference



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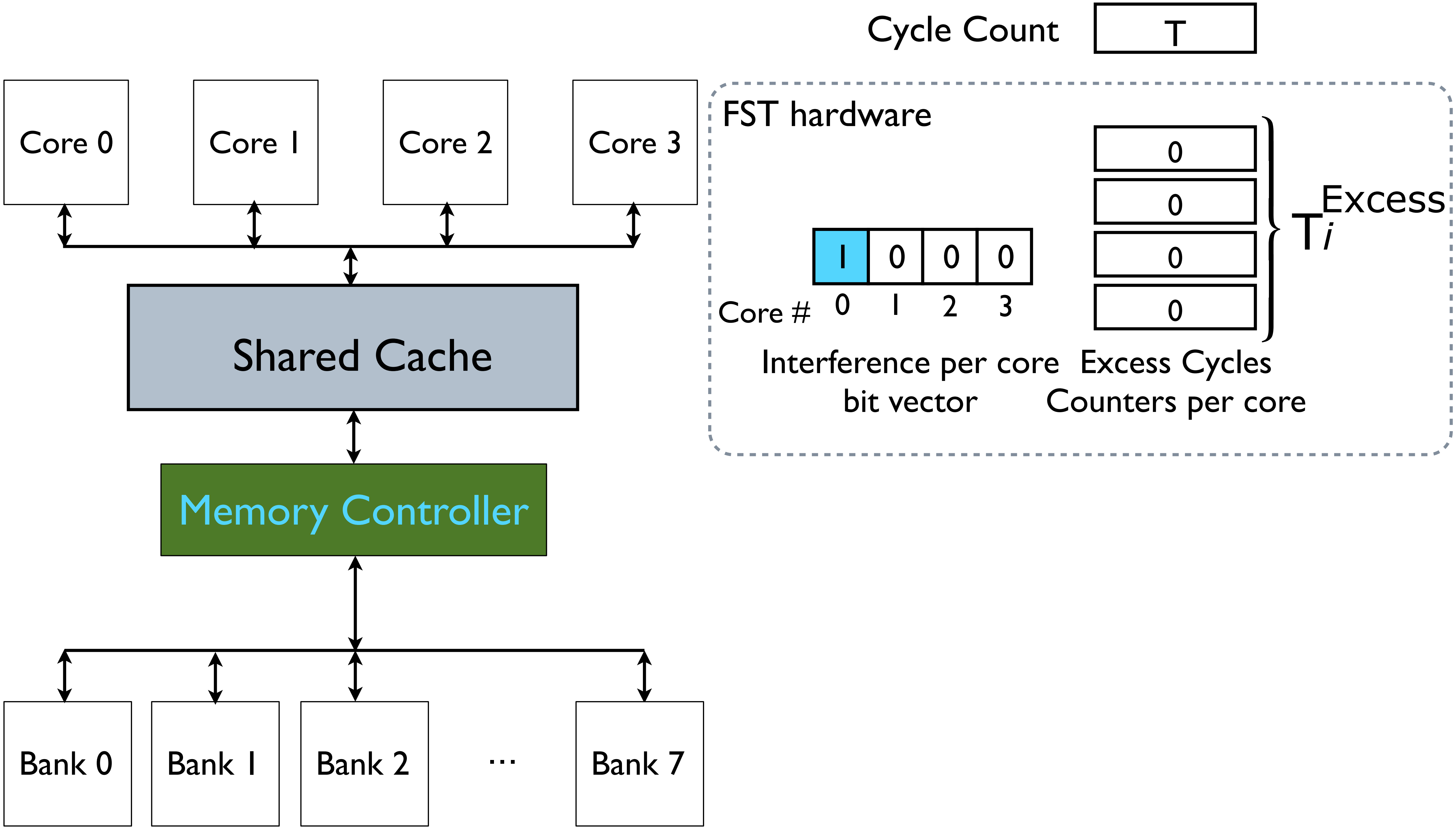

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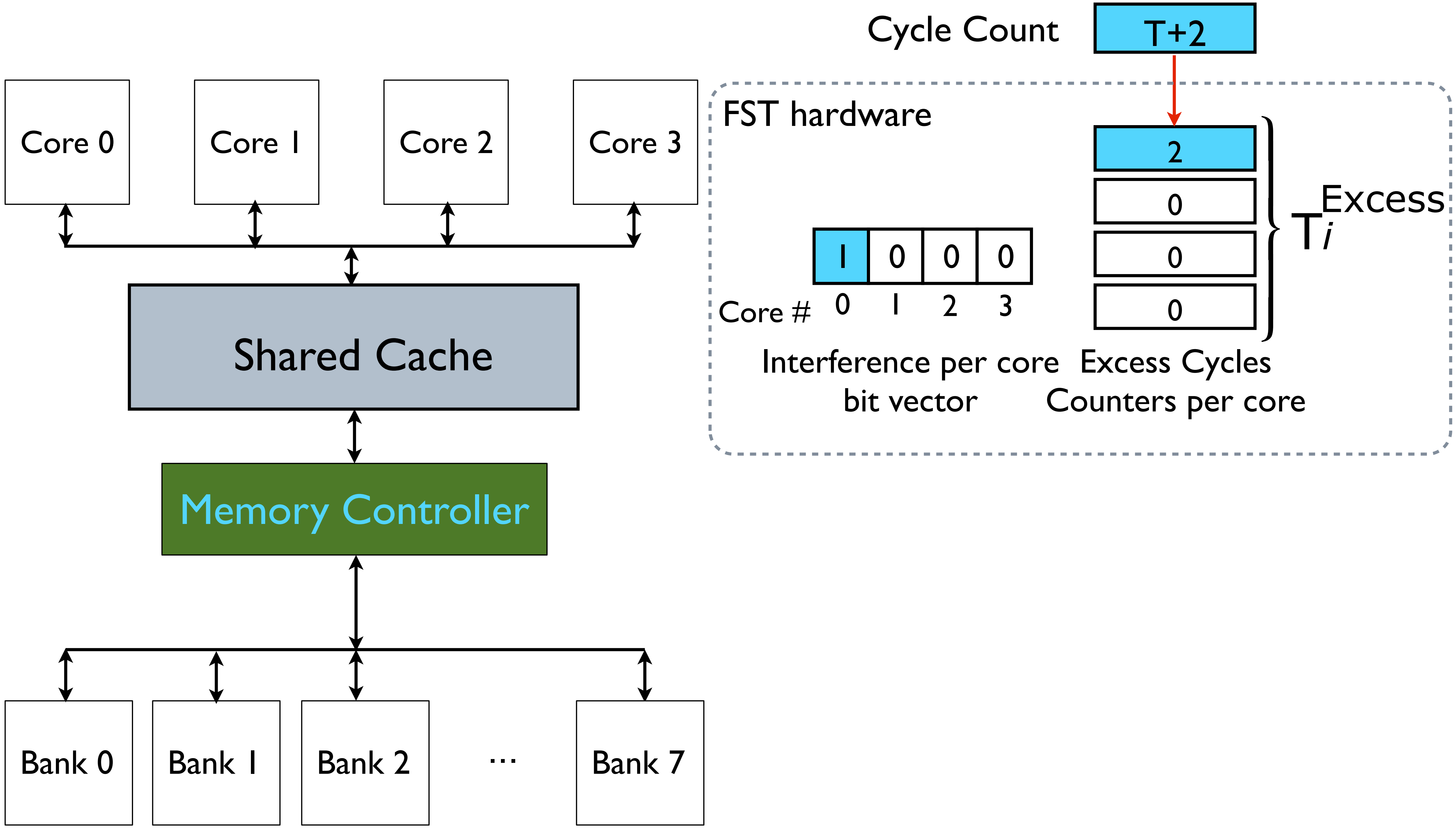
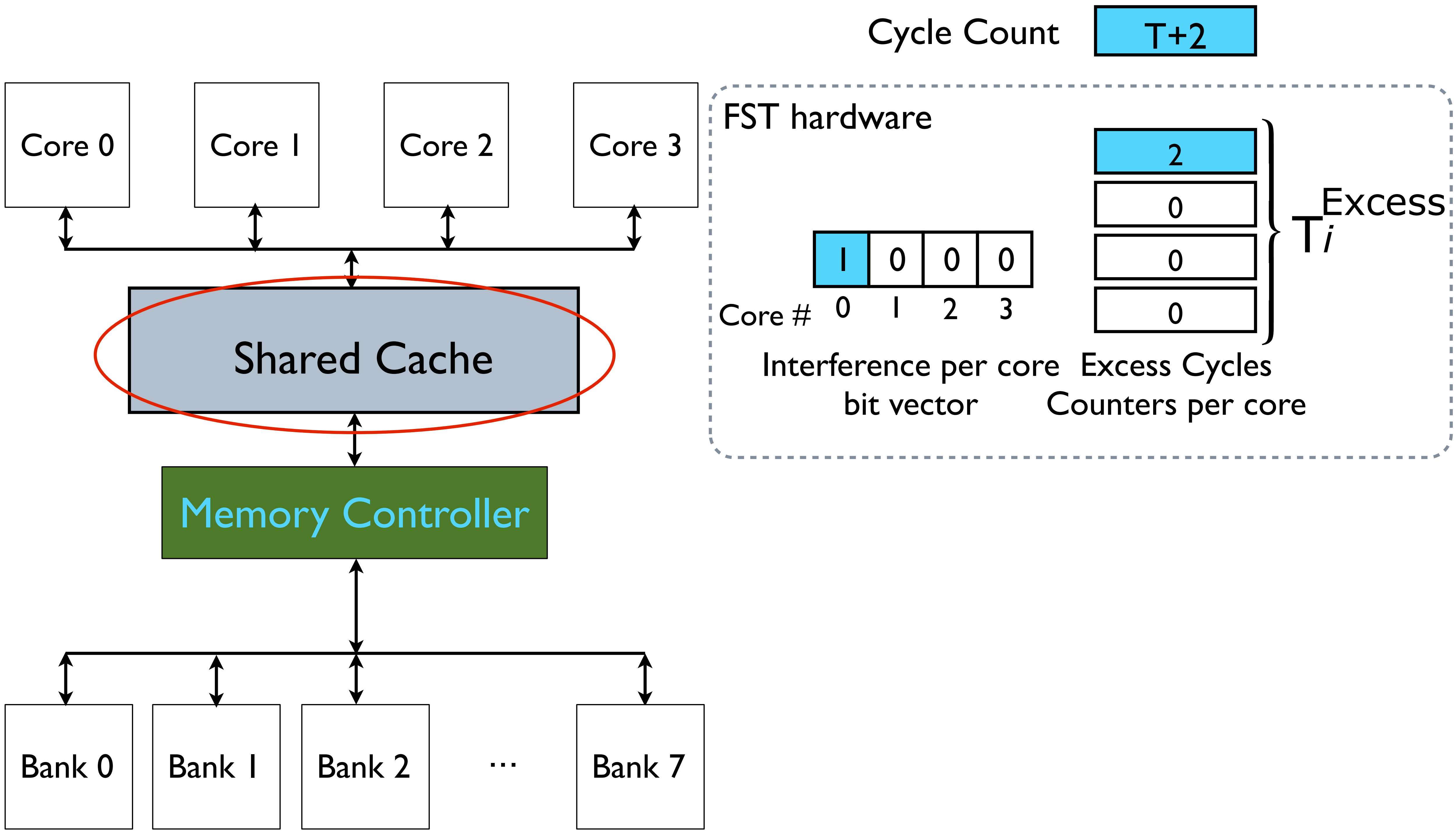


Tracking Inter-Core Interference



Cycle Count T+2

FST hardware

Core #	0	1	2	3
	1	0	0	0

Interference per core bit vector

2
0
0
0

Excess Cycles Counters per core

T_i^{Excess}

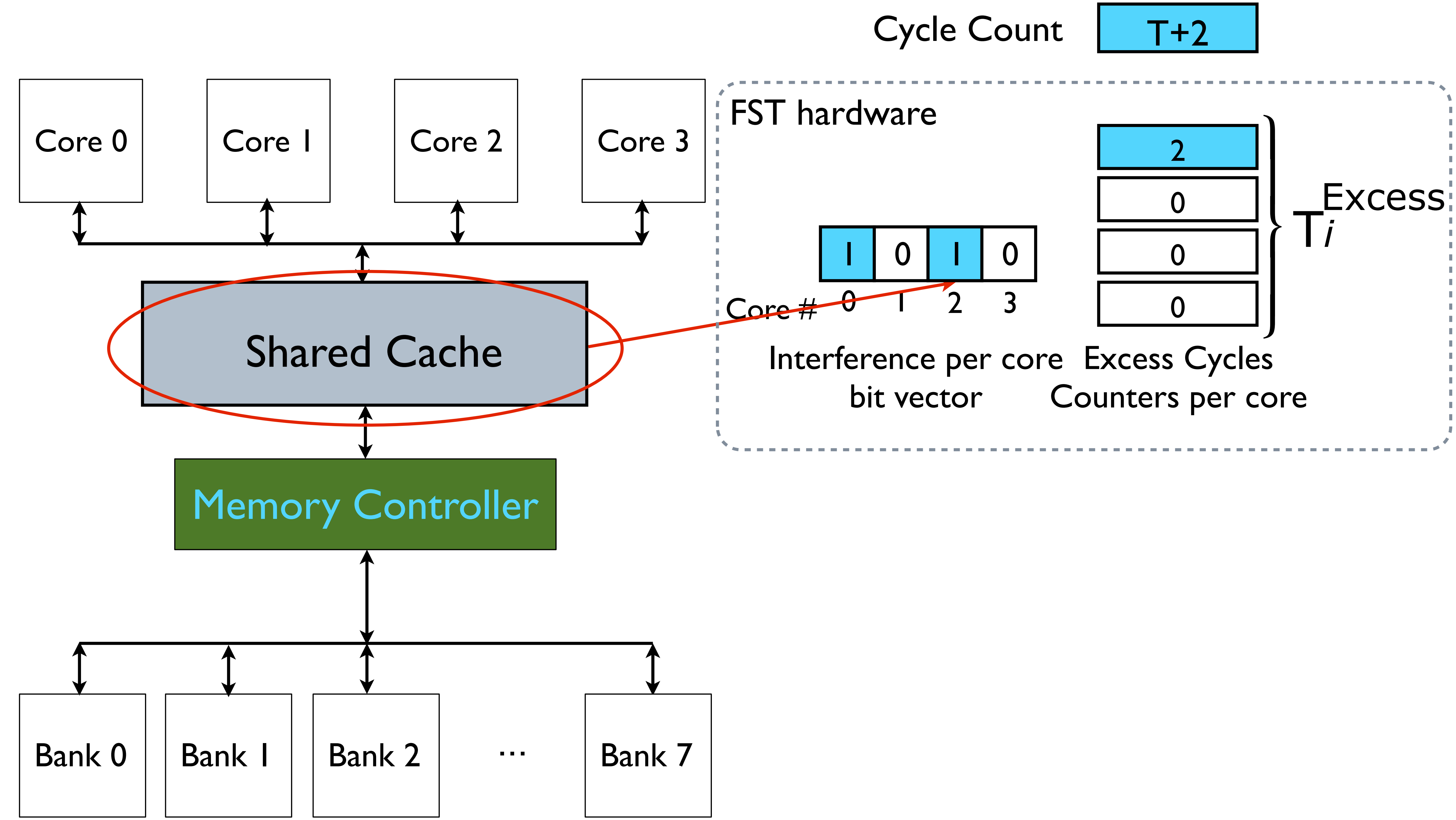
Core 0 Core 1 Core 2 Core 3

Shared Cache

Memory Controller

Bank 0 Bank 1 Bank 2 … Bank 7

Tracking Inter-Core Interference



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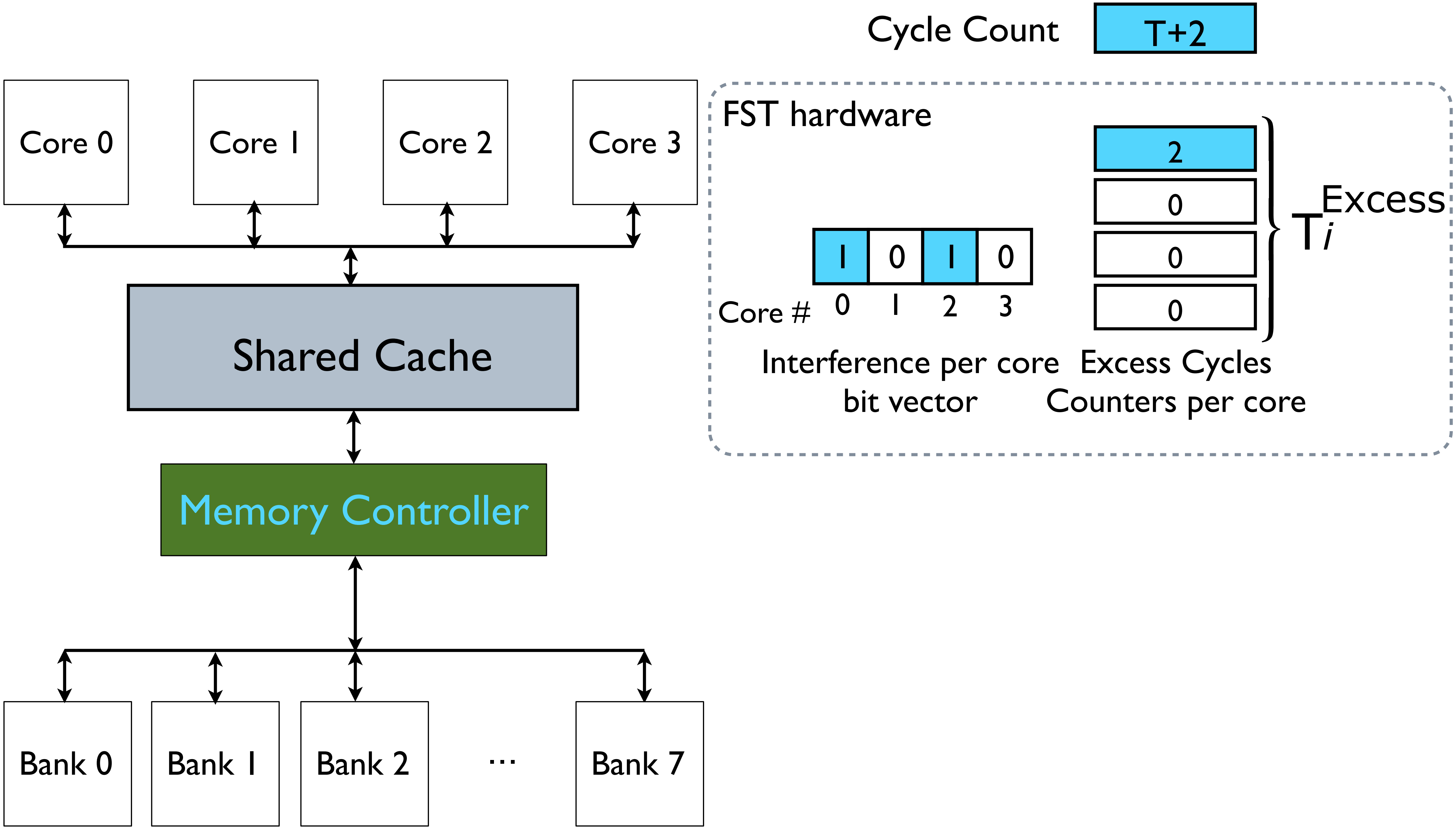

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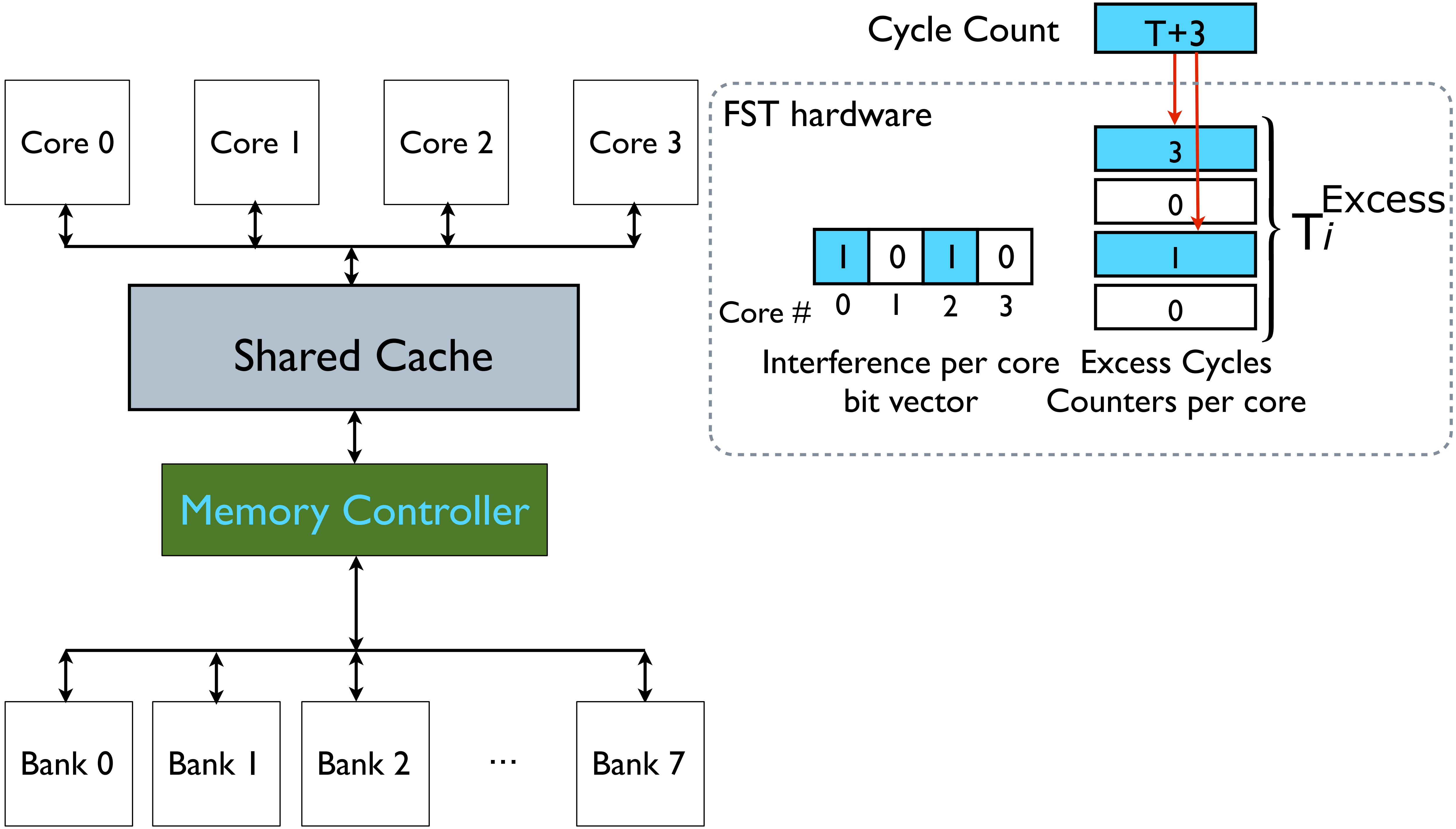
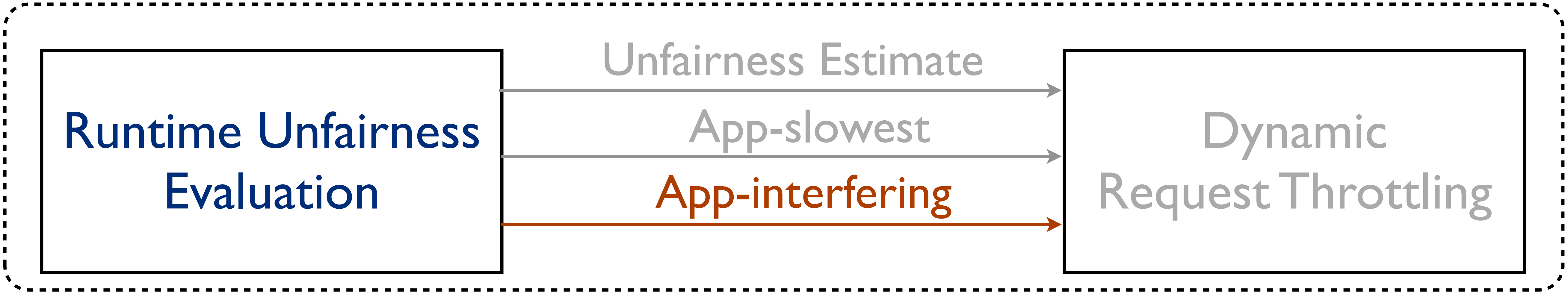


Fairness via Source Throttling (FST)

FST



1- Estimating system unfairness
2- Find app. with the highest slowdown (App-slowest)
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if (Unfairness Estimate >Target)
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 1-Throttle down App-interfering
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Tracking Inter-Core Interference

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  - FST separately tracks interference caused by each core *j* (*j* ≠ *i*)

Tracking Inter-Core Interference

- To identify App-interfering, for each core *i*
  - FST separately tracks interference caused by each core *j* ($j \neq i$)

Interference per core
bit vector

Core #	0	1	2	3
	0	0	0	0

Tracking Inter-Core Interference

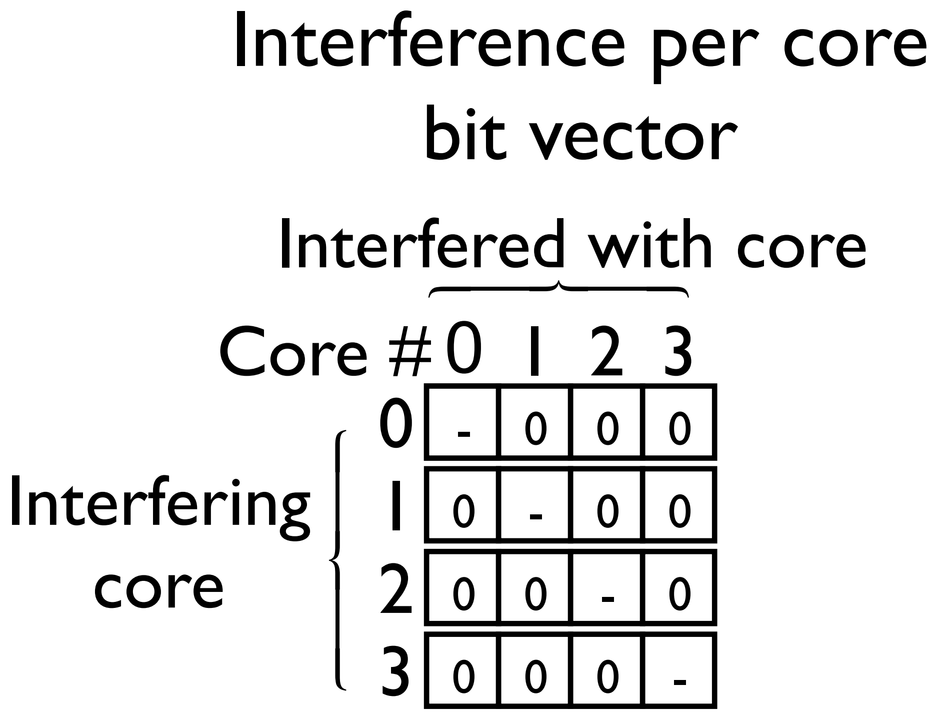
- To identify App-interfering, for each core *i*
  - FST separately tracks interference caused by each core *j* (*j* ≠ *i*)

Interference per core
bit vector

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Inter-Core Interference

- To identify App-interfering, for each core *i*
  - FST separately tracks interference caused by each core *j* (*j* ≠ *i*)



Interference per core
bit vector

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Inter-Core Interference

- To identify App-interfering, for each core *i*
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Interference per core
bit vector

Interfered with core

Interfering core	Core #	0	1	2	3
	0	-	0	0	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Excess Cycles
Counters per core

Cnt 0	Cnt 1	Cnt 2	Cnt 3

Tracking Inter-Core Interference

- To identify App-interfering, for each core *i*
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Interference per core
bit vector

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Excess Cycles
Counters per core

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

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Interference per core
bit vector

Interfered with core

Interfering core

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0	-	0	0	0
1	0	-	0	0
2	0	1	-	0
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Excess Cycles
Counters per core

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

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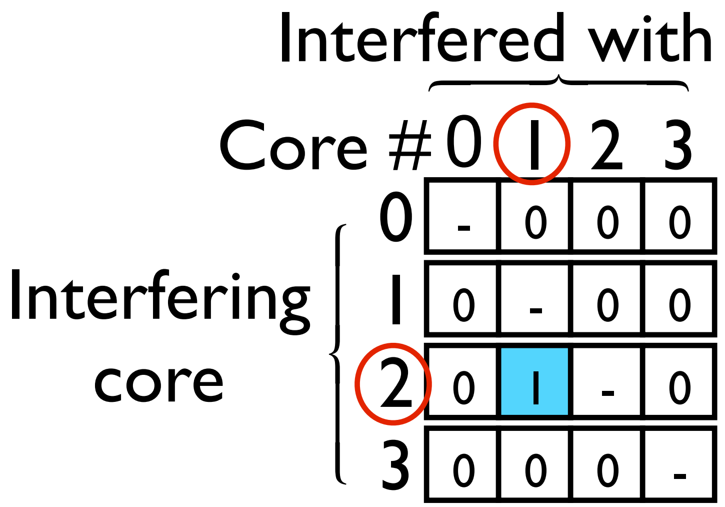

		Interfered with core			
	Core #	0	1	2	3
Interfering core	0	-	0	0	0
	1	0	-	0	0
	2	0	1	-	0
	3	0	0	0	-

core 2 interfered with core 1

Excess Cycles Counters per core

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

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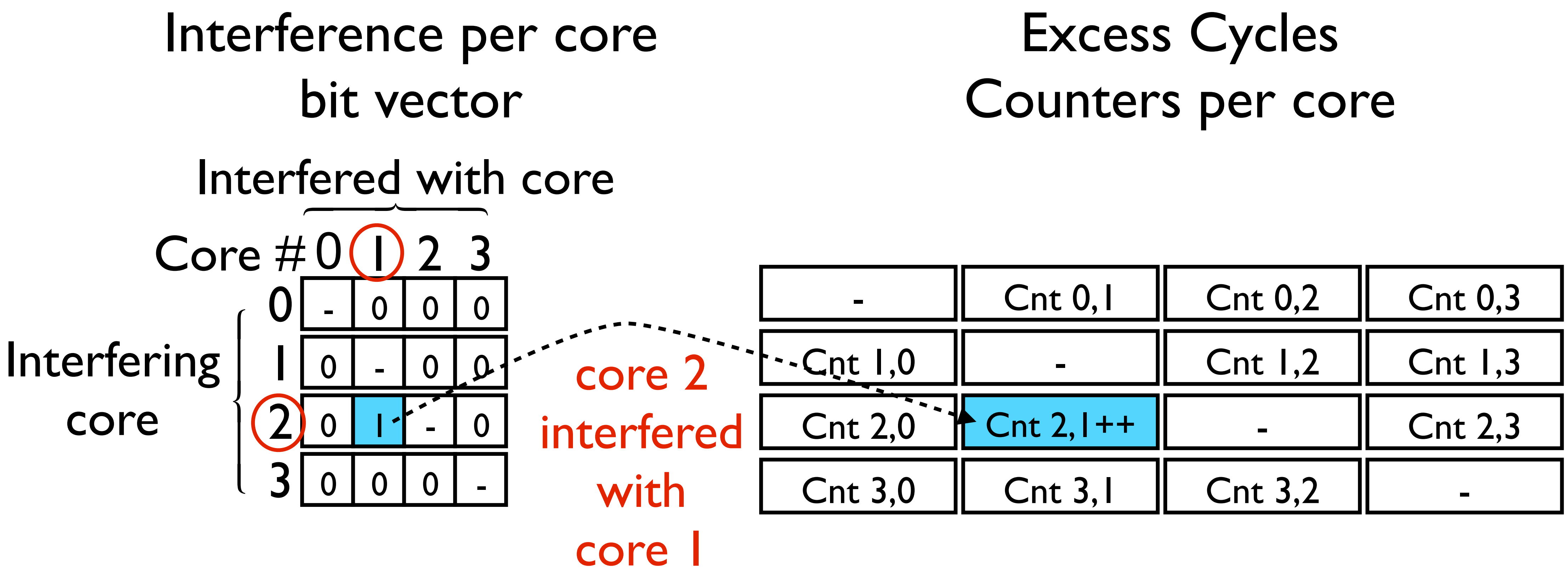

Interference per core bit vector

Interfered with core

Interfering core / Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	1	-	0
3	0	0	0	-

core 2 interfered with core 1

Excess Cycles Counters per core

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1++	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

Tracking Inter-Core Interference

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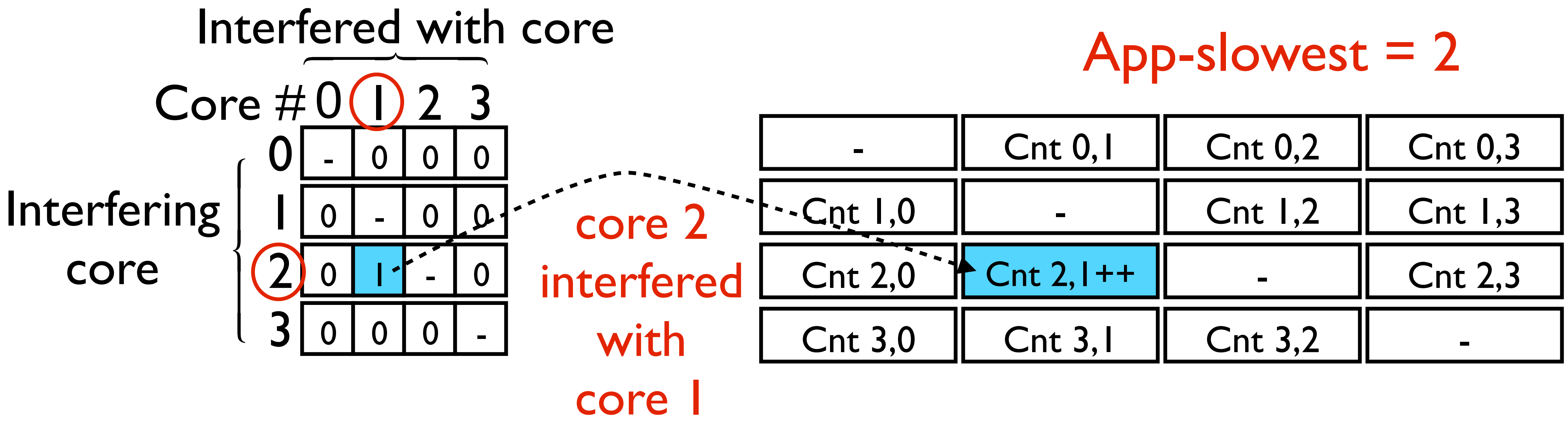
Interference per core bit vector

Excess Cycles Counters per core



Interfered with core

App-slowest = 2

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	1	-	0
3	0	0	0	-

Interfering core

core 2 interfered with core 1

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1++	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

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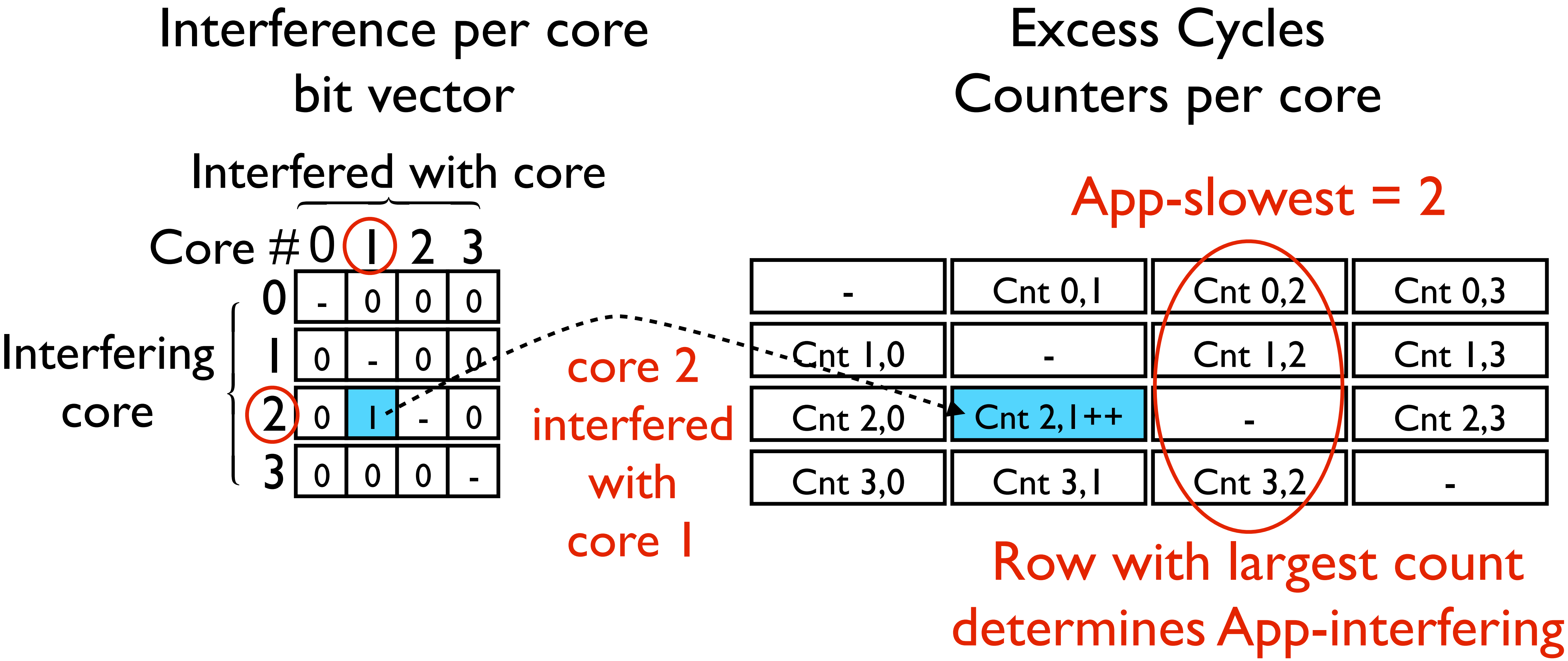


Interference per core bit vector

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	1	-	0
3	0	0	0	-

core 2 interfered with core 1

Excess Cycles Counters per core

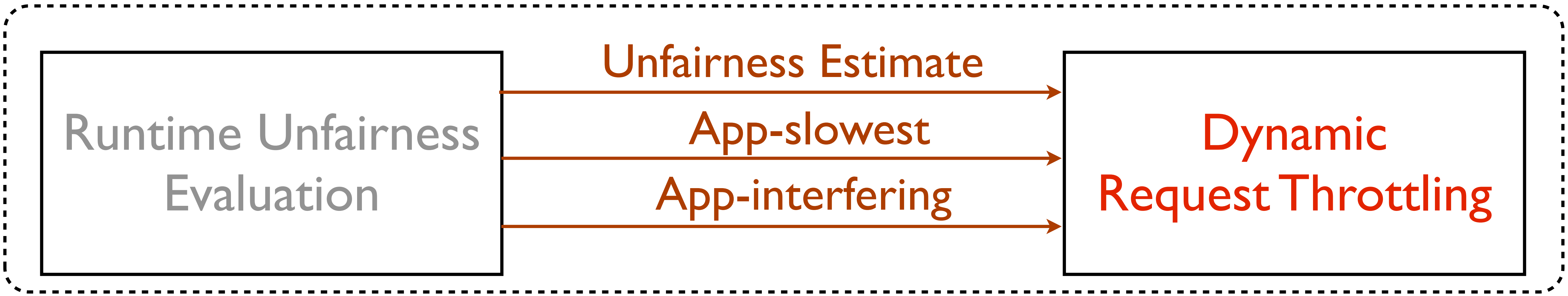
App-slowest = 2

-	Cnt 0,1	Cnt 0,2	Cnt 0,3
Cnt 1,0	-	Cnt 1,2	Cnt 1,3
Cnt 2,0	Cnt 2,1++	-	Cnt 2,3
Cnt 3,0	Cnt 3,1	Cnt 3,2	-

Row with largest count determines App-interfering

Fairness via Source Throttling (FST)

FST



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Dynamic Request Throttling

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- Goal: Adjust how aggressively each core makes requests to the shared resources

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- Mechanisms:
  - Miss Status Holding Register (MSHR) quota
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Dynamic Request Throttling

- Goal: Adjust how aggressively each core makes requests to the shared resources
- Mechanisms:
  - Miss Status Holding Register (MSHR) quota
    - Controls the number of concurrent requests accessing shared resources from each application
  - Request injection frequency
    - Controls how often memory requests are issued to the last level cache from the MSHRs

Dynamic Request Throttling

- Throttling level assigned to each core determines both MSHR quota and request injection rate

Dynamic Request Throttling

- Throttling level assigned to each core determines both MSHR quota and request injection rate

Throttling level	MSHR quota	Request Injection Rate
100%	128	Every cycle
50%	64	Every other cycle
25%	32	Once every 4 cycles
10%	12	Once every 10 cycles
5%	6	Once every 20 cycles
4%	5	Once every 25 cycles
3%	3	Once every 30 cycles
2%	2	Once every 50 cycles

Total # of MSHRs: 128

Dynamic Request Throttling

- Throttling level assigned to each core determines both MSHR quota and request injection rate

Throttling level	MSHR quota	Request Injection Rate
100%	128	Every cycle
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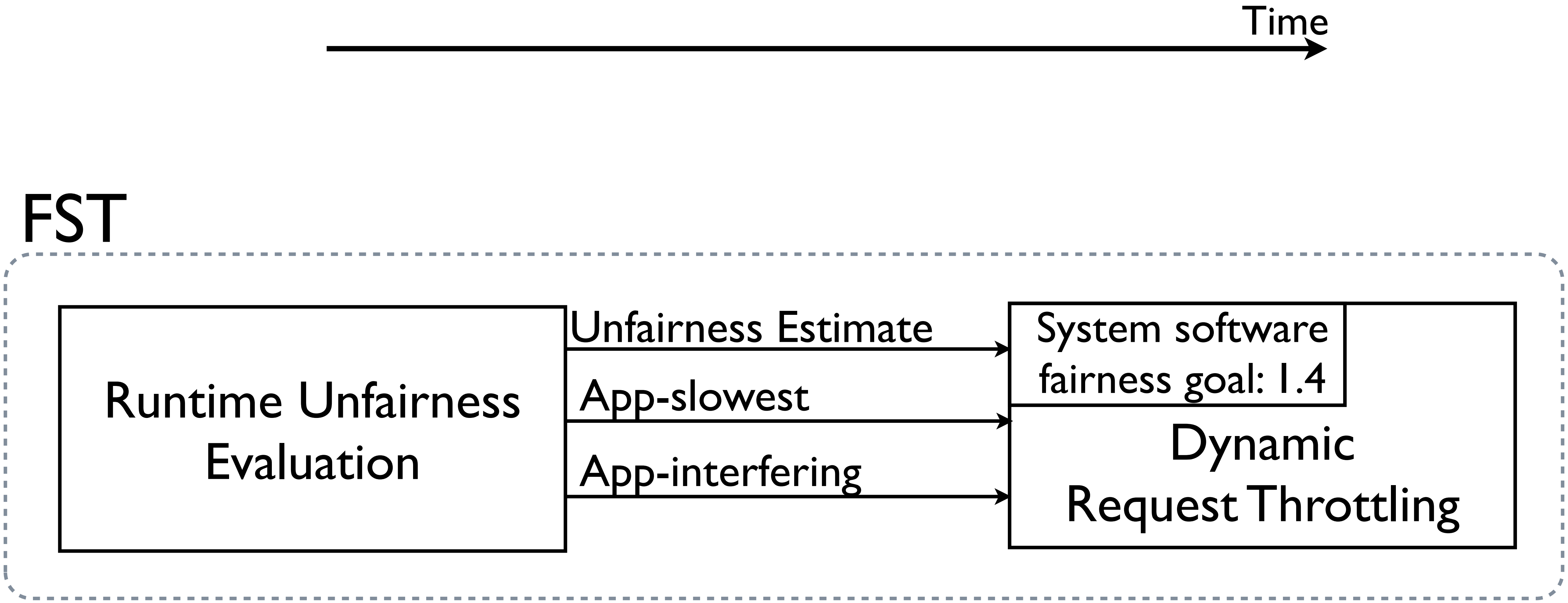
Total # of MSHRs: 128

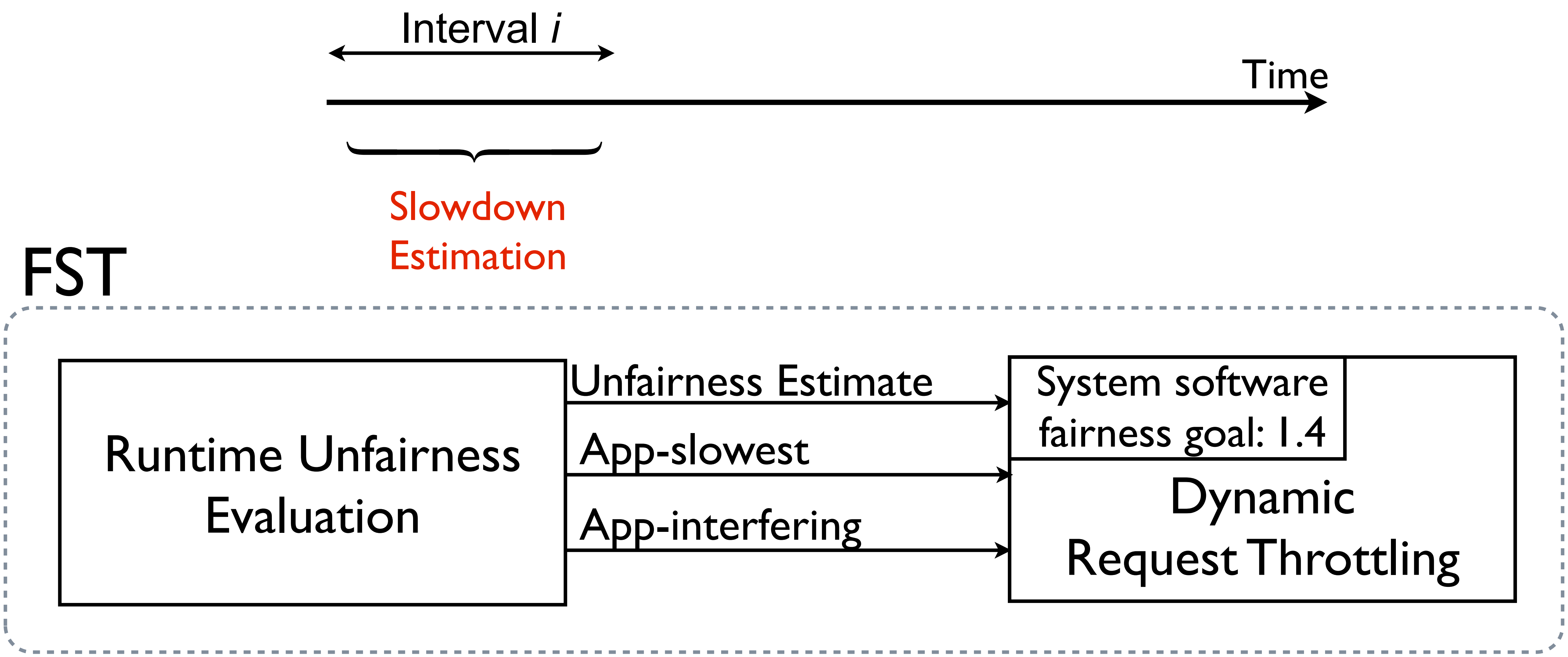
FST at Work


Time
FST
Runtime Unfairness Evaluation
Unfairness Estimate
App-slowest
App-interfering
System software fairness goal: 1.4
Dynamic Request Throttling

	Core 0	Core 1	Core 2	Core 3
Interval *i*				
Interval *i* + 1				
Interval *i* + 2				

Throttling Levels

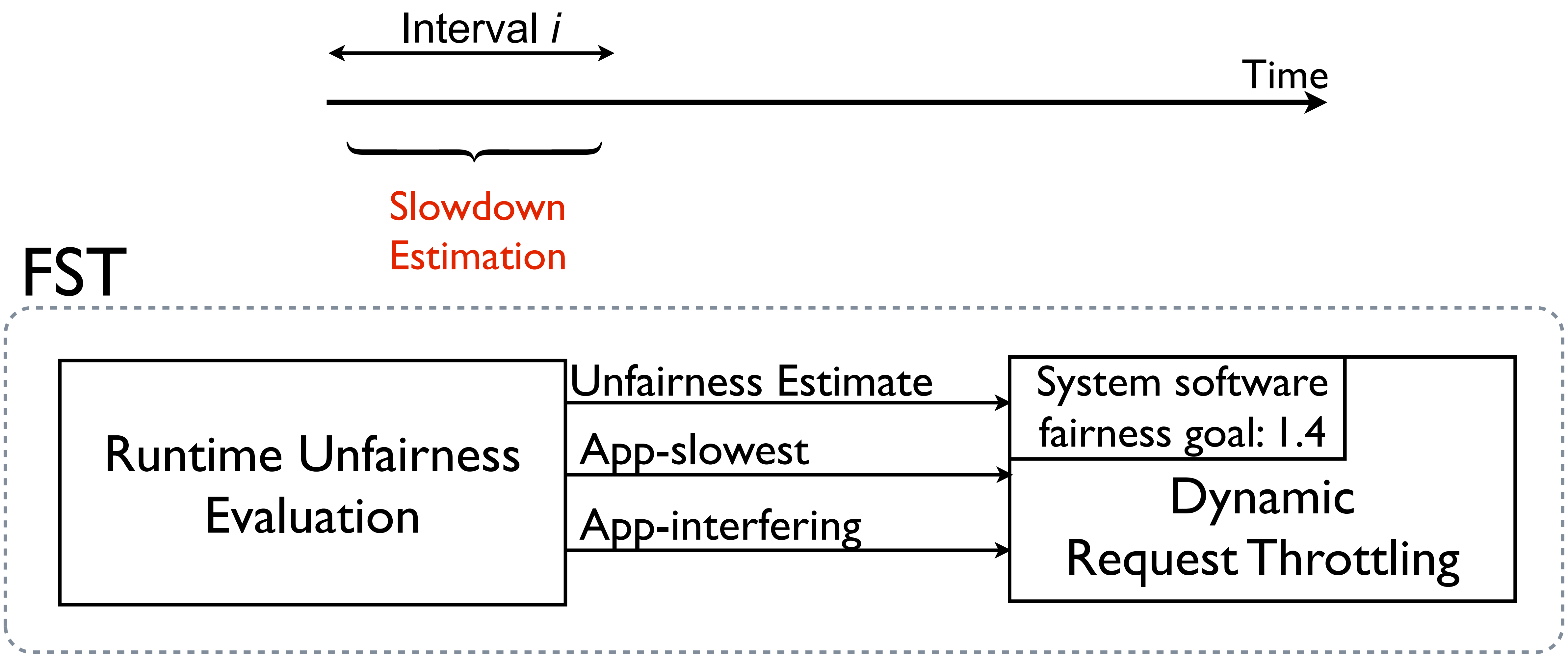
FST at Work


Interval *i*
Time
Slowdown
Estimation
FST
Runtime Unfairness Evaluation
Unfairness Estimate
App-slowest
App-interfering
System software fairness goal: 1.4
Dynamic Request Throttling

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1				
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate

App-slowest

App-interfering

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Dynamic Request Throttling

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1				
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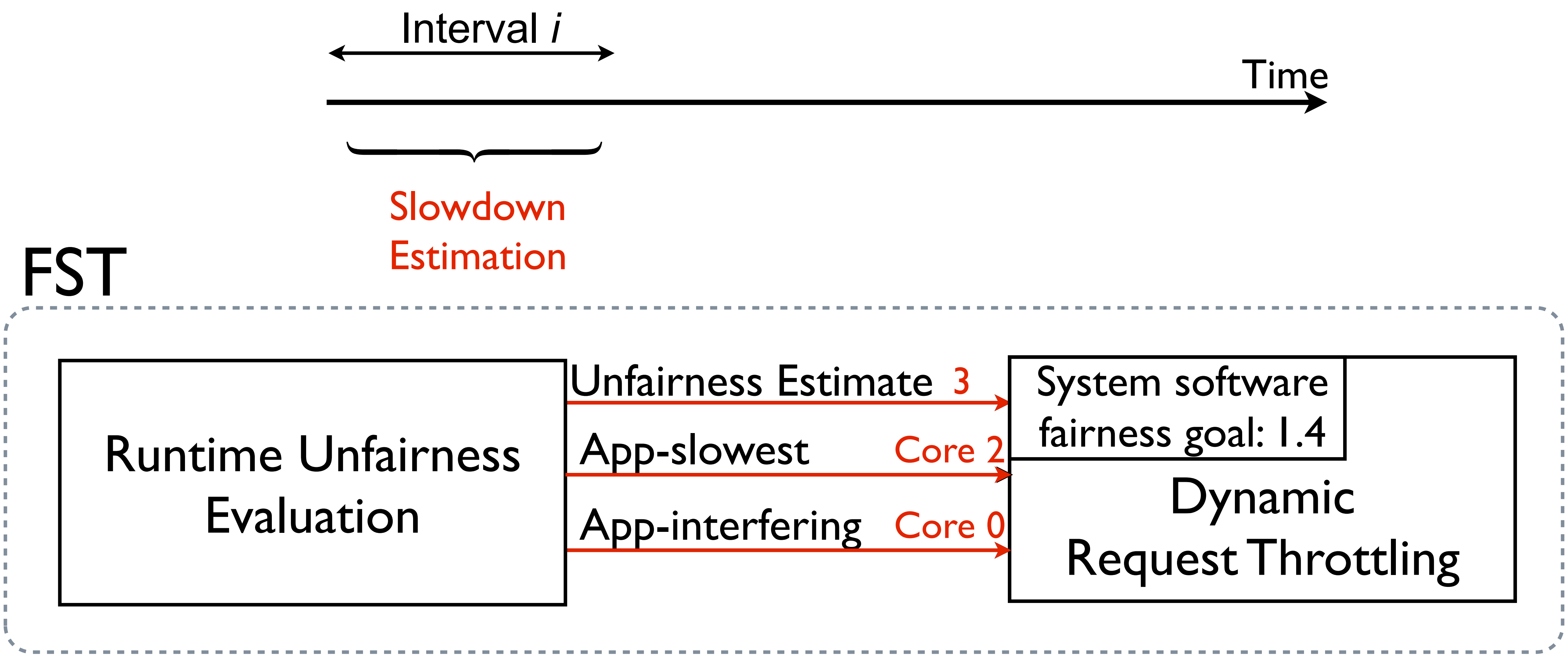
Throttling Levels

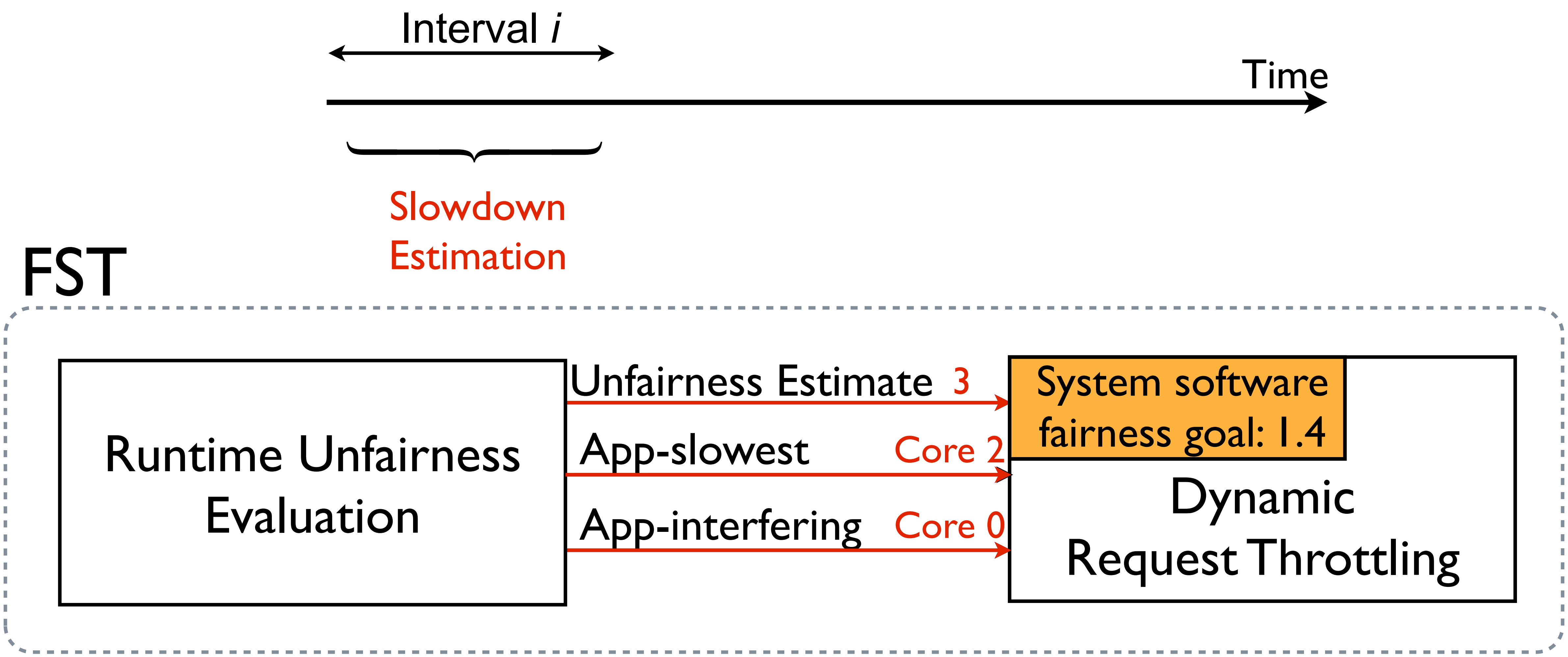
FST at Work



	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1				
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate 3

App-slowest Core 2

App-interfering Core 0

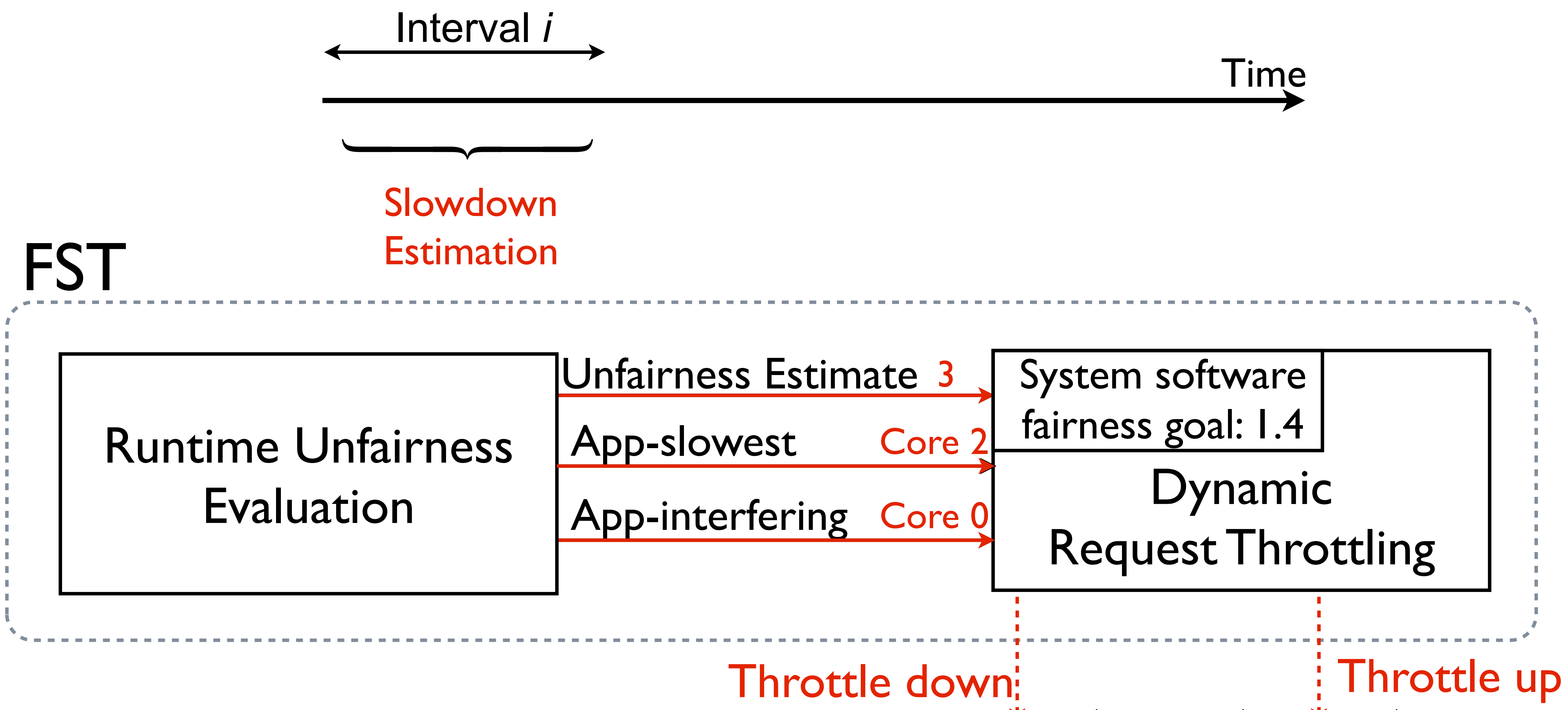
System software fairness goal: 1.4

Dynamic Request Throttling

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1				
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate 3

App-slowest Core 2

App-interfering Core 0

System software fairness goal: 1.4

Dynamic Request Throttling

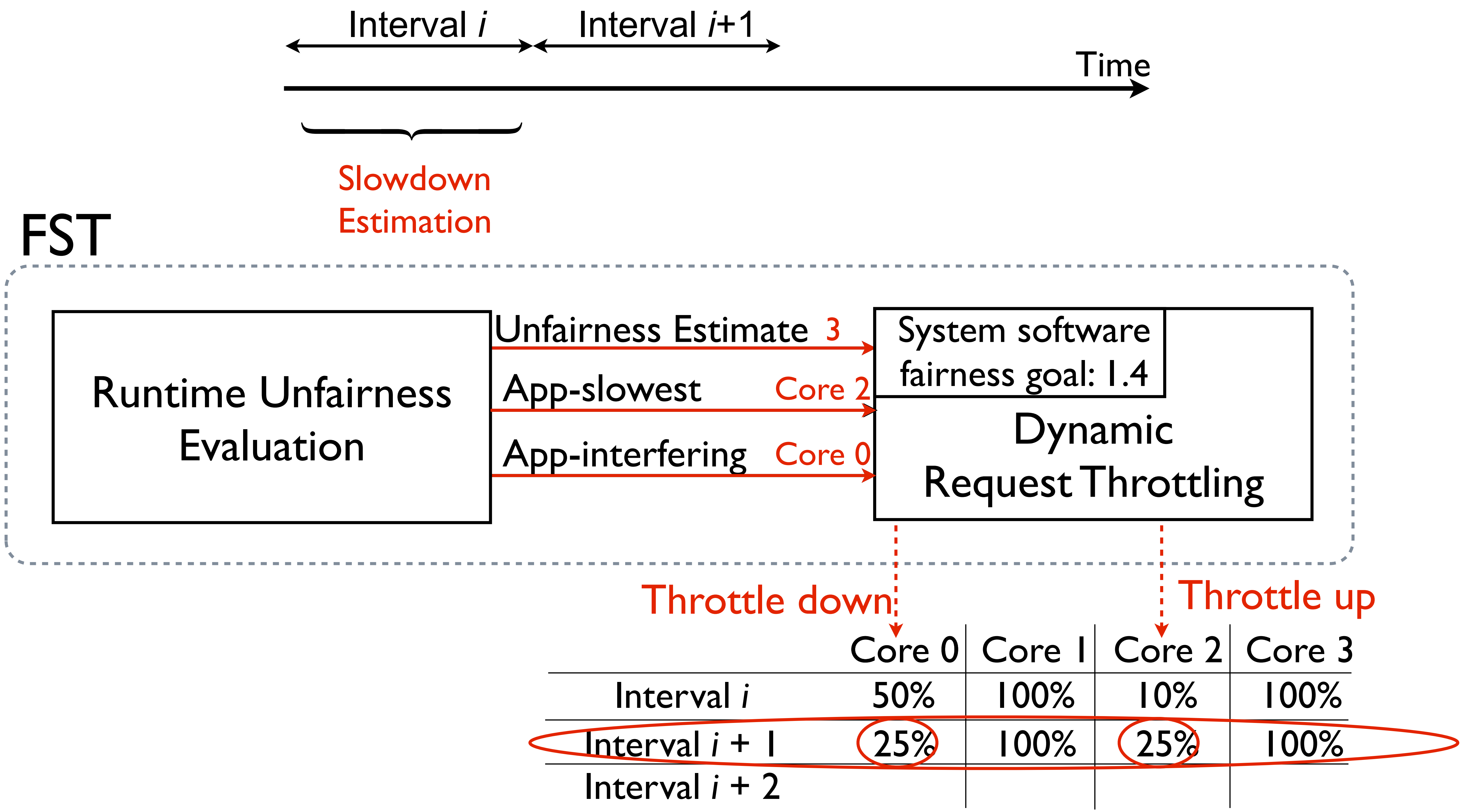
Throttle down

Throttle up

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1				
Interval *i* + 2				

Throttling Levels

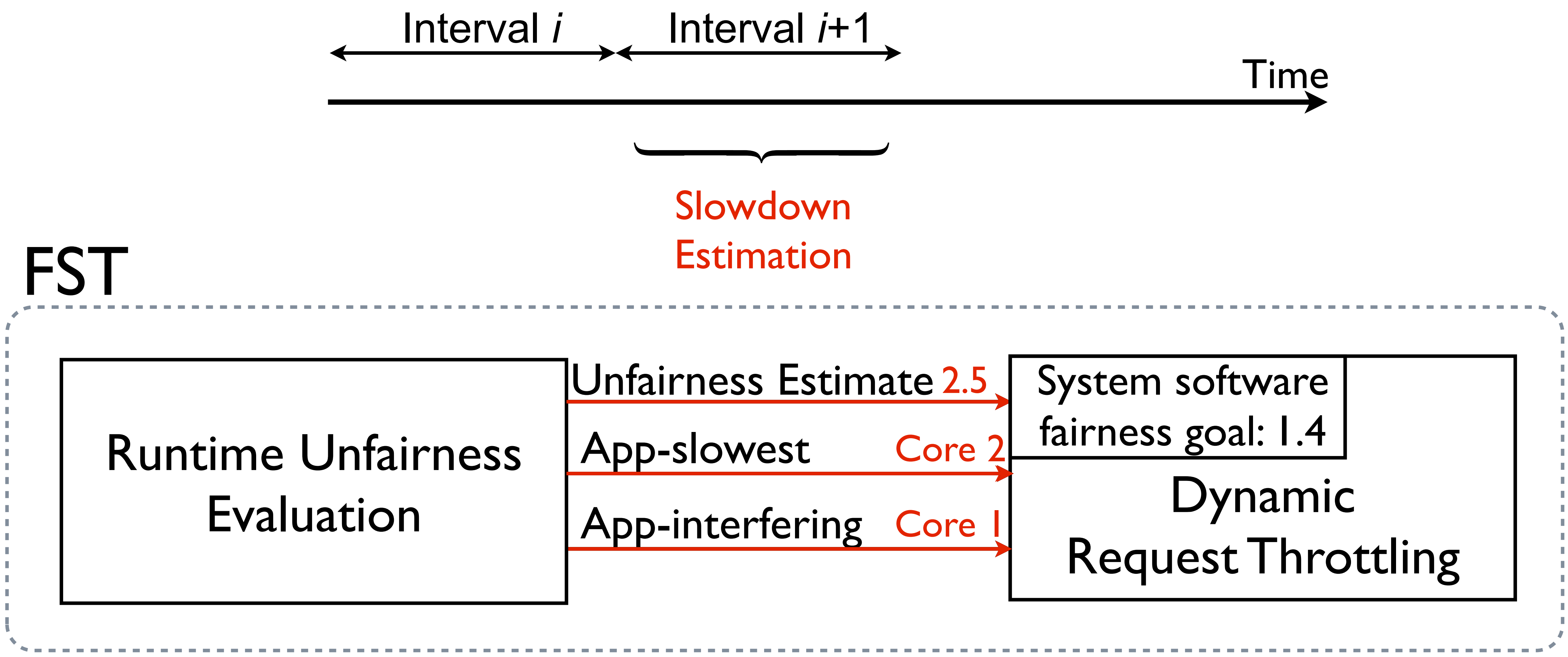
FST at Work



	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1	25%	100%	25%	100%
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Interval *i*+1

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate 2.5

App-slowest Core 2

App-interfering Core 1

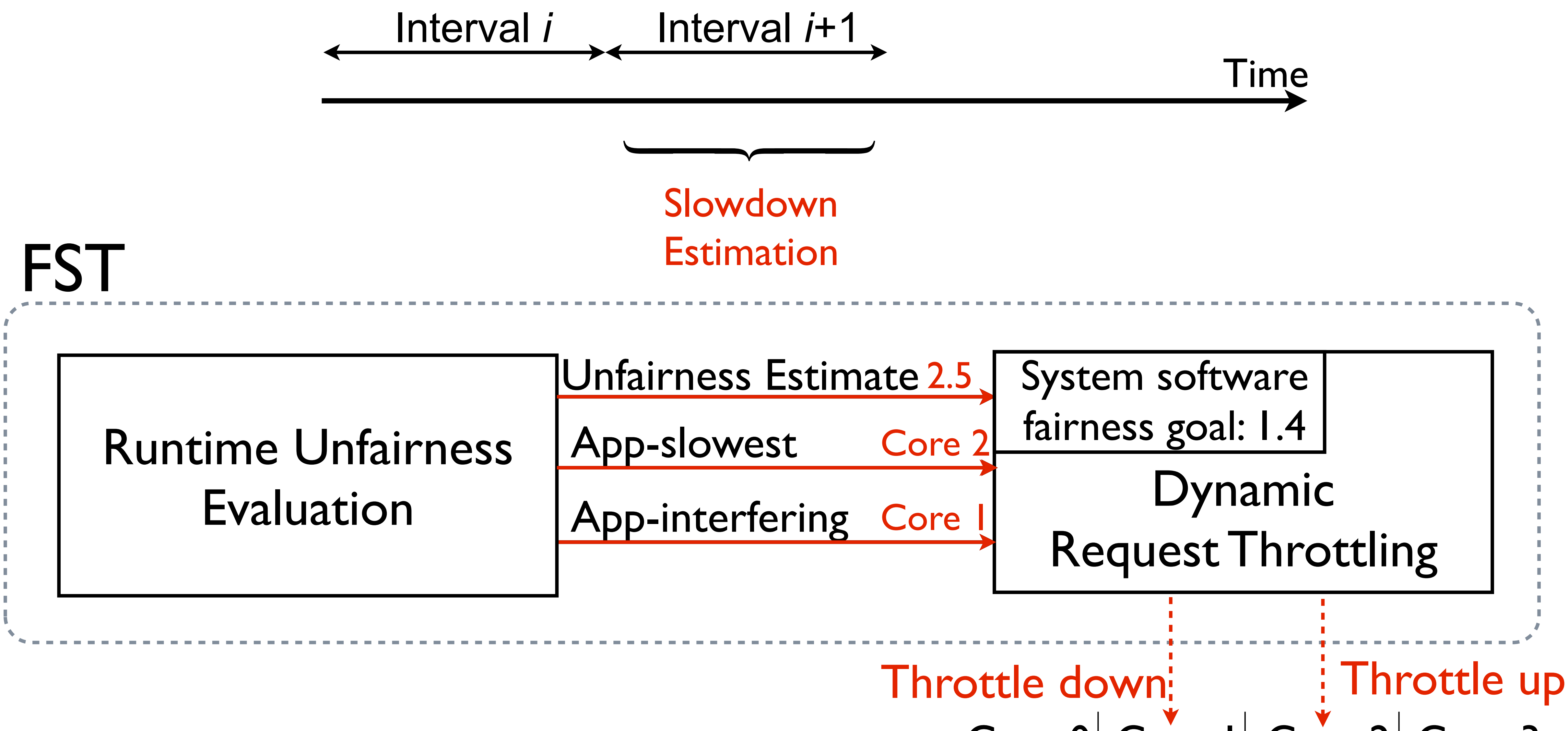
System software fairness goal: 1.4

Dynamic Request Throttling

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1	25%	100%	25%	100%
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Interval *i*+1

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate 2.5

App-slowest Core 2

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System software fairness goal: 1.4

Dynamic Request Throttling

Throttle down

Throttle up

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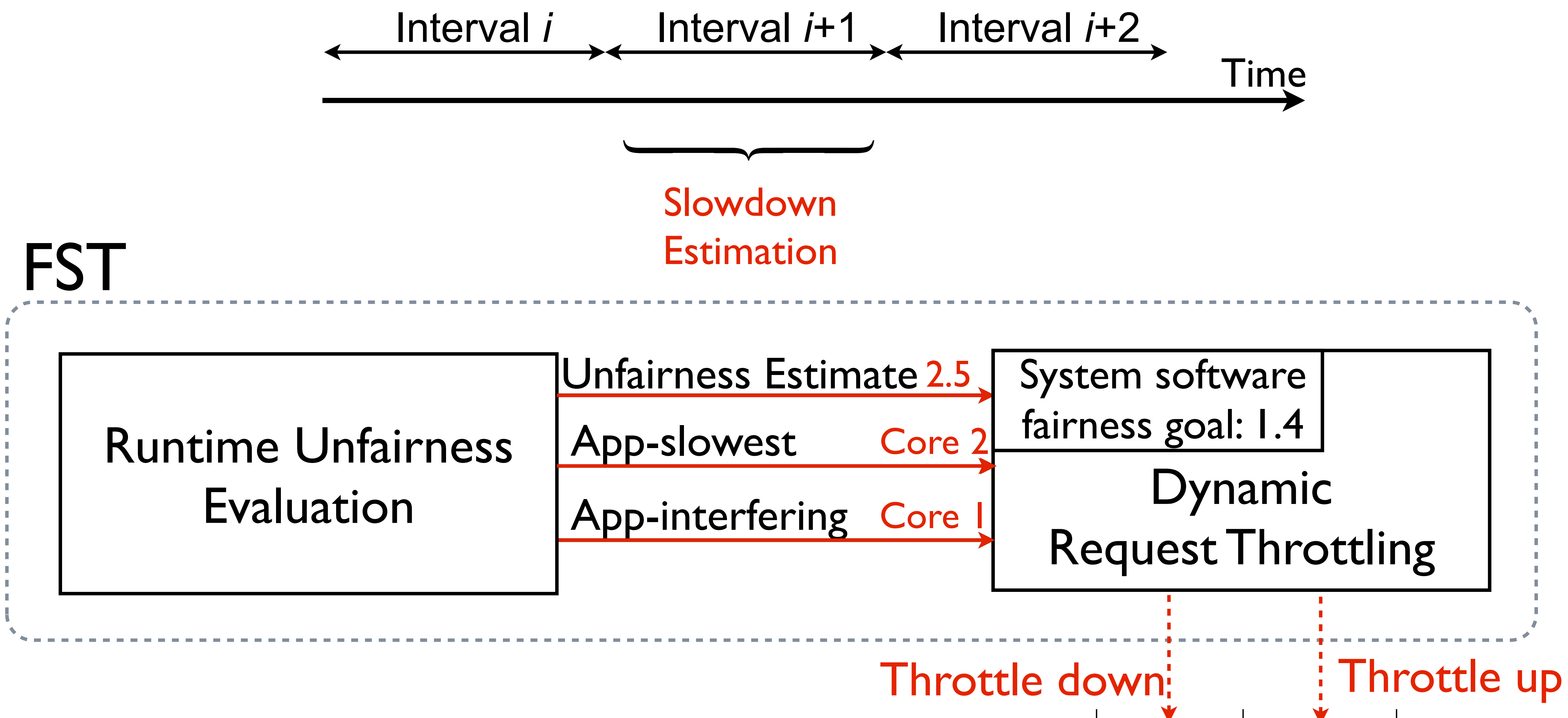
Interval *i* + 1	25%	100%	25%	100%
Interval *i* + 2				

Throttling Levels

FST at Work



Interval *i*

Interval *i*+1

Interval *i*+2

Time

Slowdown Estimation

FST

Runtime Unfairness Evaluation

Unfairness Estimate 2.5

App-slowest Core 2

App-interfering Core 1

System software fairness goal: 1.4

Dynamic Request Throttling

Throttle down

Throttle up

	Core 0	Core 1	Core 2	Core 3
Interval *i*	50%	100%	10%	100%
Interval *i* + 1	25%	100%	25%	100%
Interval *i* + 2	25%	50%	50%	100%

Throttling Levels

System Software Support

System Software Support

- Different fairness objectives can be configured by system software

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  - *Estimated Unfairness > Target Unfairness*

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  - *Estimated Max Slowdown > Target Max Slowdown*
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- Support for thread priorities

System Software Support

- Different fairness objectives can be configured by system software
  - *Estimated Unfairness > Target Unfairness*
  - *Estimated Max Slowdown > Target Max Slowdown*
  - *Estimated Slowdown(i) > Target Slowdown(i)*

- Support for thread priorities
  - *Weighted Slowdown(i) =*
    Estimated Slowdown(i) x Weight(i)

Hardware Cost

- Total storage cost required for 4 cores is ~ 12KB

- FST does not require any structures or logic that are on the processor's critical path

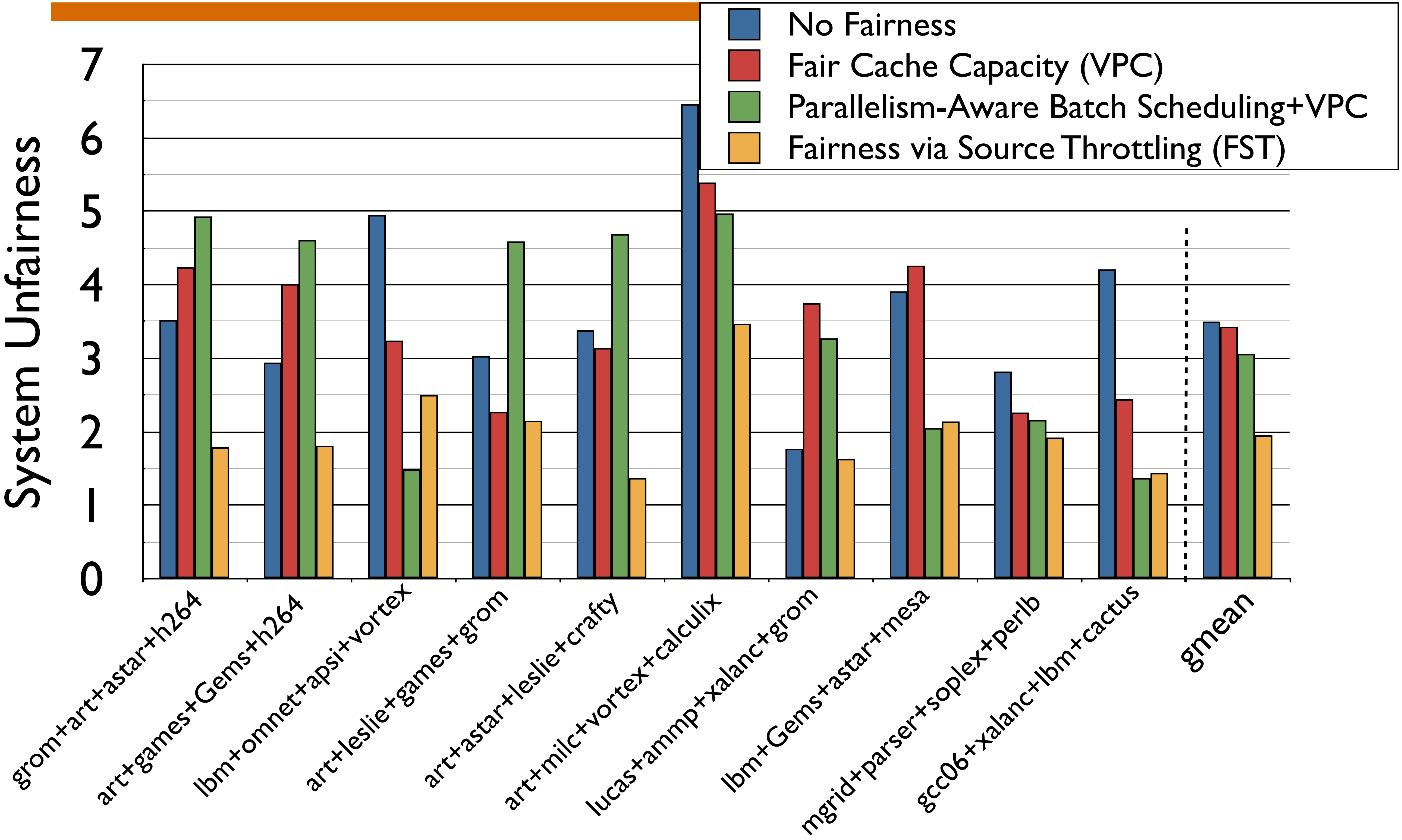
Outline

- Background and Problem
- Motivation for Source Throttling
- Fairness via Source Throttling (FST)
- Evaluation
- Conclusion

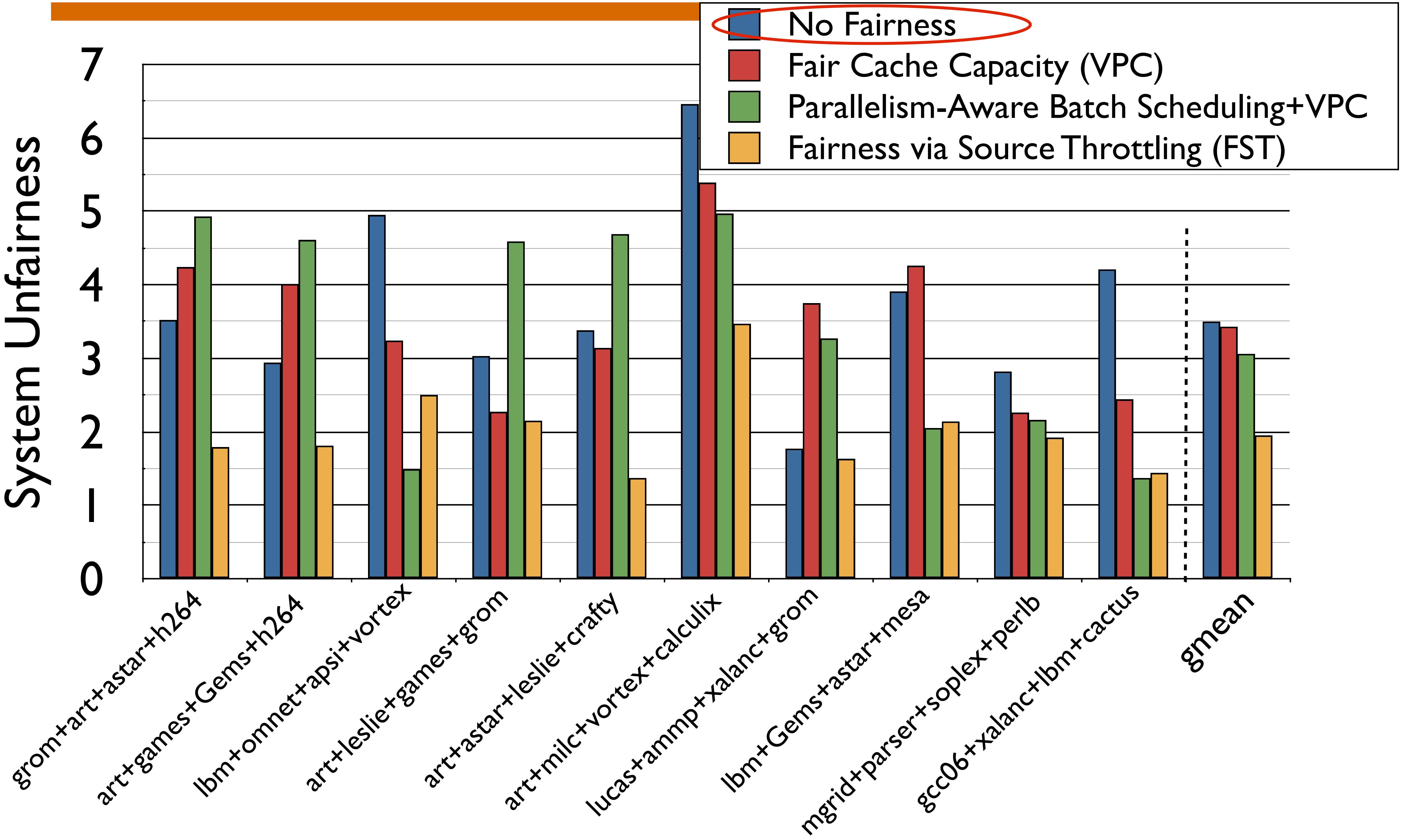
Evaluation Methodology

- x86 cycle accurate simulator
- Baseline processor configuration
  - Per-core
    - 4-wide issue, out-of-order, 256 entry ROB
  - Shared (4-core system)
    - 128 MSHRs
    - 2 MB, 16-way L2 cache
  - Main Memory
    - DDR3 1333 MHz
    - Latency of 15ns per command (*tRP, tRCD, CL*)
    - 8B wide core to memory bus

System Unfairness Results



System Unfairness Results



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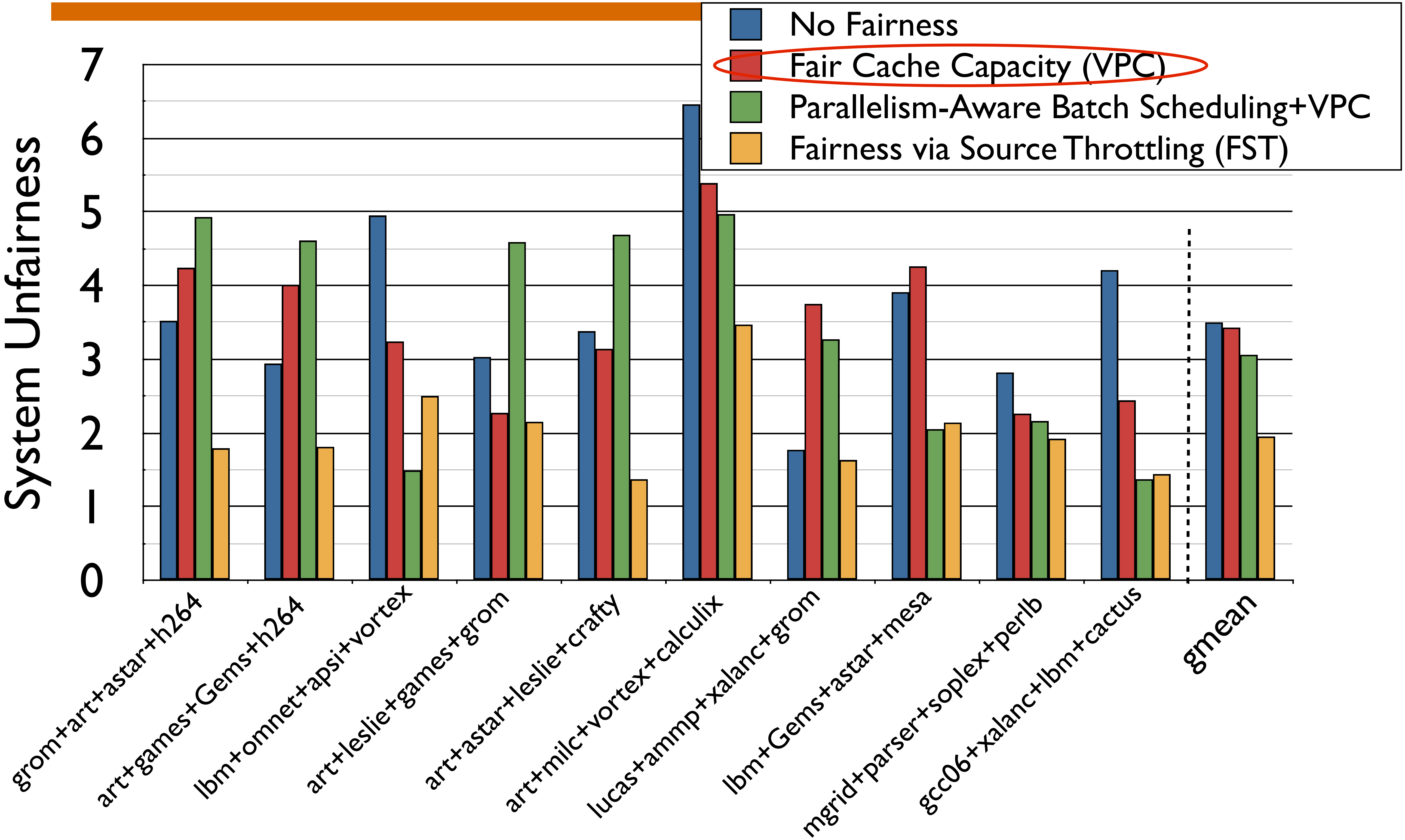

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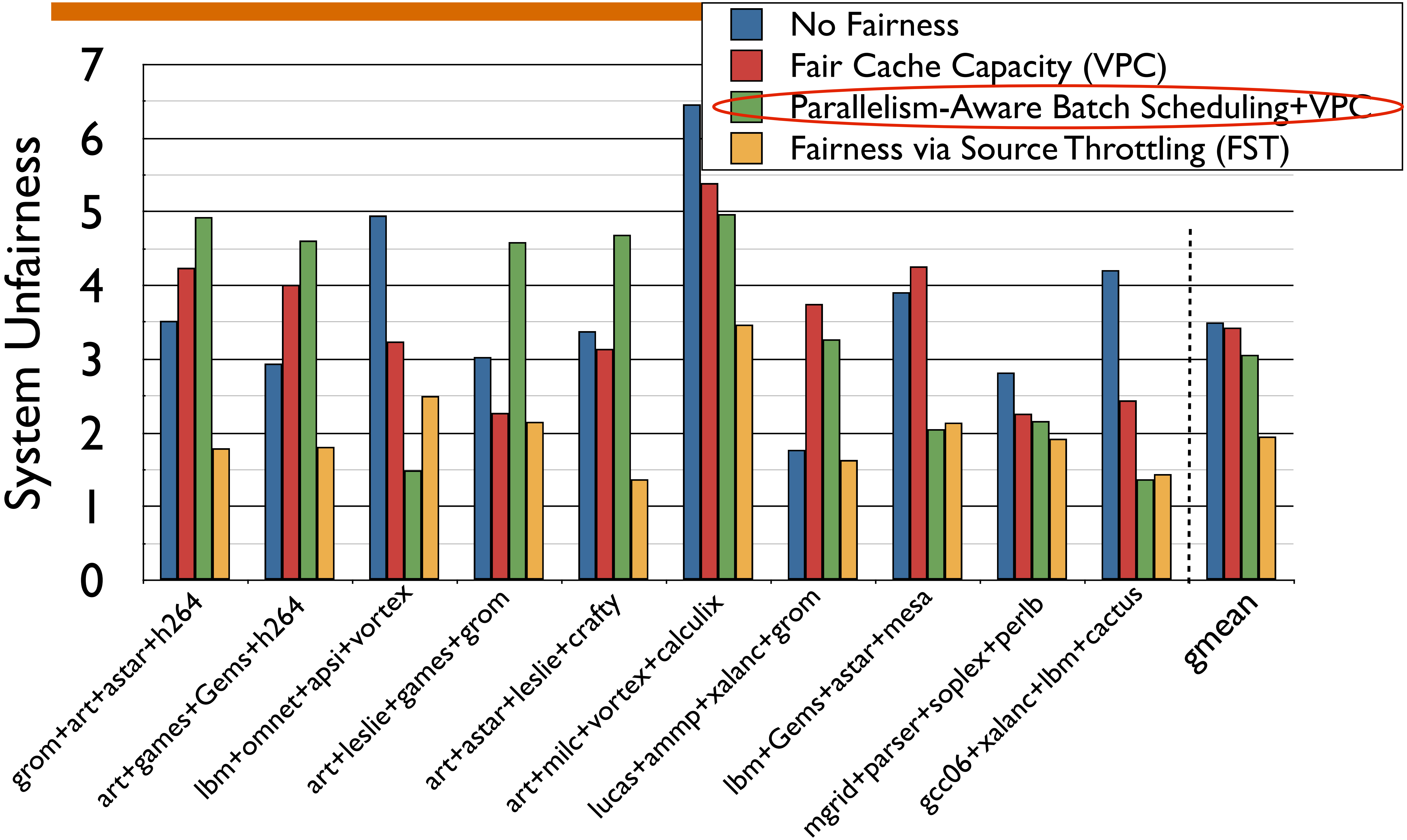

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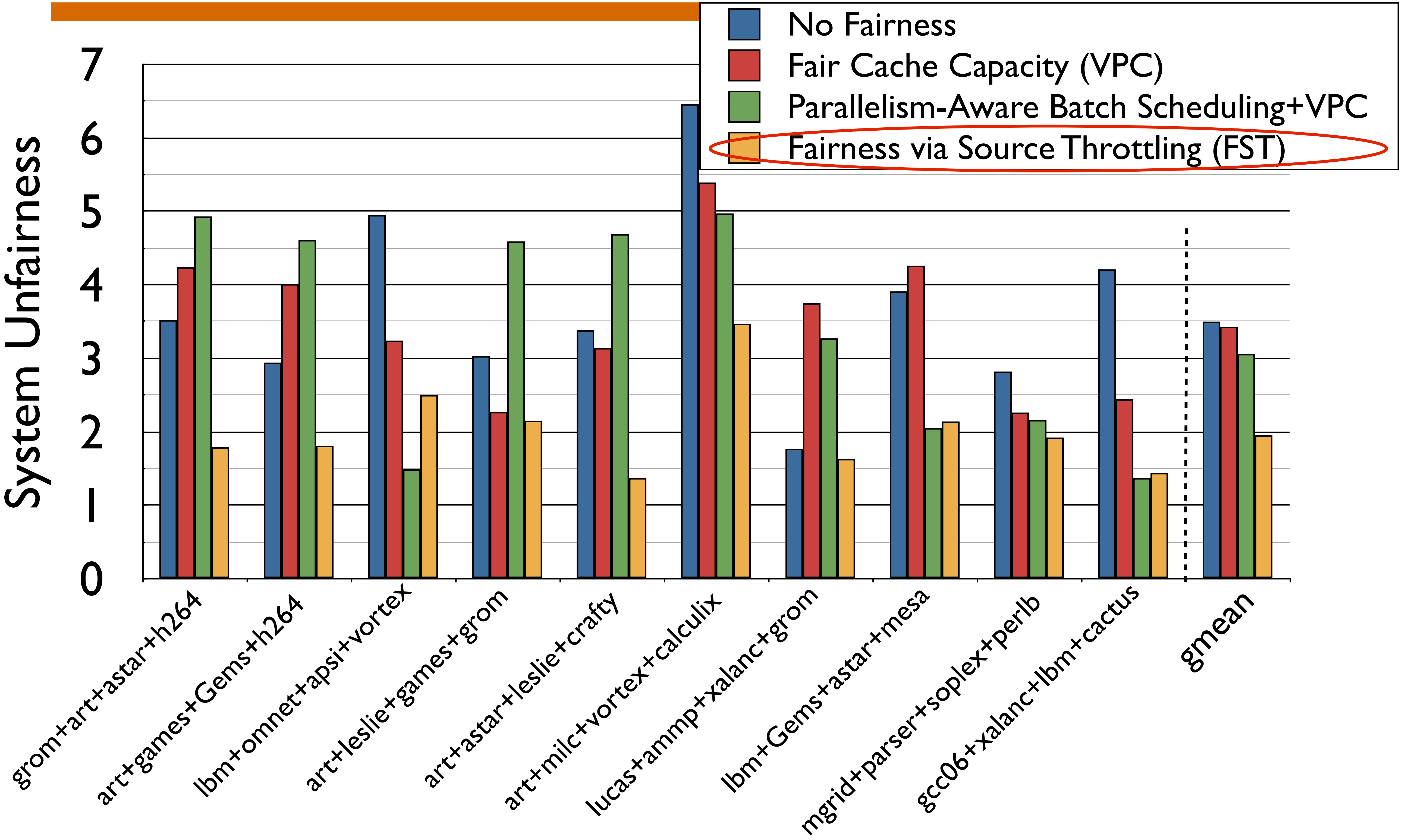

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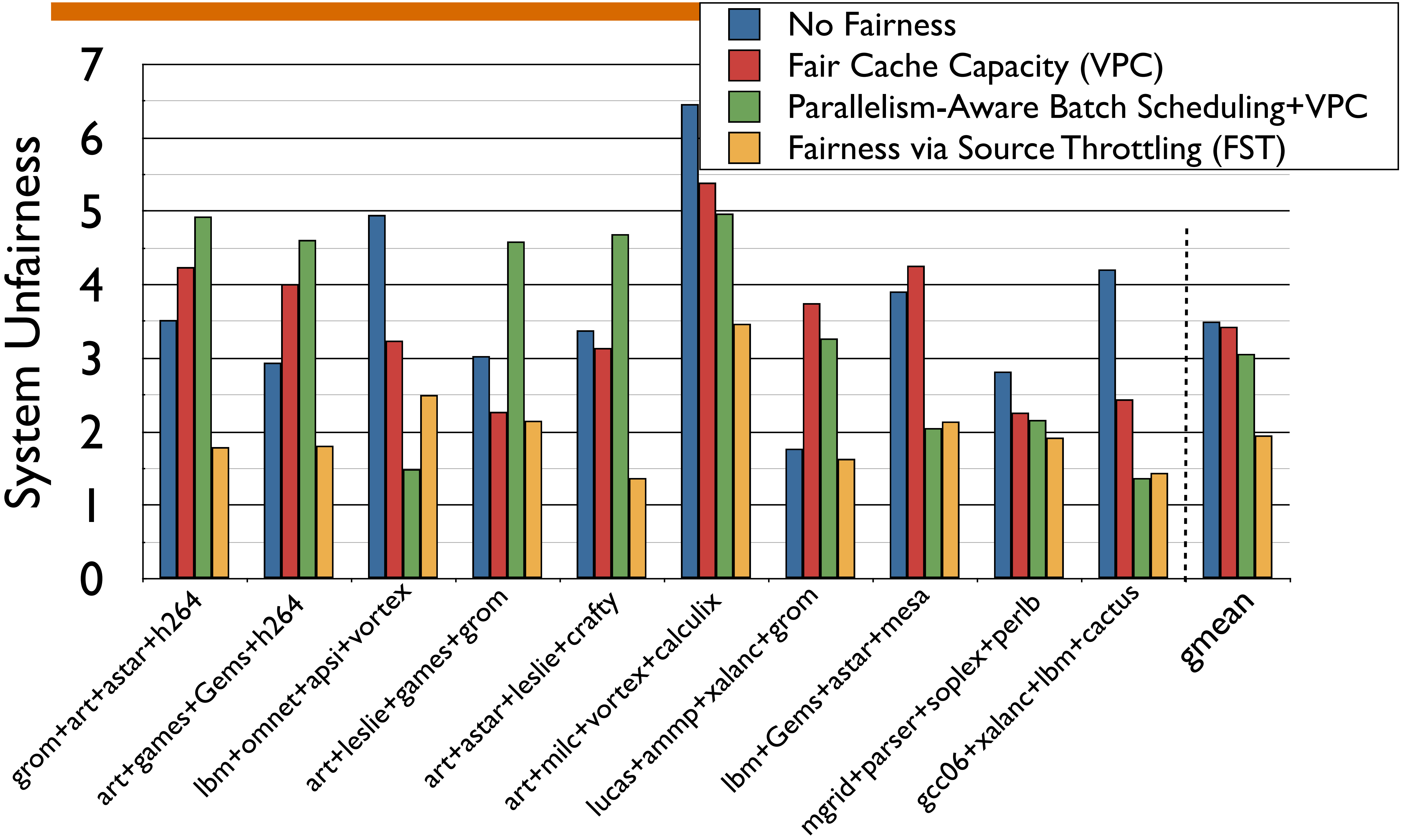

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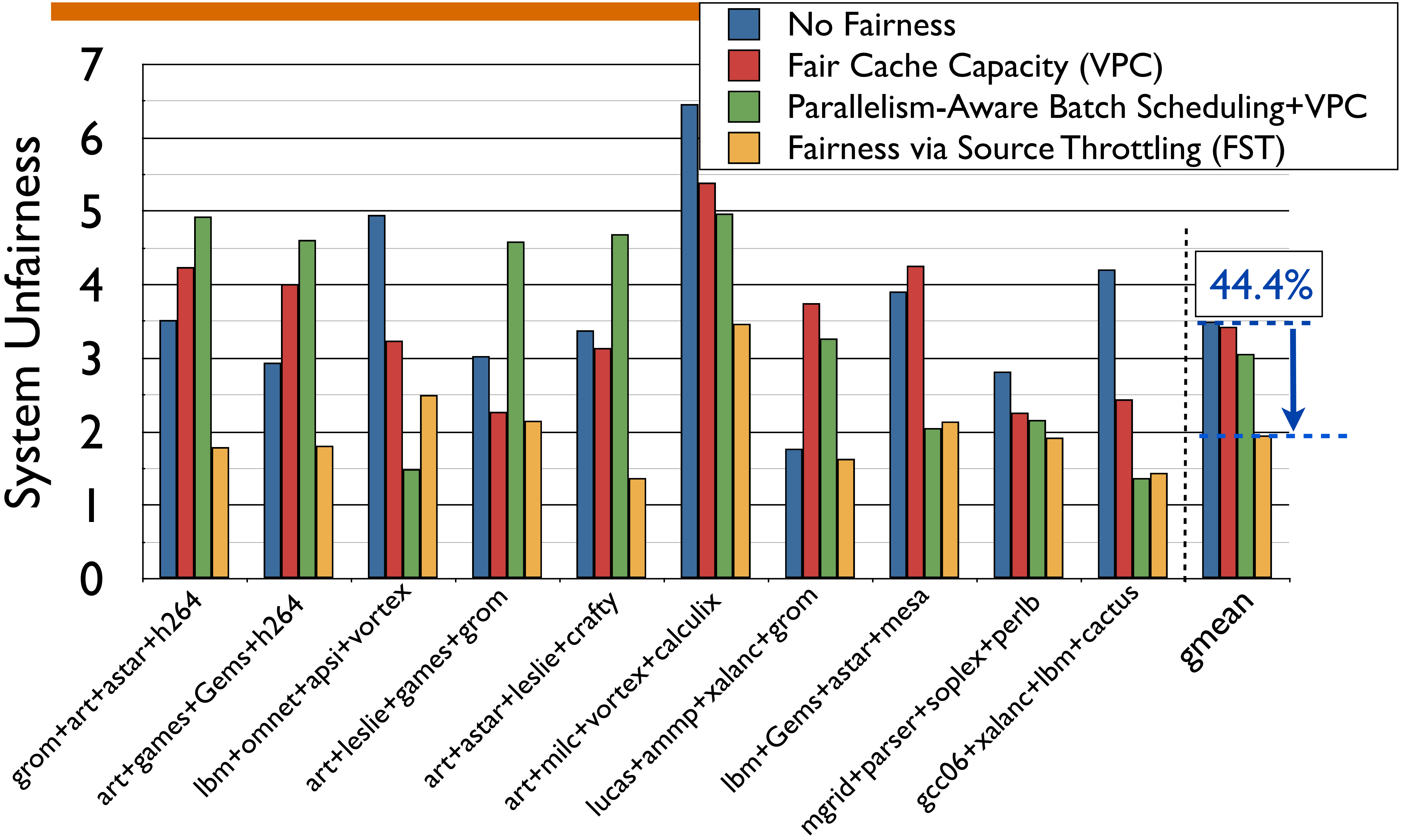

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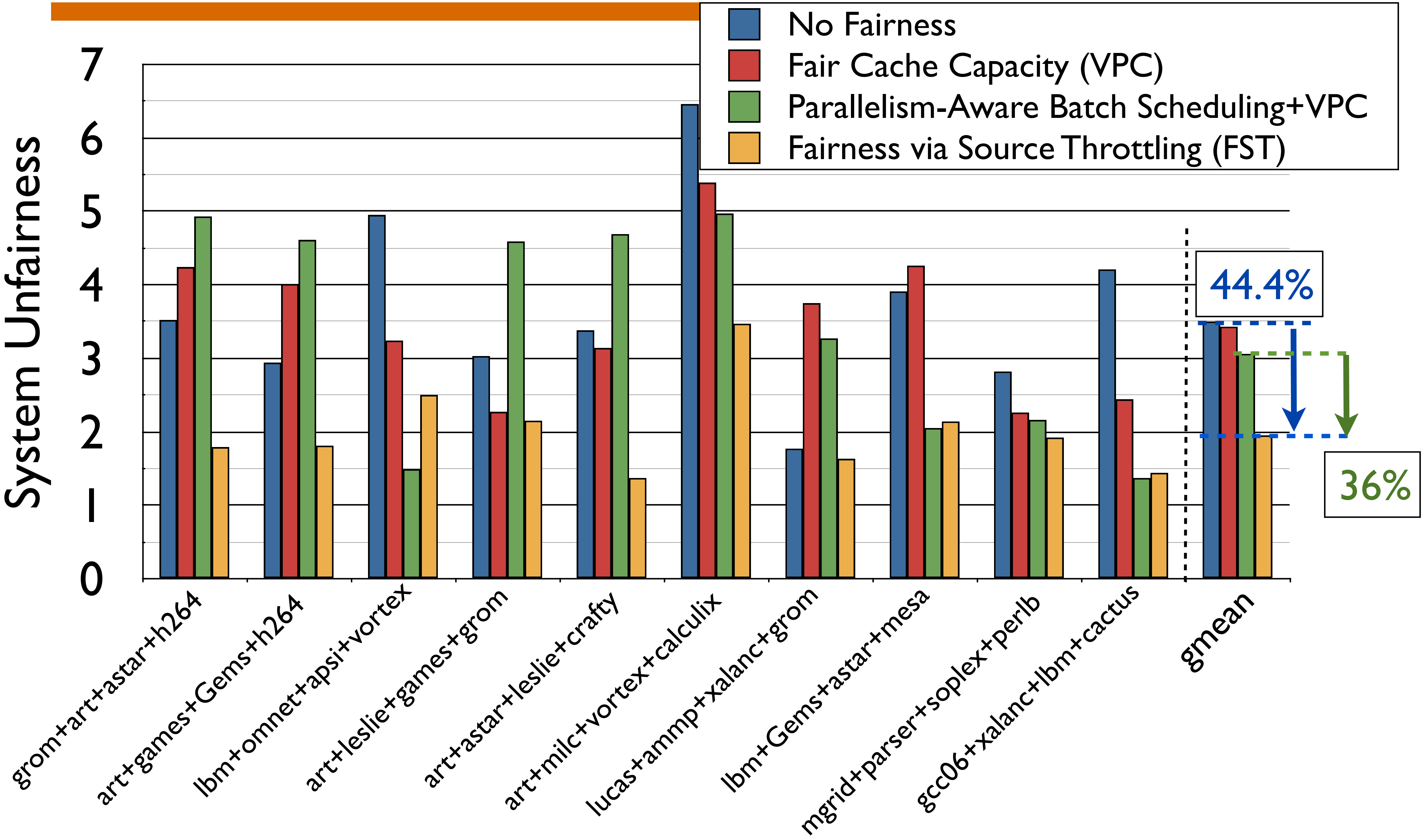
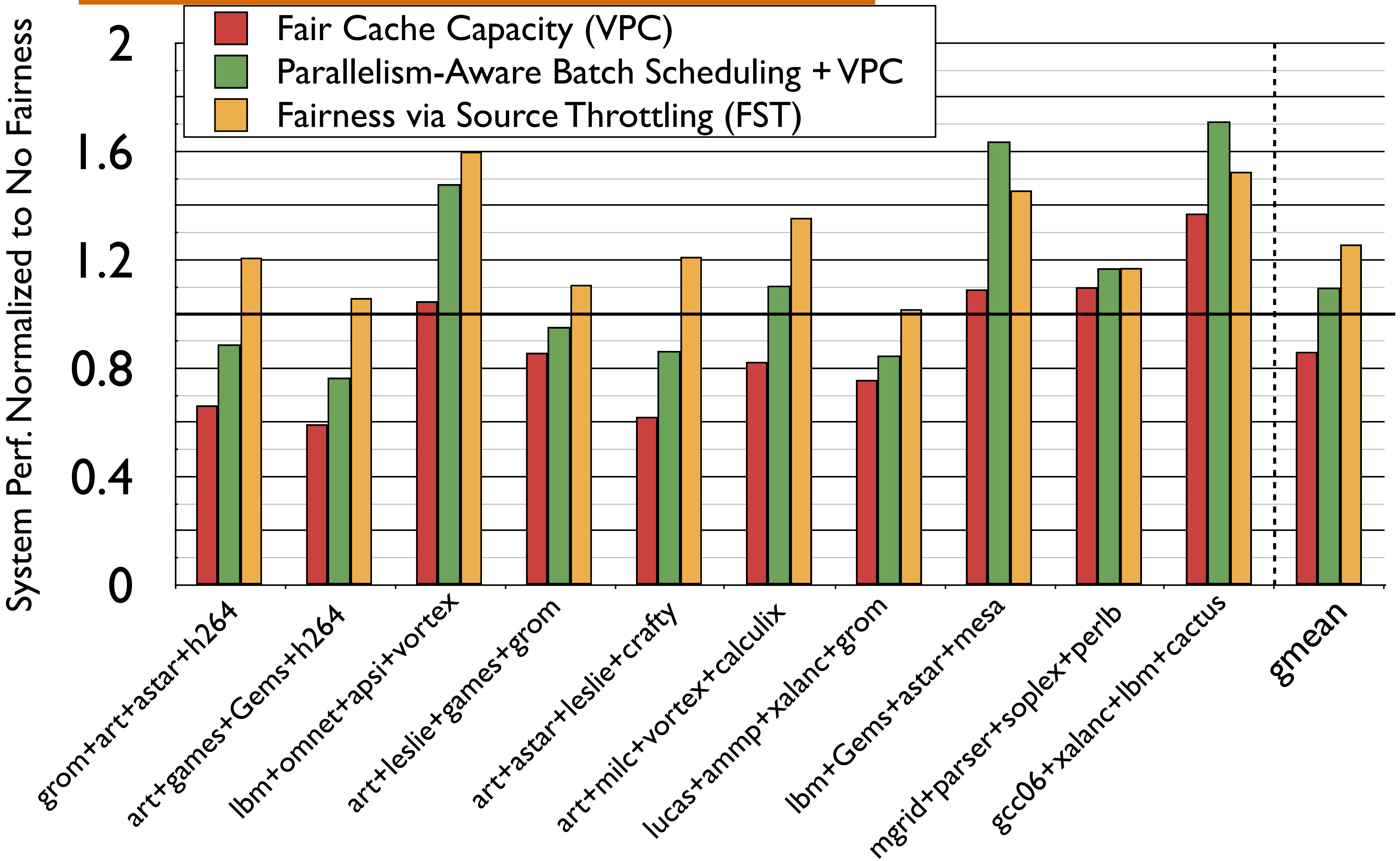


System Performance Results



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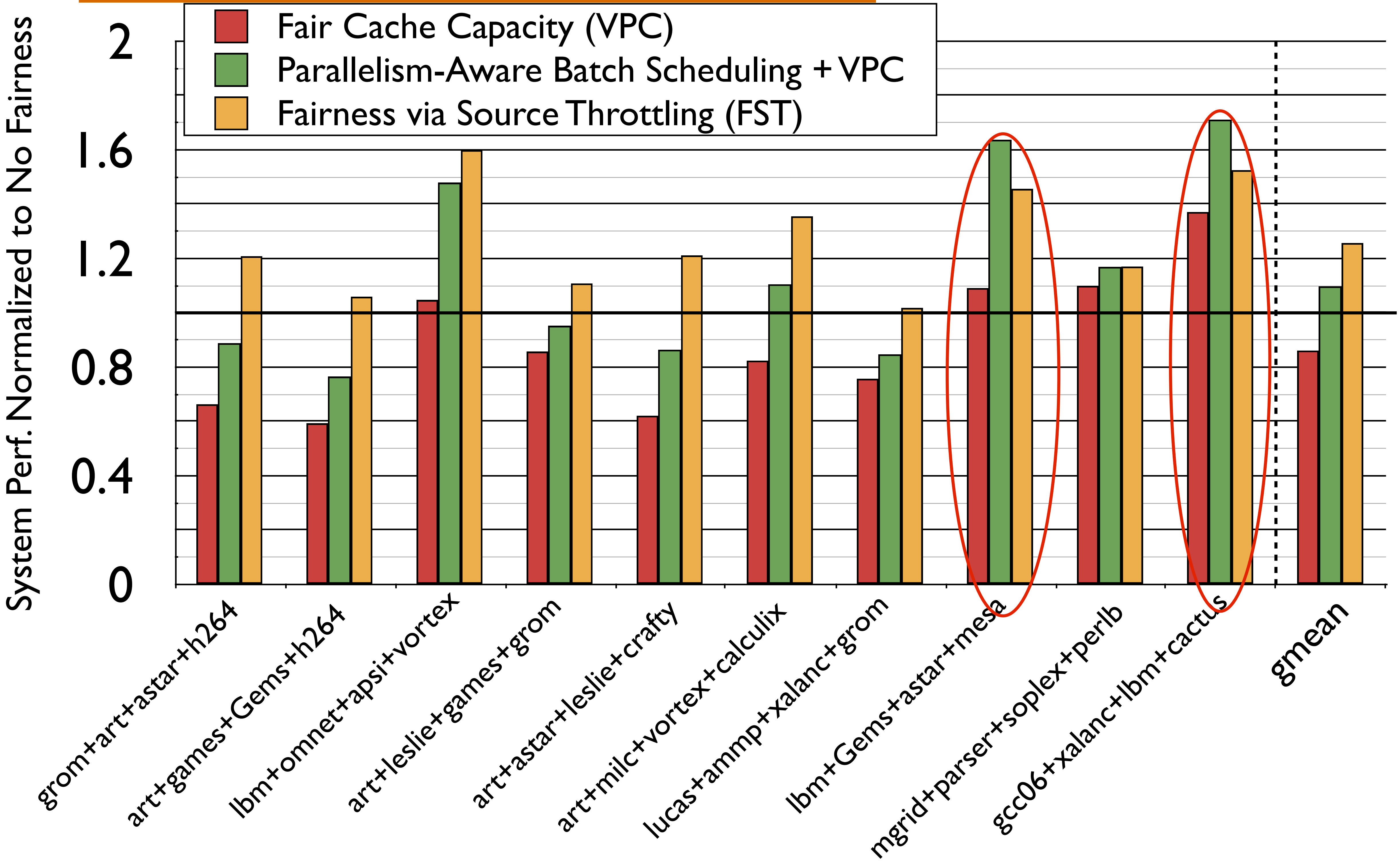
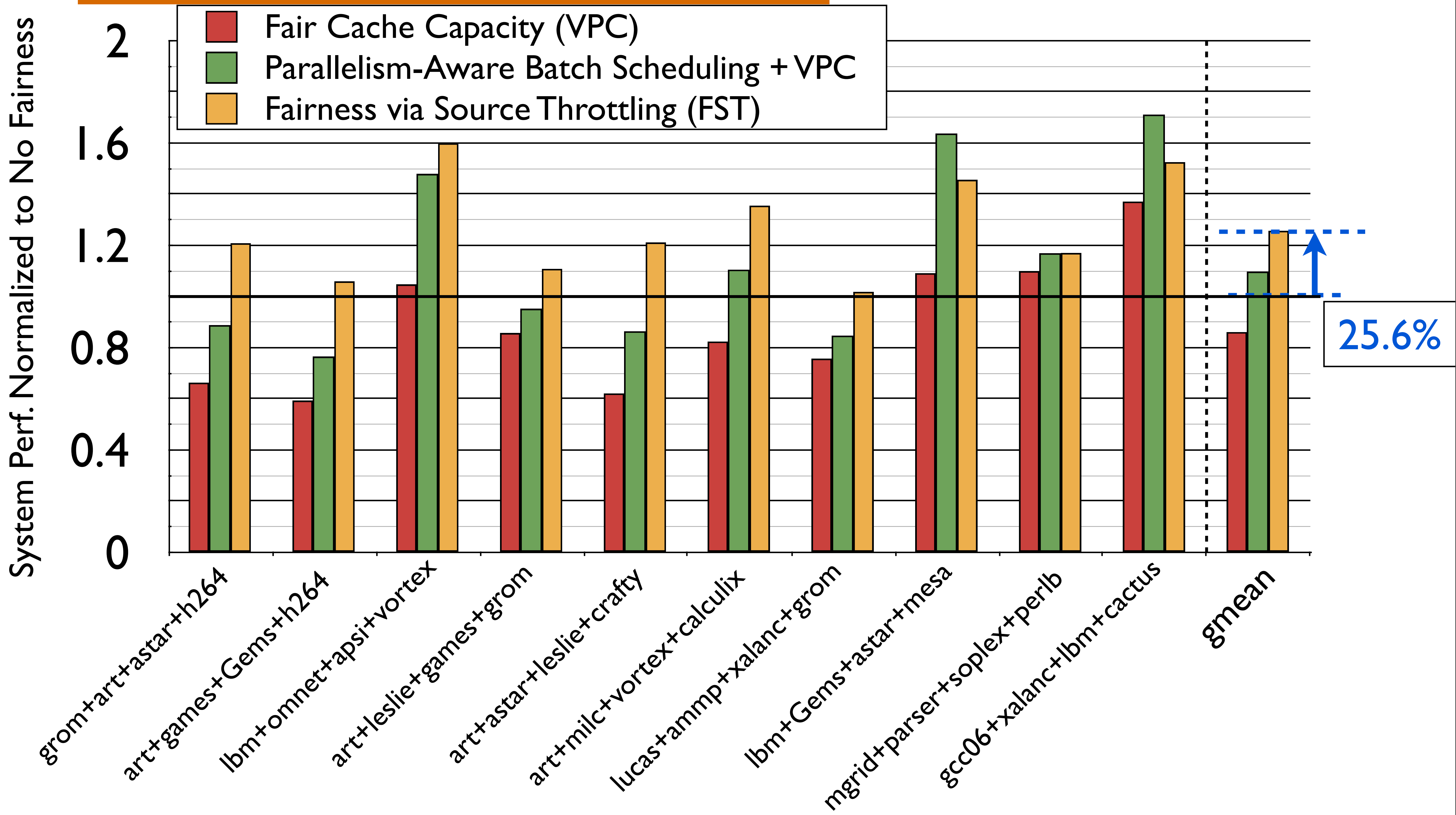
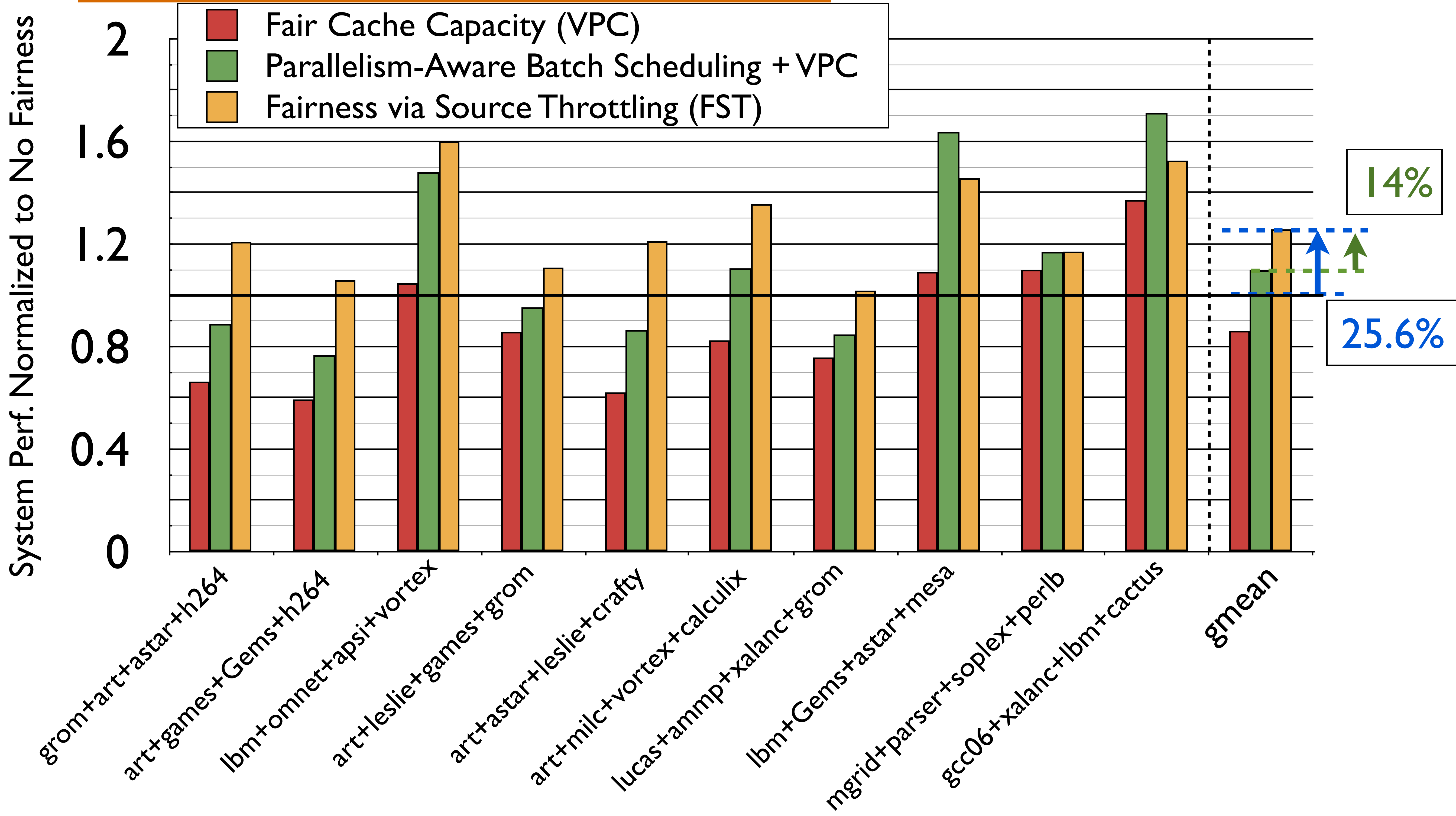


System Performance Results



System Performance Results



Conclusion

- Fairness via Source Throttling (FST) is a new fair and high-performance shared resource management approach for CMPs
- Dynamically monitors unfairness and throttles down sources of interfering memory requests
- Eliminates the need for and complexity of multiple per-resource fairness techniques
- Improves both system fairness and performance
- Incorporates thread weights and enables different fairness objectives

Fairness via Source Throttling:

A configurable and high-performance fairness substrate for multi-core memory systems

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Chang Joo Lee[*]

Onur Mutlu[‡]

Yale N. Patt[*]

[*] **HPS Research Group**
The University of Texas at Austin

[‡] **Computer Architecture Laboratory**
Carnegie Mellon University

Backups

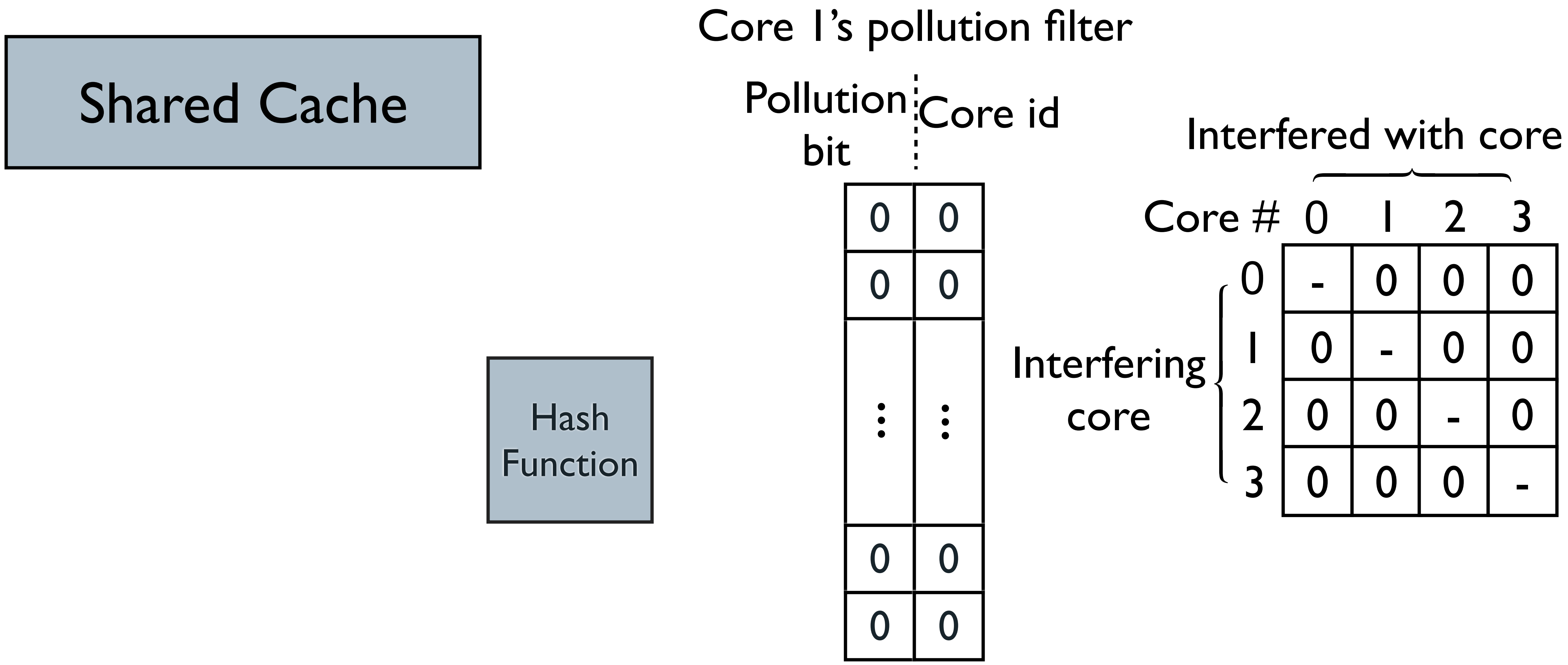
Other Source-Based Techniques

- Herdrich et. al. ICS ’09
Rate-based QoS techniques for cache/memory in CMP platforms
- Zhang et. al., USENIX ’09
Hardware execution throttling for multi-core resource management
- Jahre and Natvig, Computing Frontiers ’09
A light-weight fairness mechanism for chip multiprocessor memory systems

Interference-Aware Thread Scheduling

- Zhuravlev et. al. ASPLOS ’10
  Addressing Shared Resource Contention in Multicore Processors Via Scheduling
- Schedules applications which interfere less with each other as best as possible
- Advantages of FST:
  - □ The mix of apps may force co-scheduling of intensive applications
  - □ FST can make scheduling decisions easier for system software
- Advantages of using thread scheduling:
  - □ Does not require hardware support
- Approaches are complementary

Tracking Cache Interference



Shared Cache

Hash Function

Core 1's pollution filter

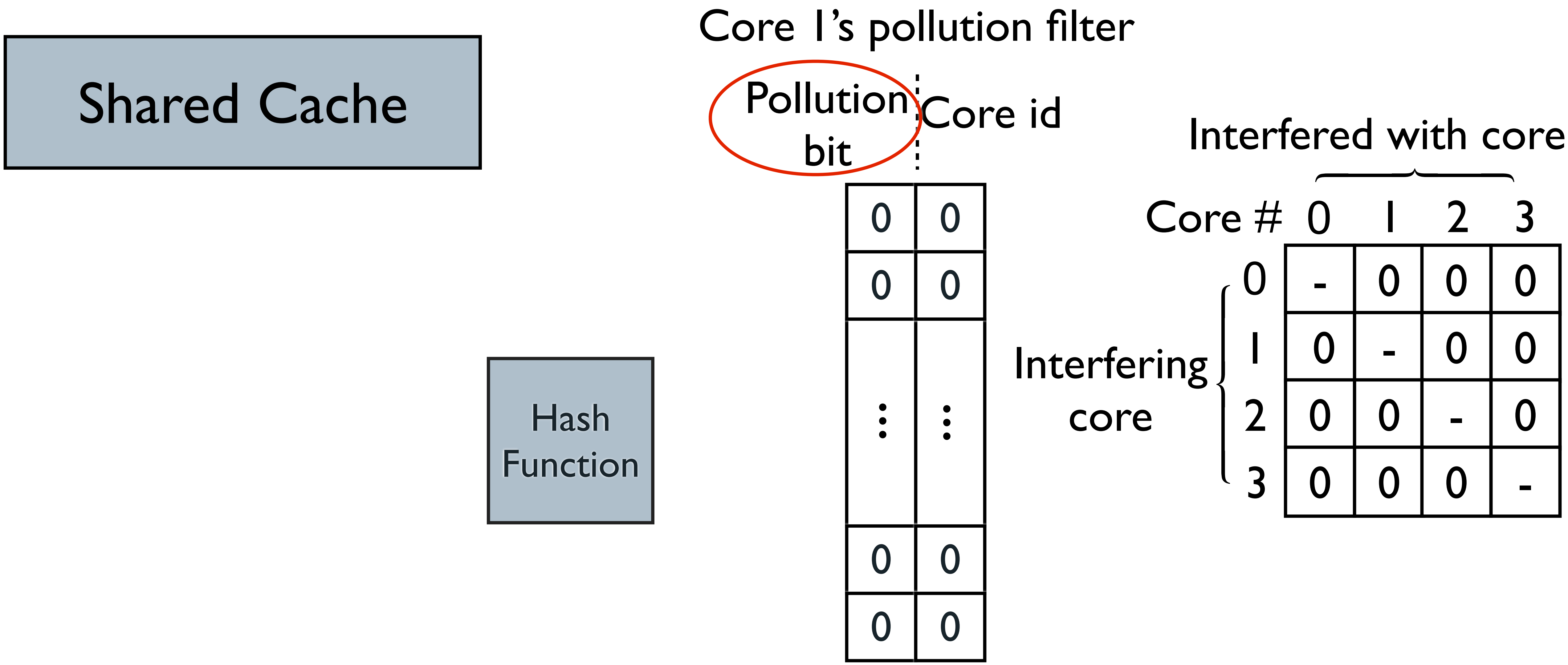
Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Shared Cache

Hash Function

Core 1's pollution filter

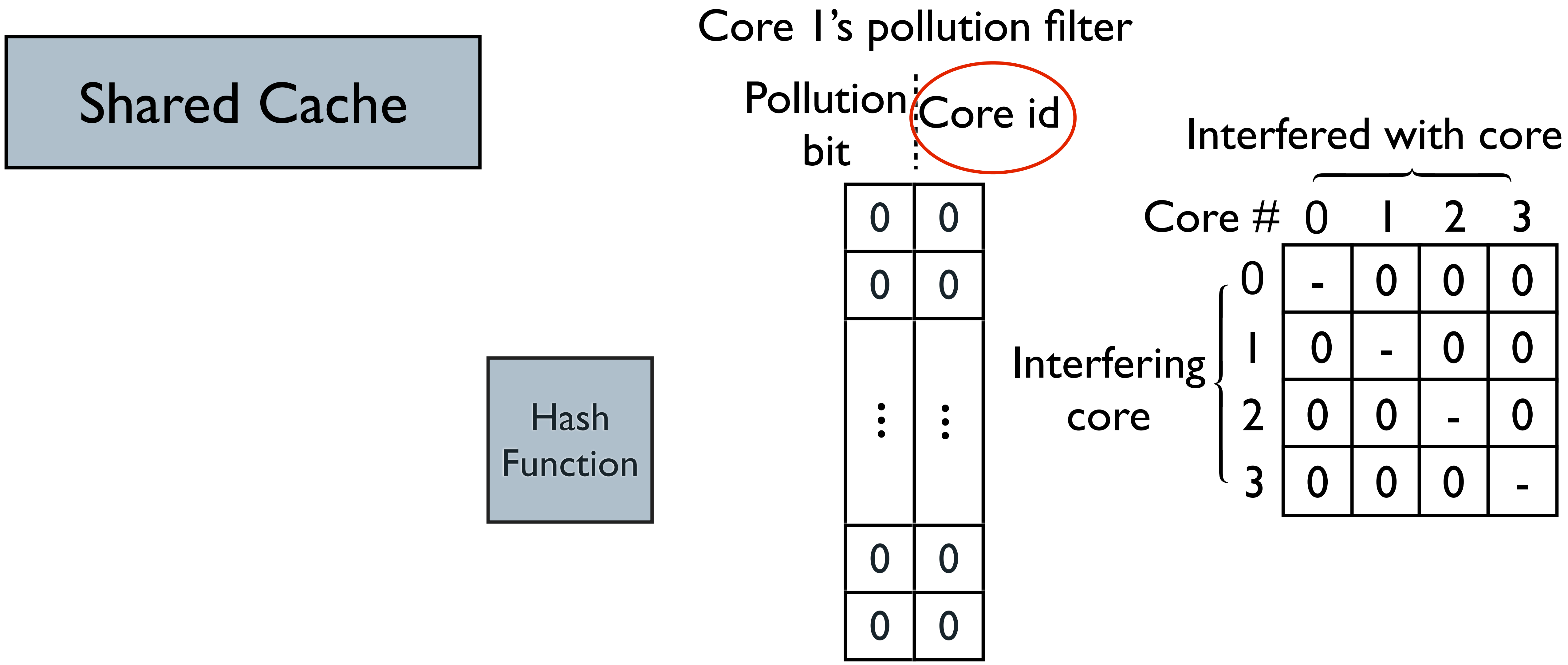
Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Shared Cache

Hash Function

Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference

Shared Cache

Hash Function

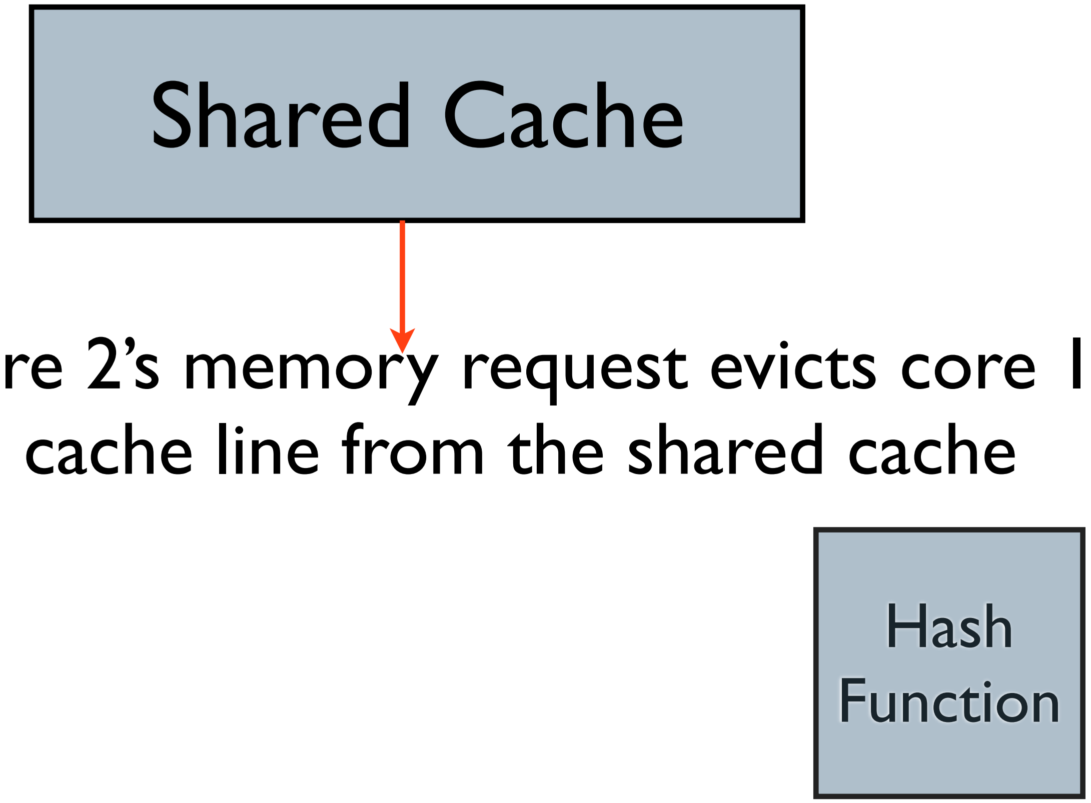
Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core	Core #	0	1	2	3
	0	-	0	0	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Tracking Cache Interference



Core 2's memory request evicts core 1's cache line from the shared cache

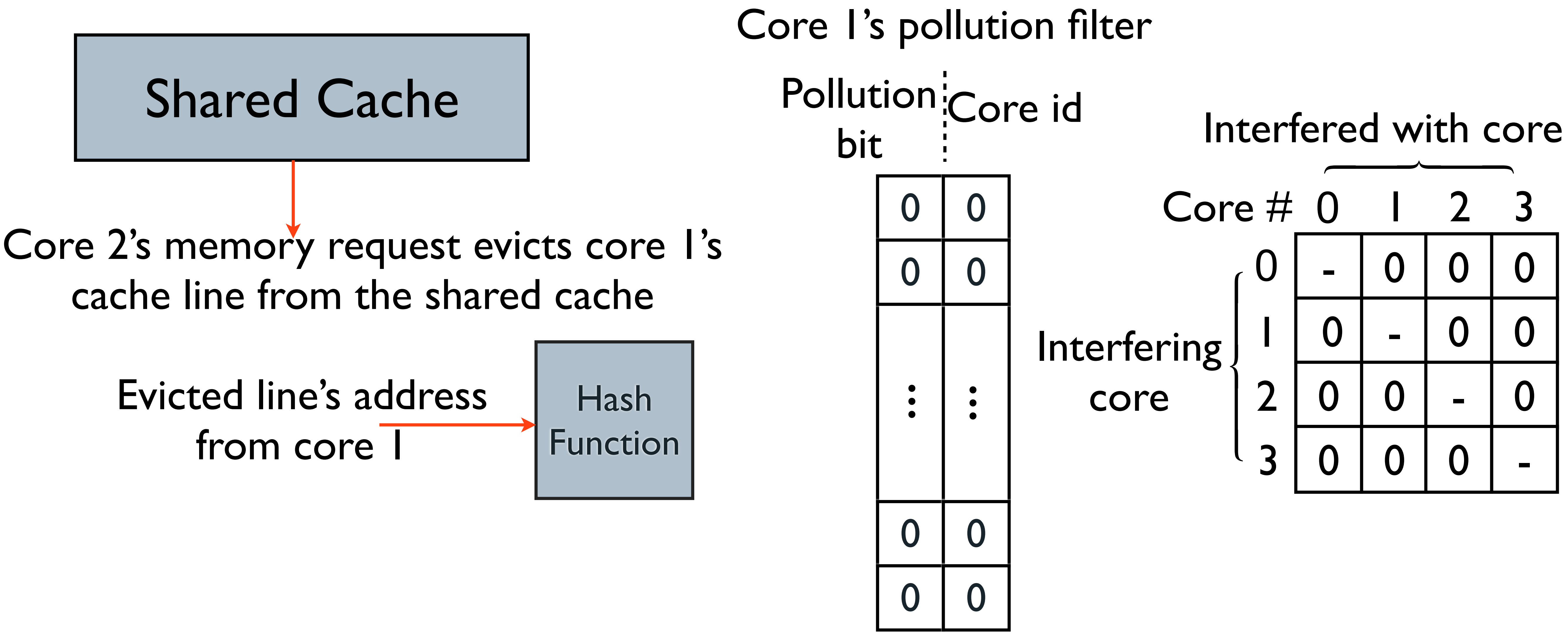
Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core	Core #	0	1	2	3
	0	-	0	0	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Tracking Cache Interference



Core 2's memory request evicts core 1's cache line from the shared cache

Evicted line's address from core 1

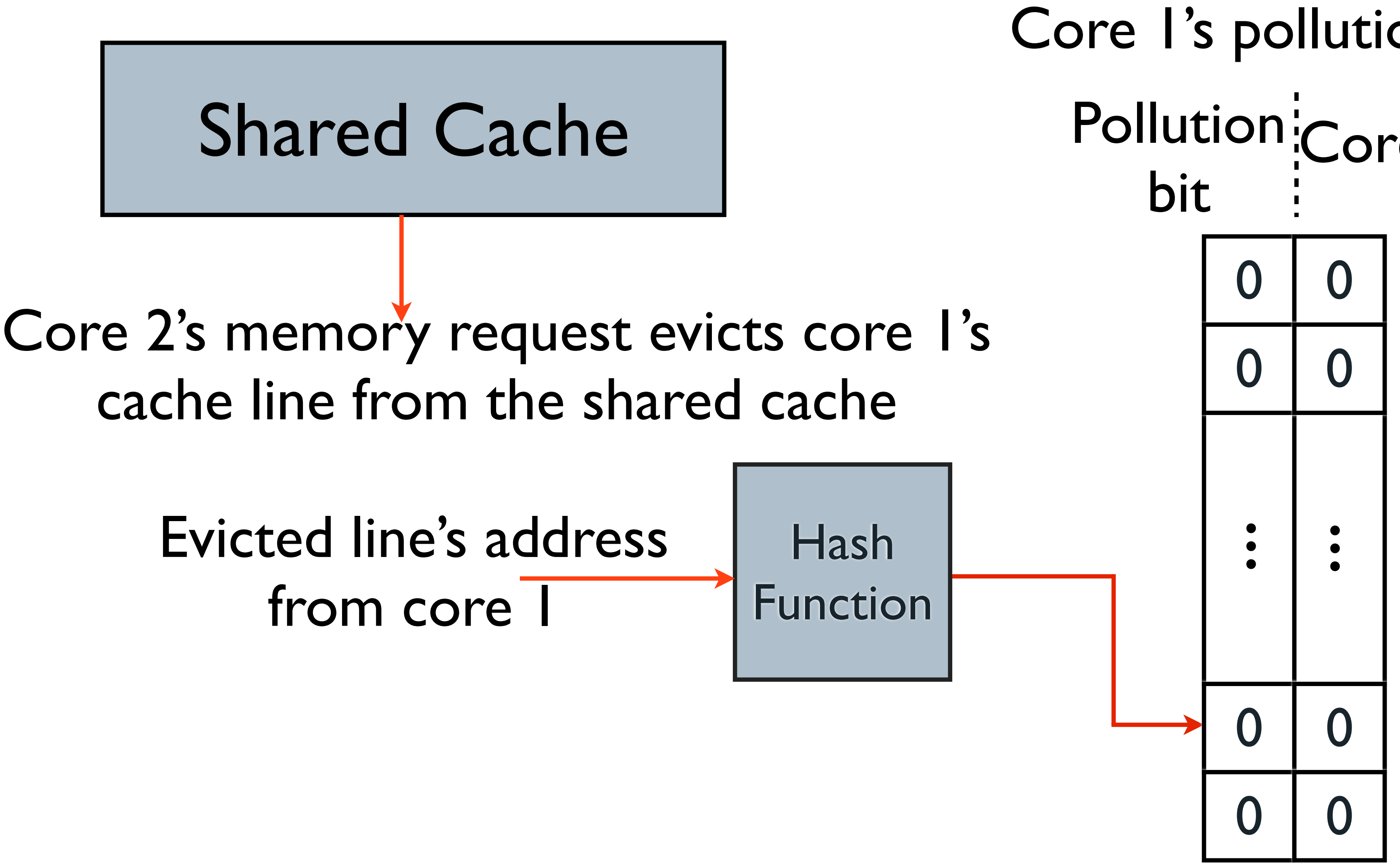
Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core / Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Core 2's memory request evicts core 1's cache line from the shared cache

Evicted line's address from core 1

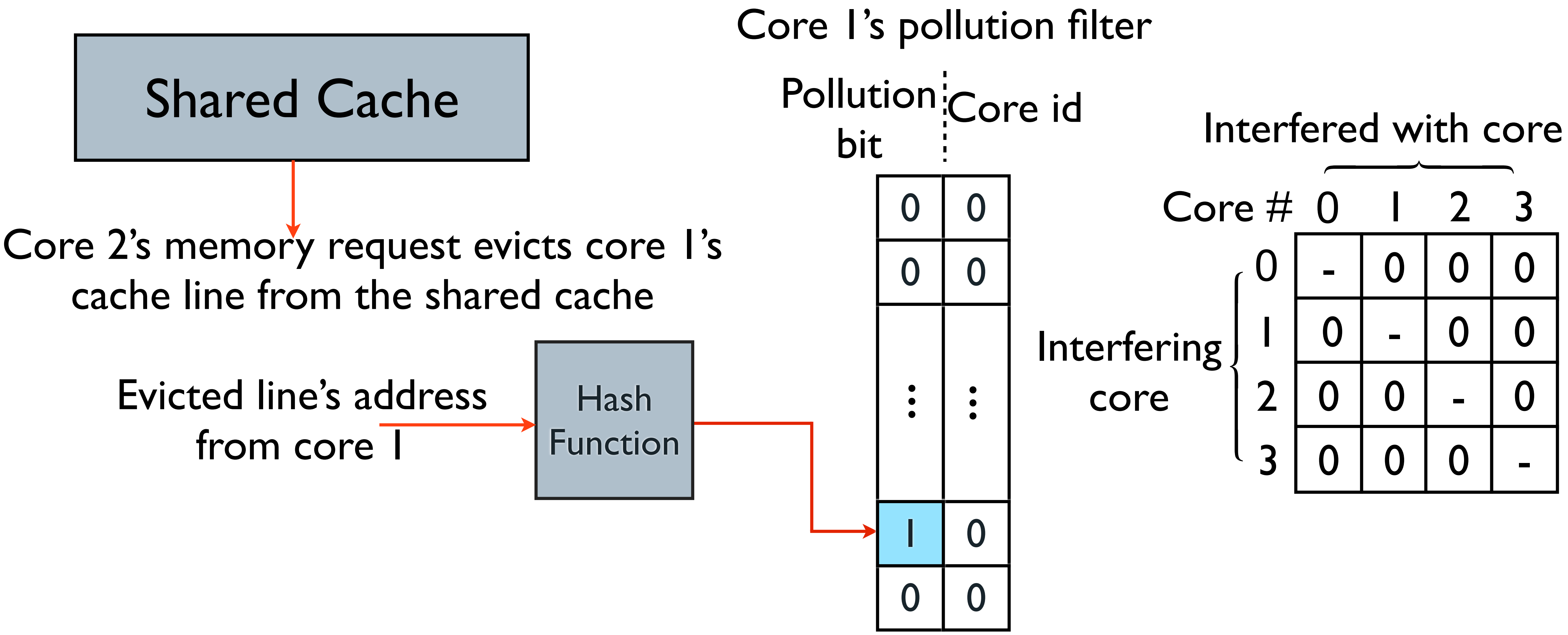
Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
0	0
0	0

Interfered with core

Interfering core	Core #	0	1	2	3
	0	-	0	0	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Tracking Cache Interference



Shared Cache

Core 2’s memory request evicts core 1’s cache line from the shared cache

Evicted line’s address from core 1

Hash Function

Core 1’s pollution filter

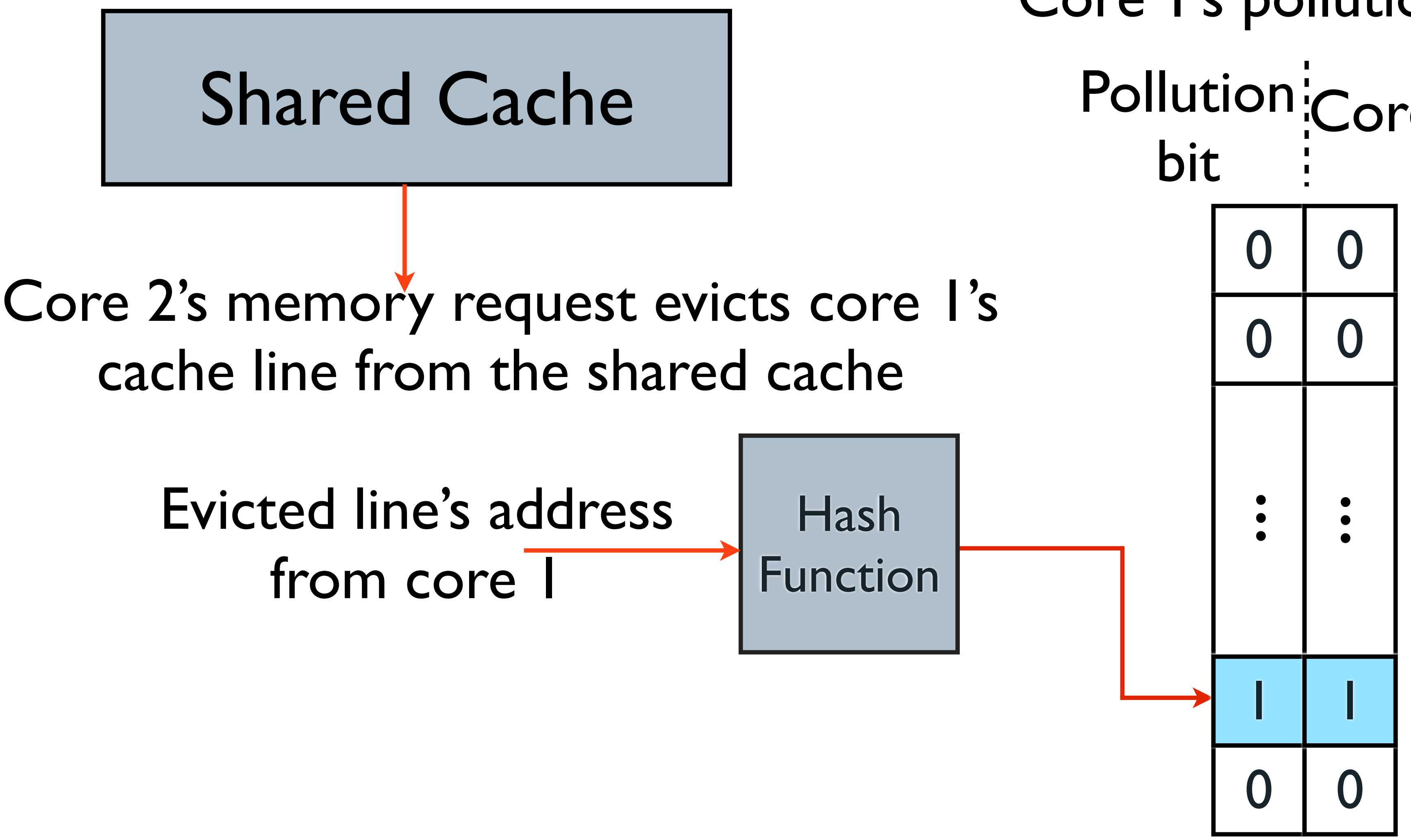
Pollution bit	Core id
0	0
0	0
⋮	⋮
1	0
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Shared Cache

Core 2’s memory request evicts core 1’s cache line from the shared cache

Evicted line’s address from core 1

Core 1’s pollution filter

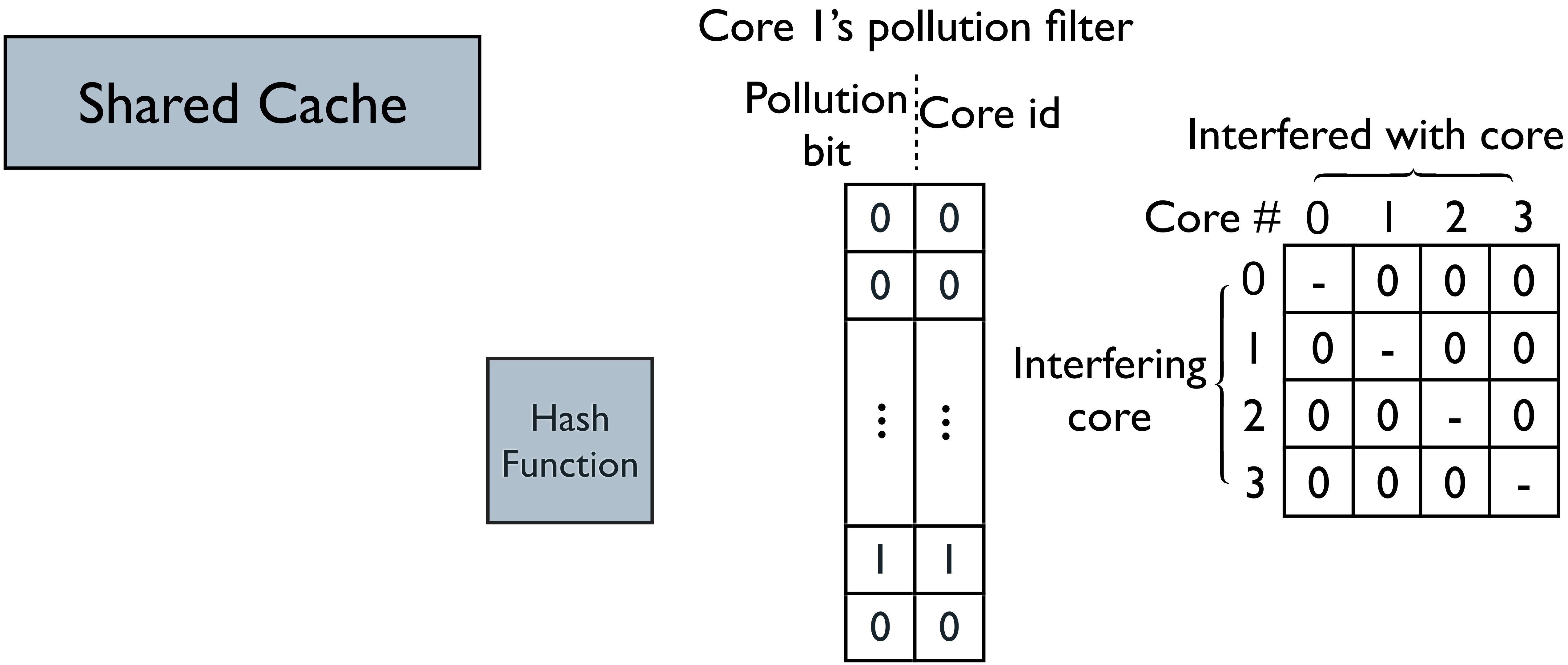
Pollution bit	Core id
0	0
0	0
⋮	⋮
1	1
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Shared Cache

Hash Function

Core 1's pollution filter

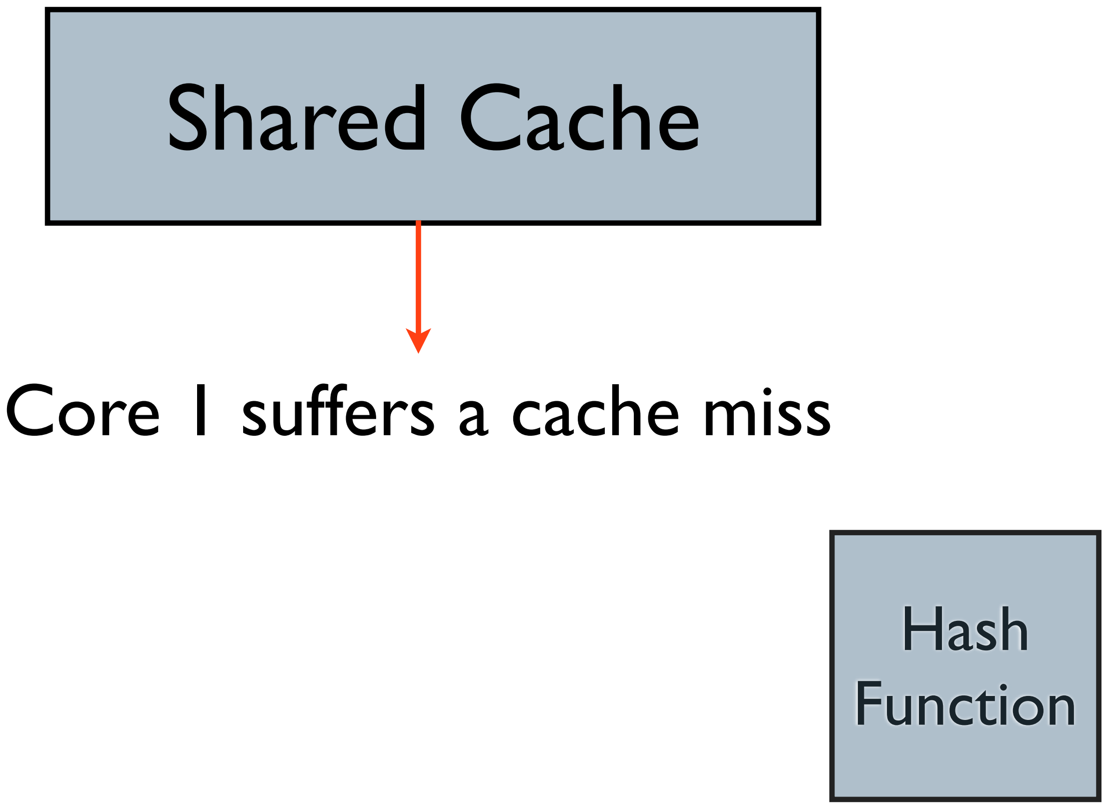
Pollution bit	Core id
0	0
0	0
⋮	⋮
1	1
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Core 1's pollution filter

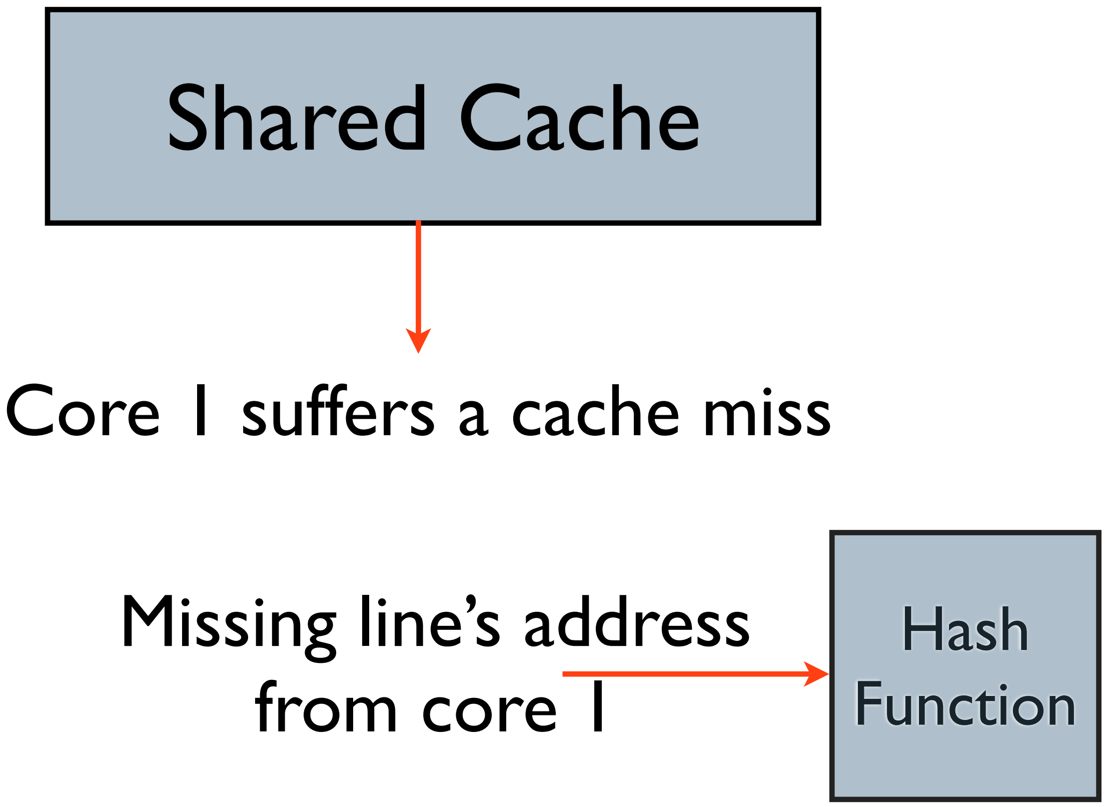
Pollution bit	Core id
0	0
0	0
⋮	⋮
1	1
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference


Shared Cache

Core 1 suffers a cache miss

Missing line's address from core 1

Hash Function

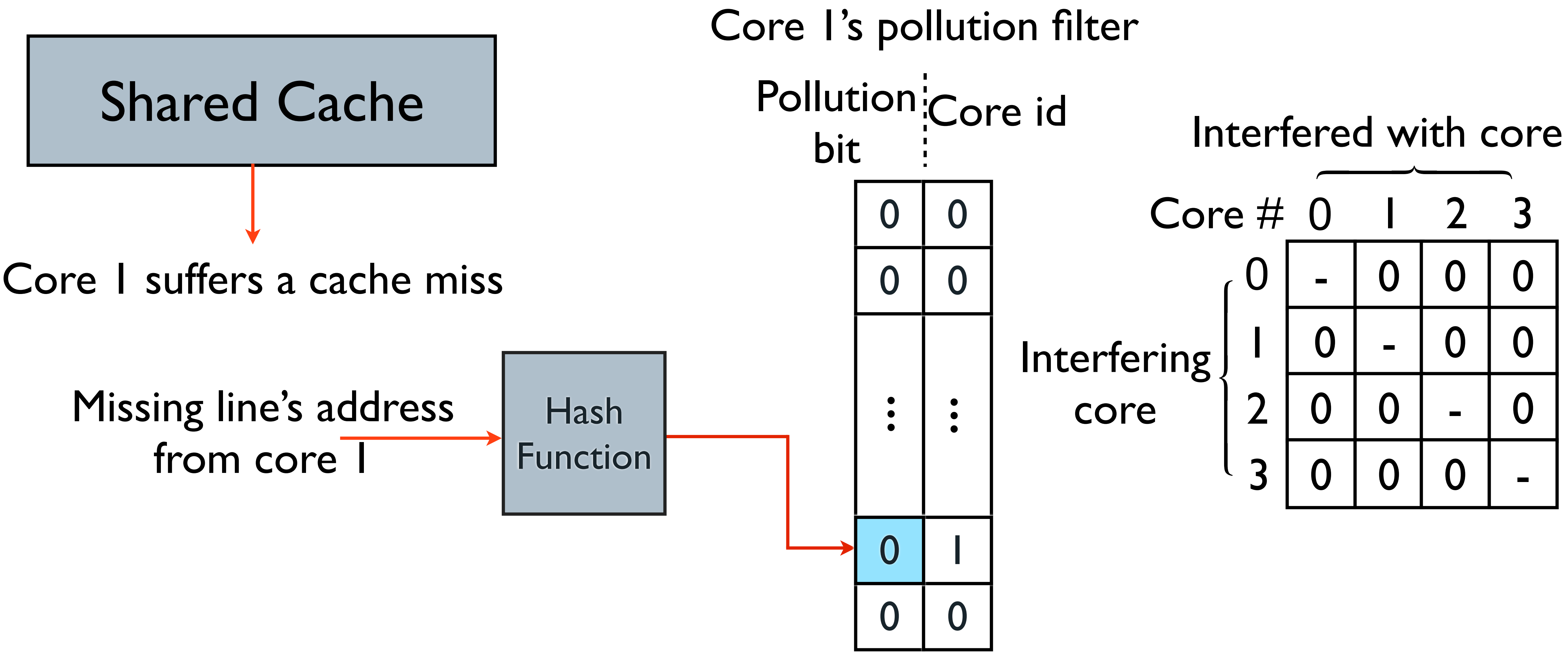
Core 1's pollution filter

Pollution bit	Core id
0	0
0	0
⋮	⋮
1	1
0	0

Interfered with core

Interfering core	Core #	0	1	2	3
	0	-	0	0	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Tracking Cache Interference


Shared Cache
Core 1 suffers a cache miss
Missing line’s address from core 1
Hash Function

Core 1’s pollution filter

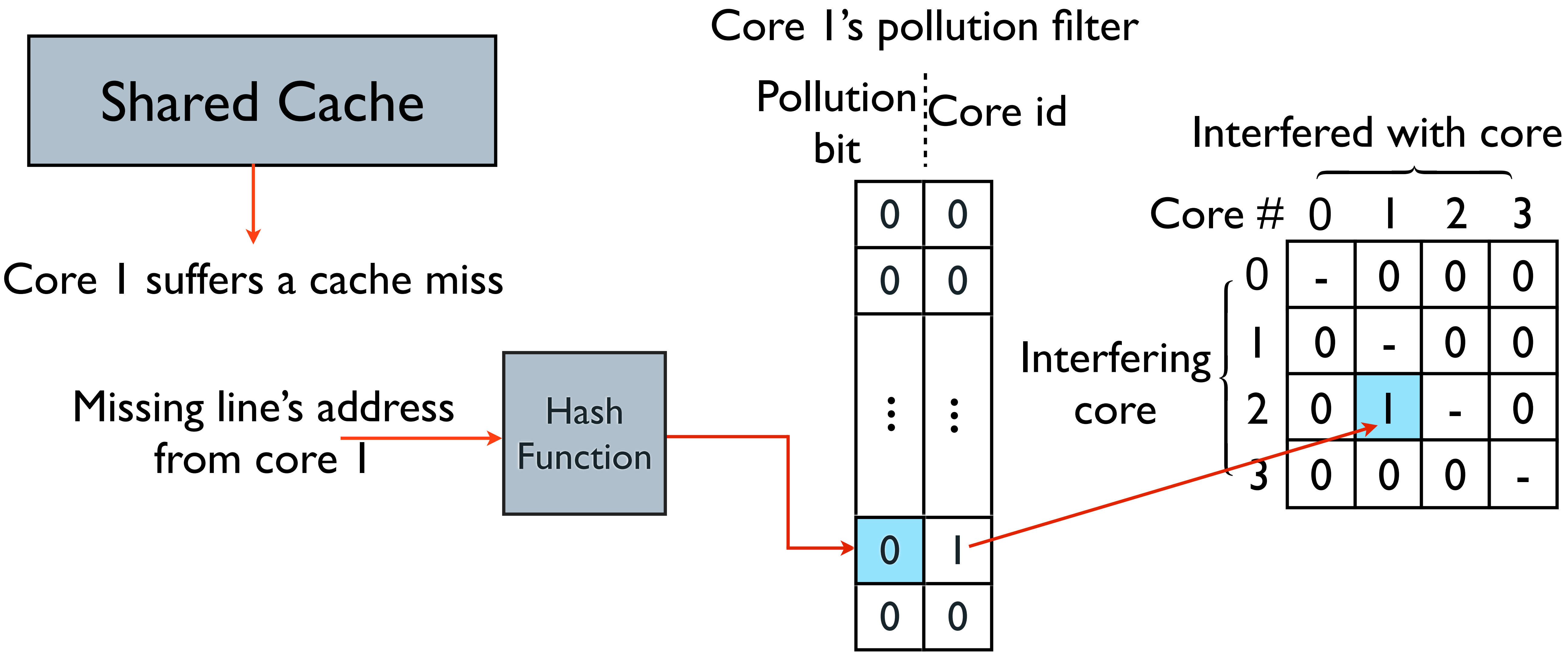
Pollution bit	Core id
0	0
0	0
⋮	⋮
0	1
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking Cache Interference



Shared Cache

Core 1 suffers a cache miss

Missing line's address from core 1

Hash Function

Core 1's pollution filter

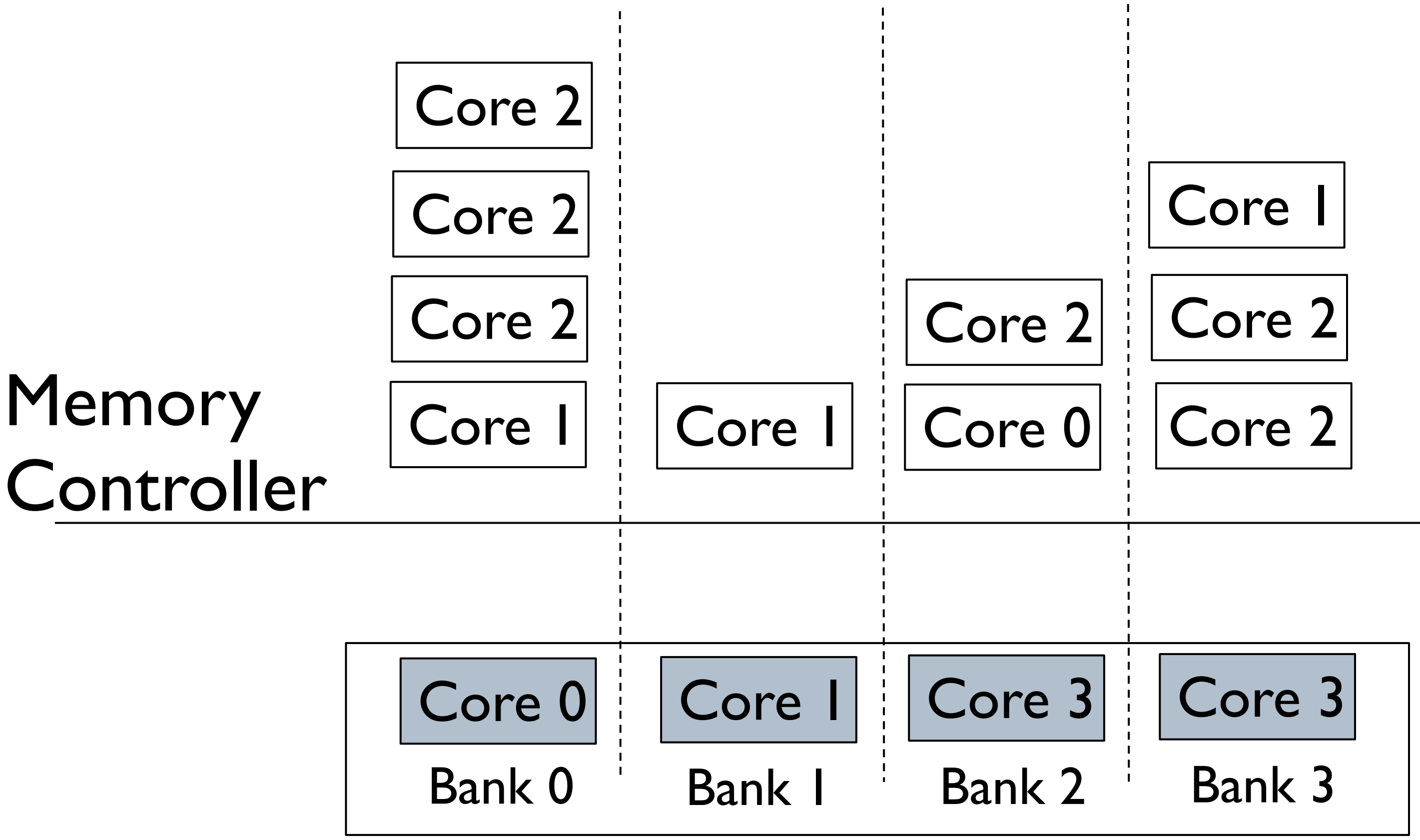
Pollution bit	Core id
0	0
0	0
⋮	⋮
0	1
0	0

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	1	-	0
3	0	0	0	-

Tracking DRAM Bank Interference



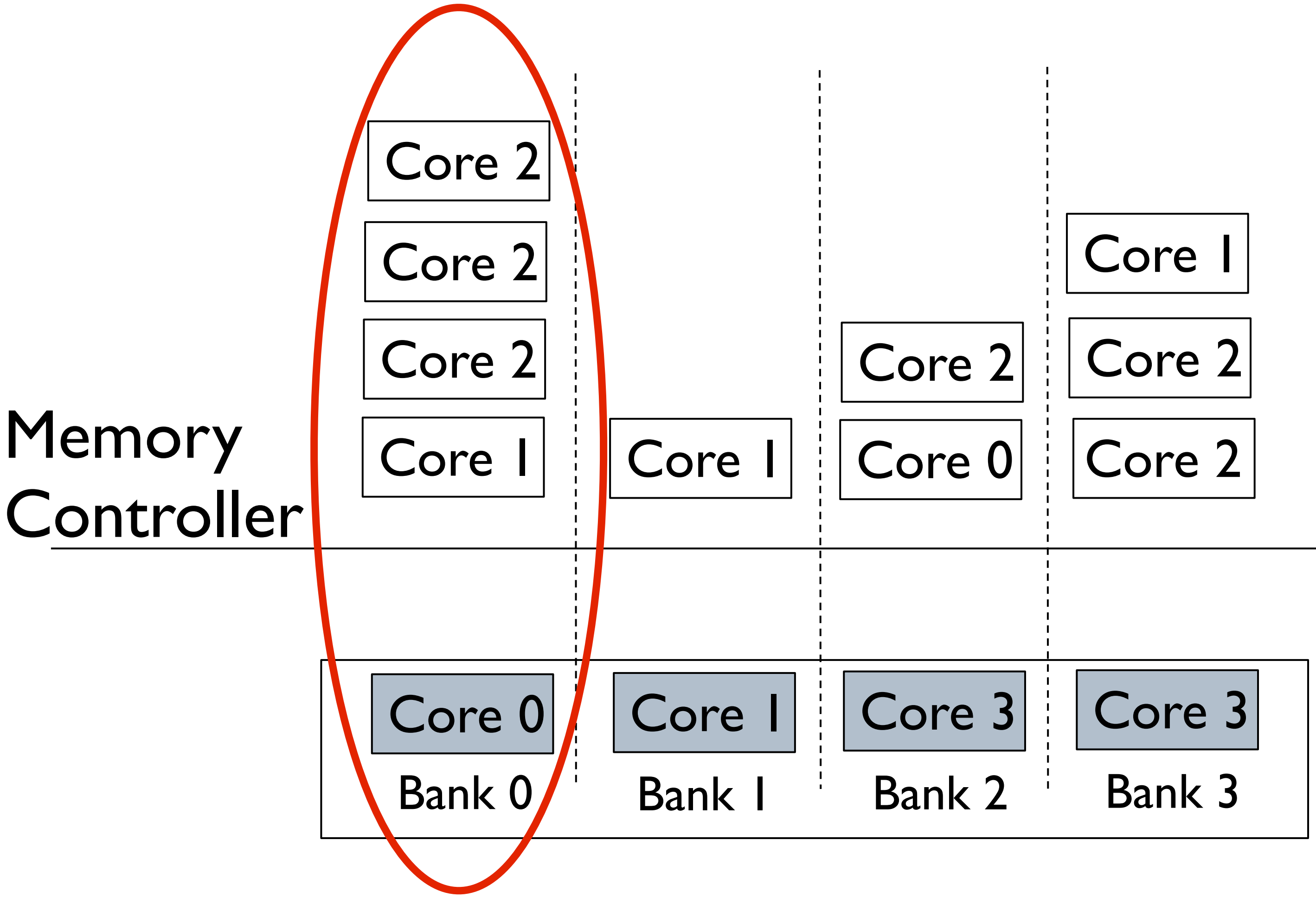
Snapshot of memory requests

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking DRAM Bank Interference



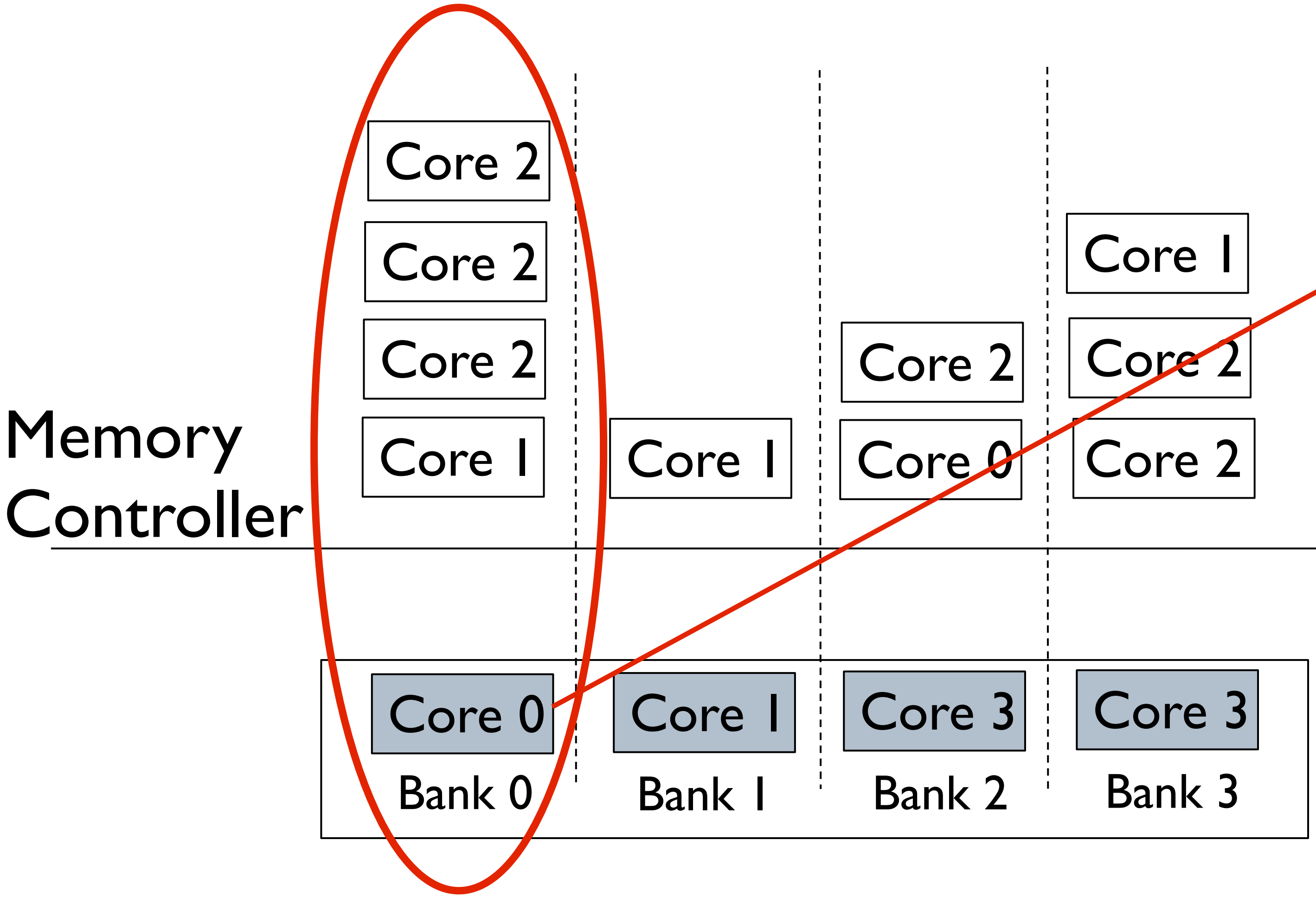
Snapshot of memory requests

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking DRAM Bank Interference



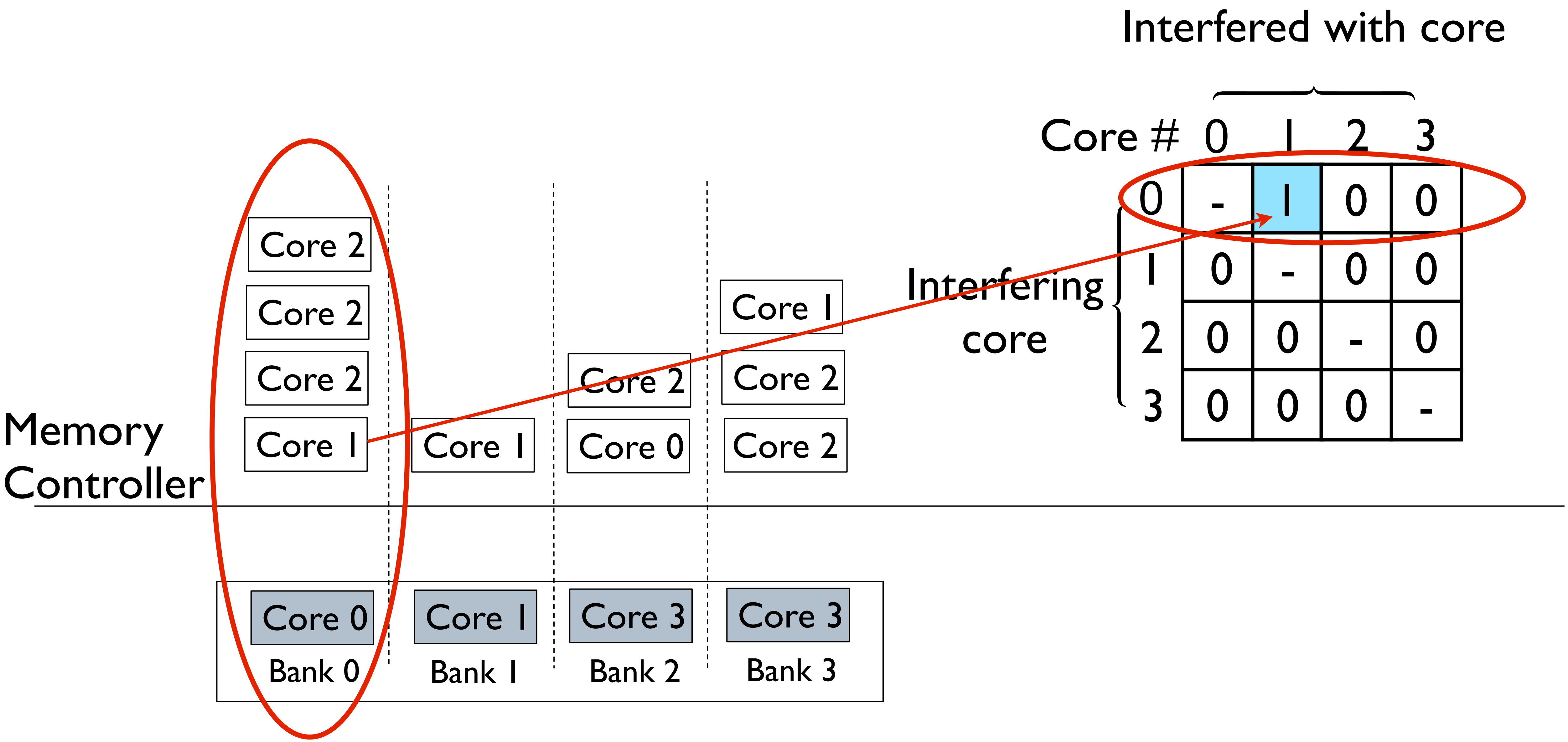
Snapshot of memory requests

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	0	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking DRAM Bank Interference



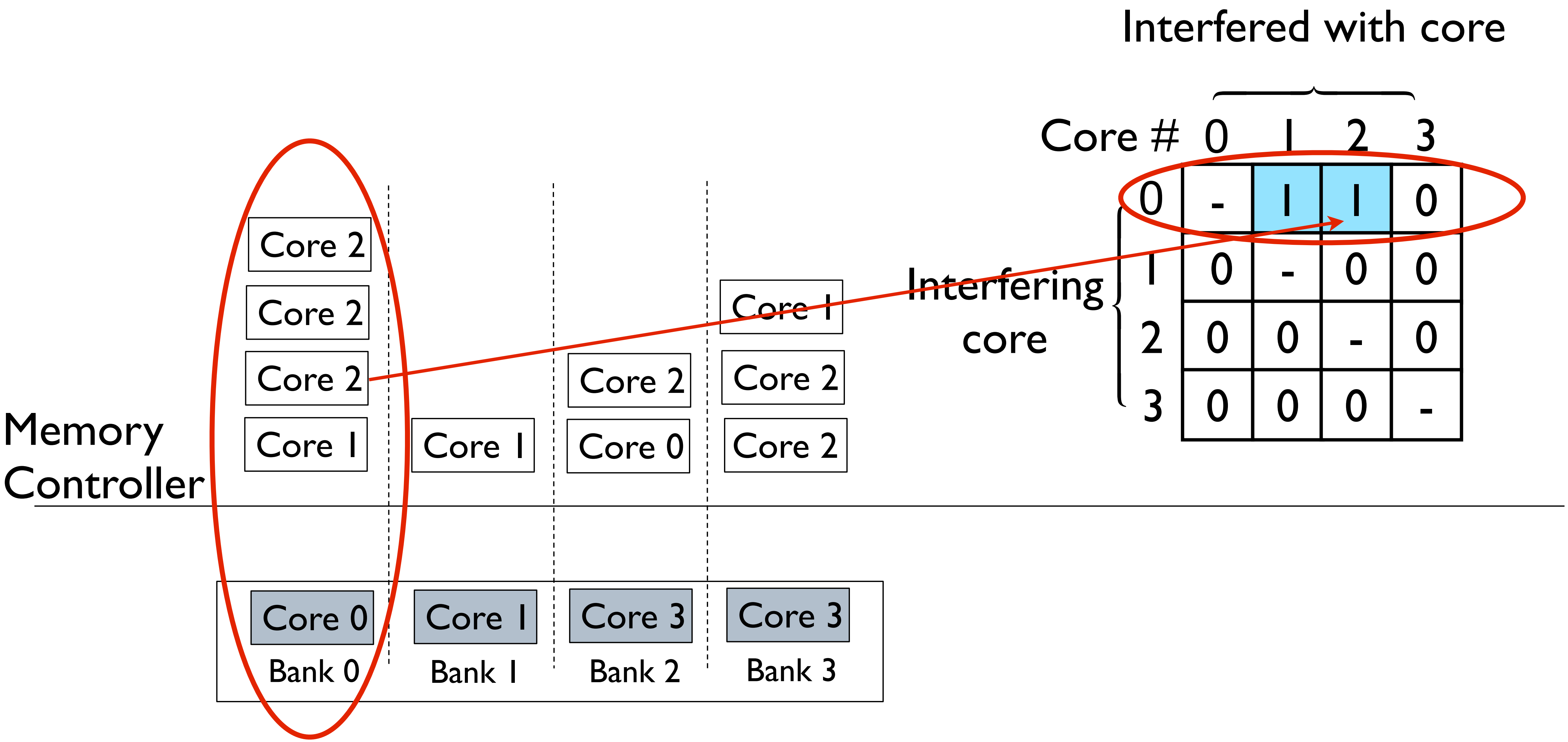
Snapshot of memory requests

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	1	0	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

Tracking DRAM Bank Interference



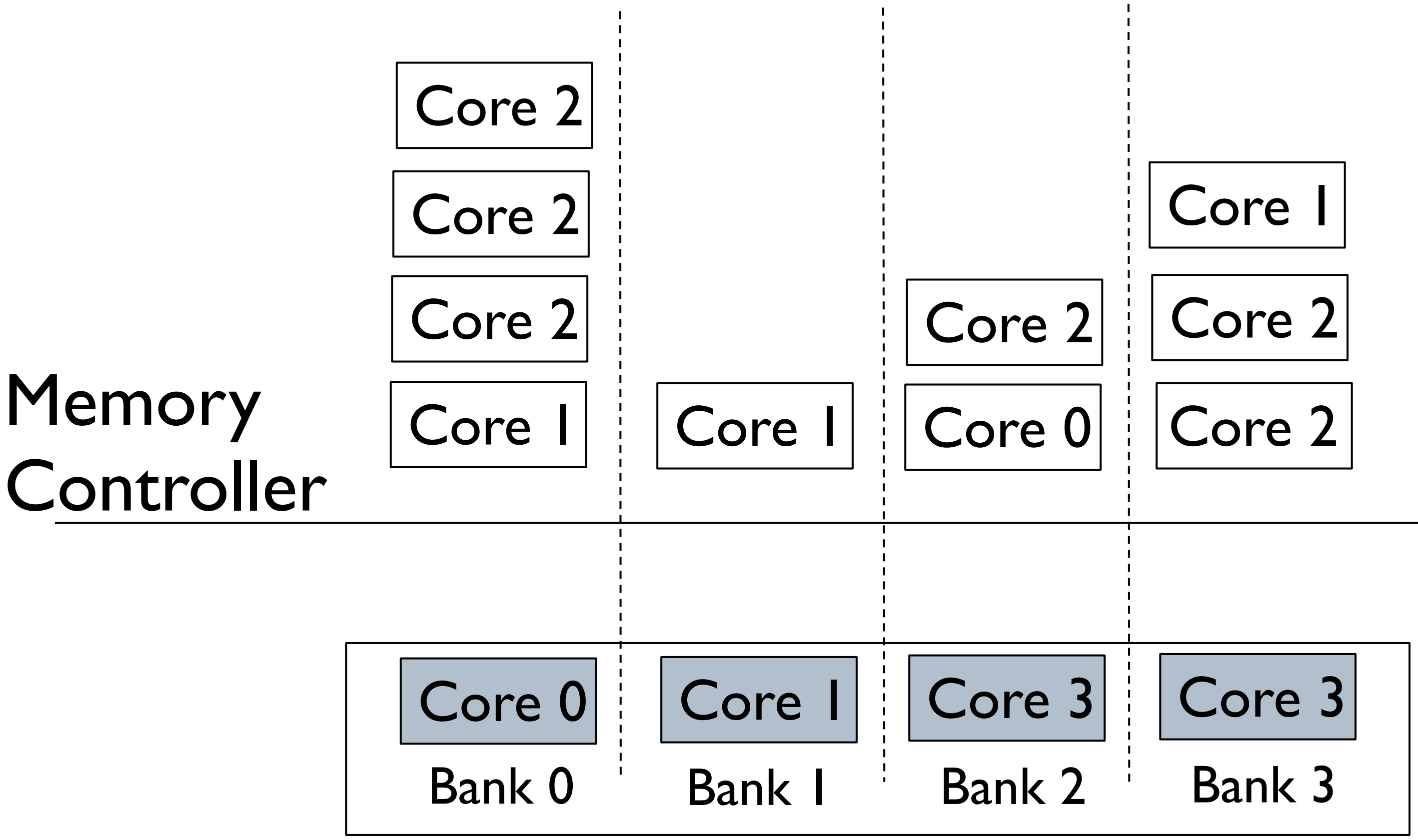
Snapshot of memory requests

Interfered with core

Interfering core

Core #	0	1	2	3
0	-	1	1	0
1	0	-	0	0
2	0	0	-	0
3	0	0	0	-

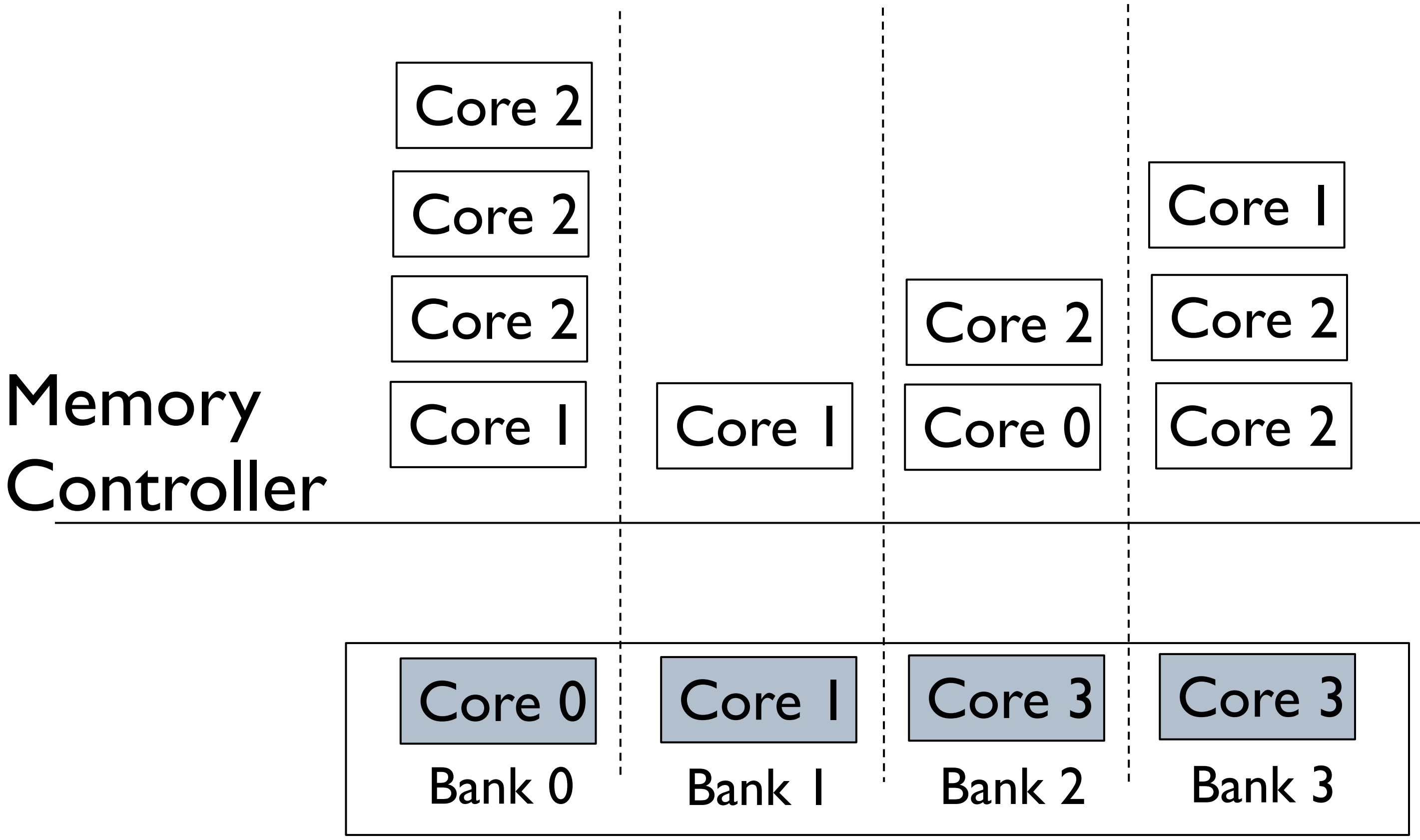
Tracking DRAM Bank Interference



Snapshot of memory requests

		Interfered with core			
	Core #	0	1	2	3
Interfering core	0	-	1	1	0
	1	0	-	0	0
	2	0	0	-	0
	3	0	0	0	-

Tracking DRAM Bank Interference



Memory Controller

Core 2
Core 2
Core 2
Core 1

Core 1

Core 2
Core 0

Core 1
Core 2
Core 2

Core 0
Bank 0

Core 1
Bank 1

Core 3
Bank 2

Core 3
Bank 3

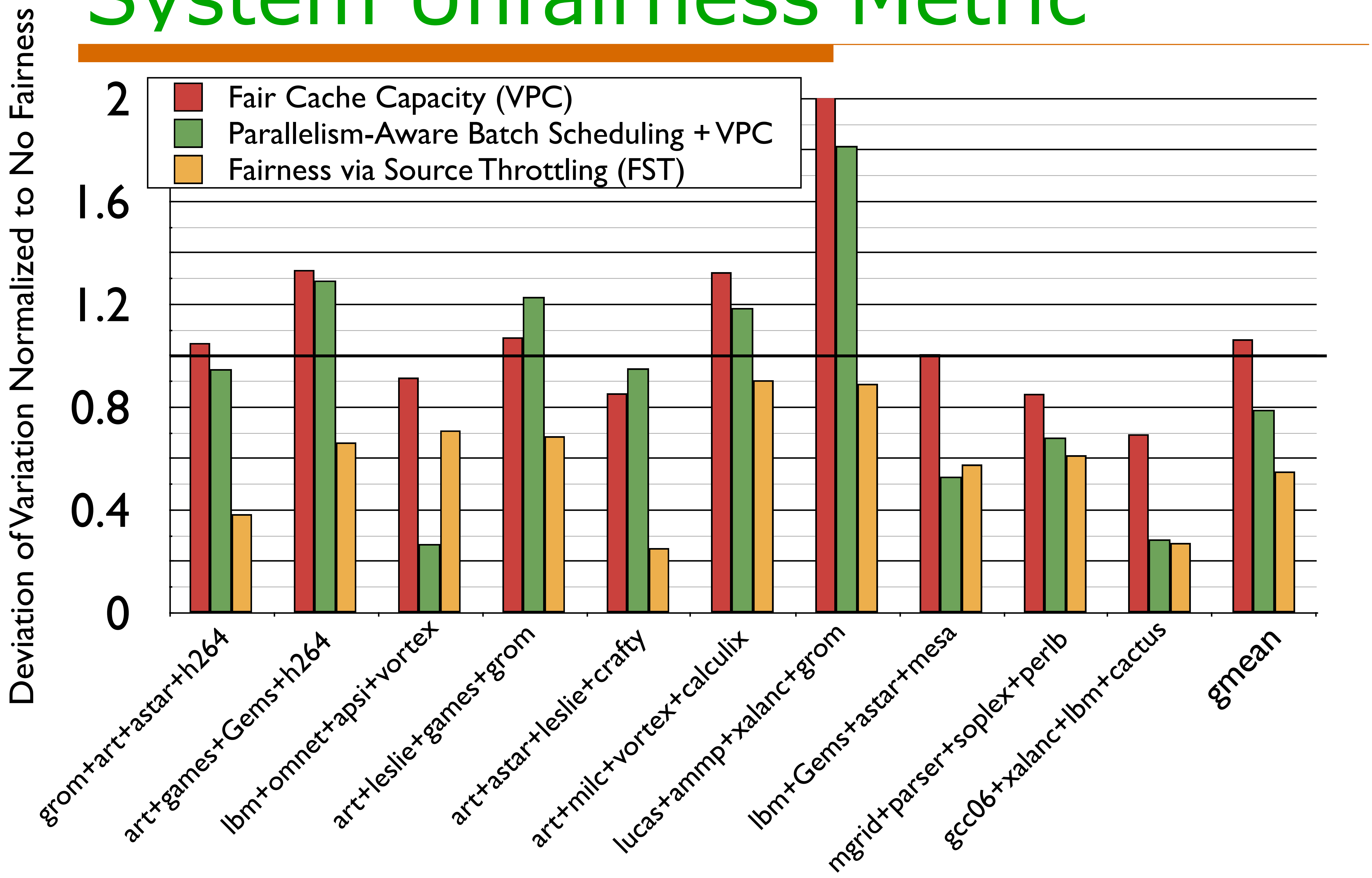
Snapshot of memory requests

Interfered with core

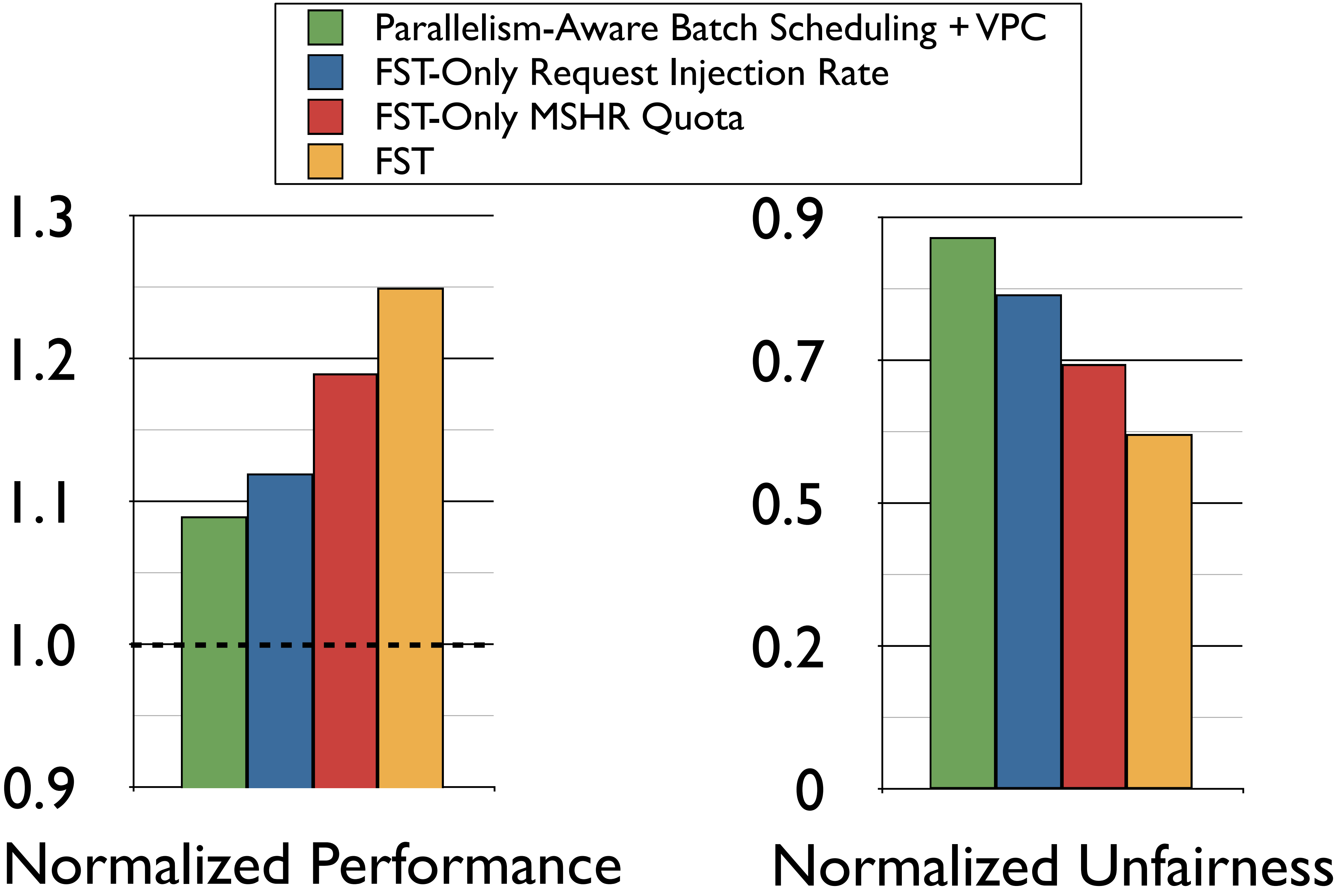
Interfering core

Core #	0	1	2	3
0	-	1	1	0
1	0	-	0	0
2	0	0	-	0
3	1	1	1	-

Results For Alternative System Unfairness Metric



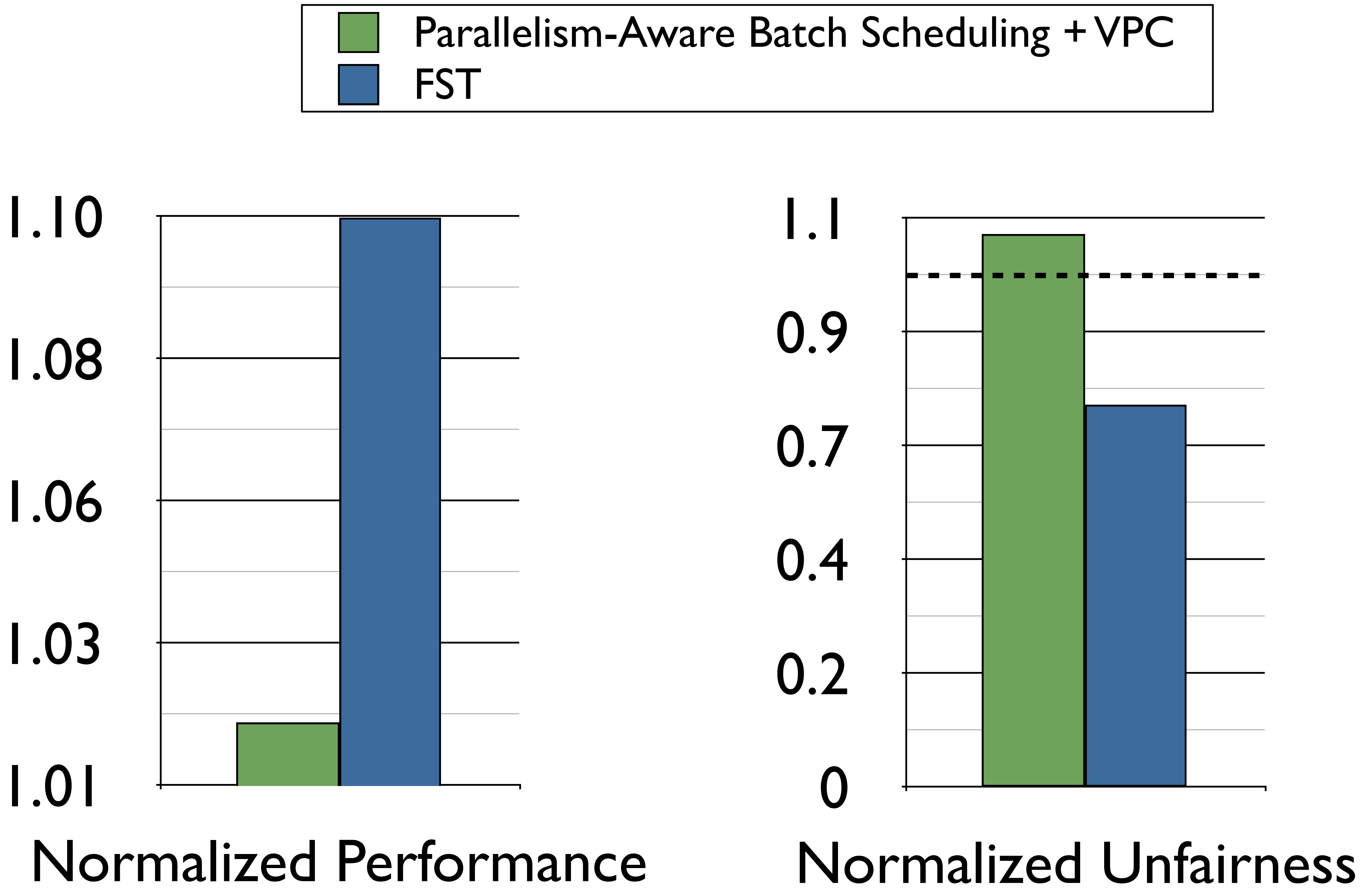
Results of Different Throttling Mechanisms



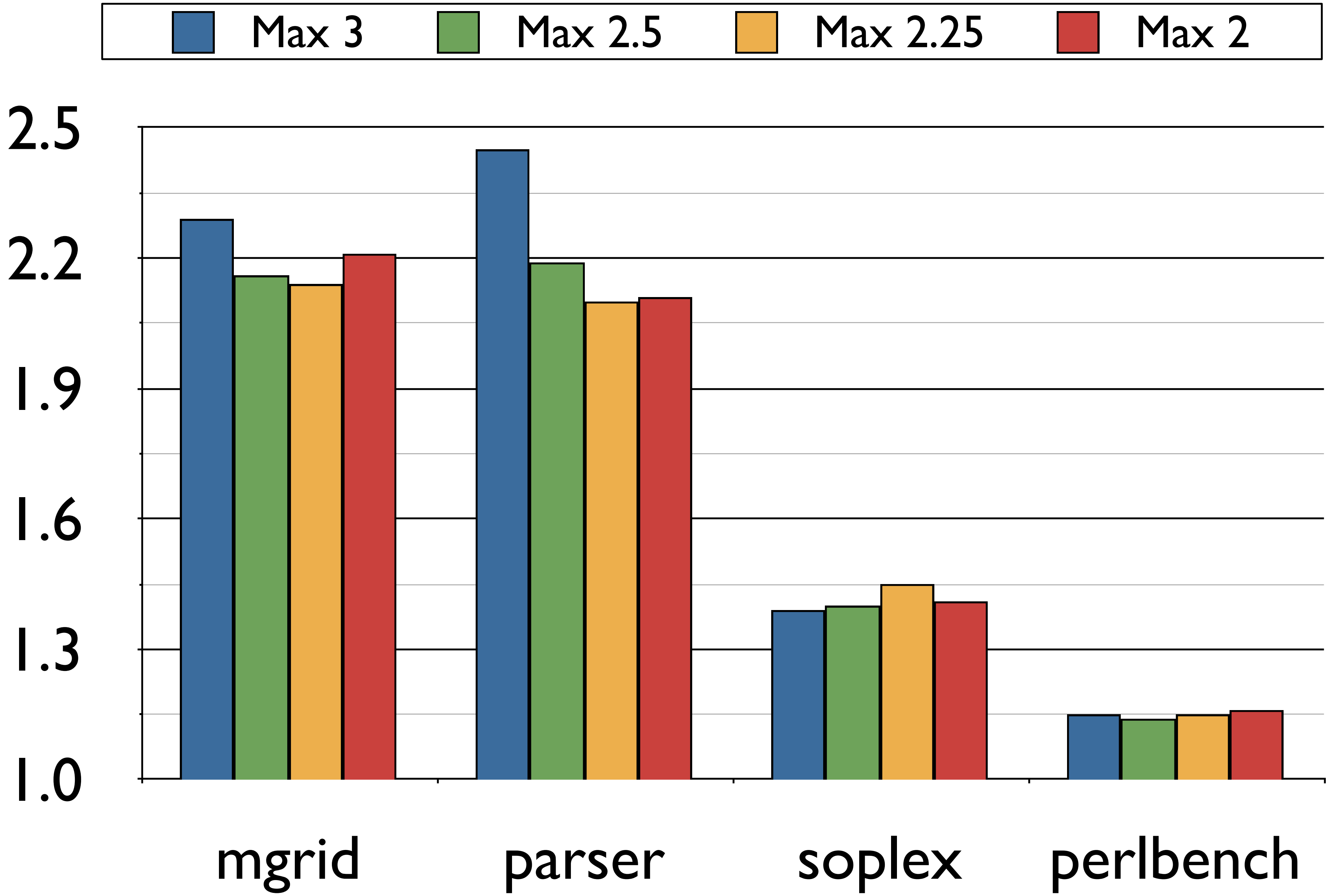
Normalized Performance

Normalized Unfairness

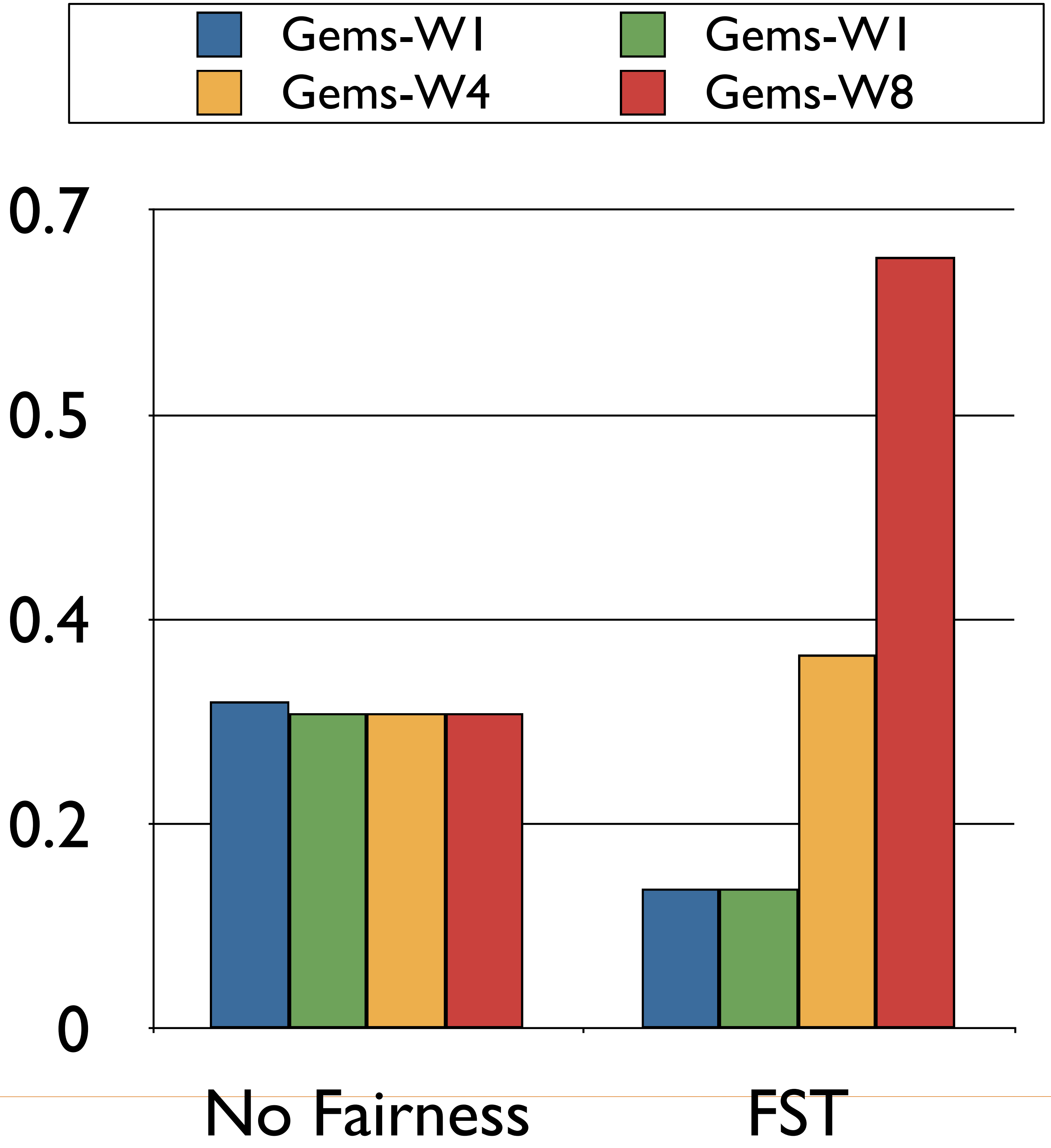
Results With 2 Memory Channels



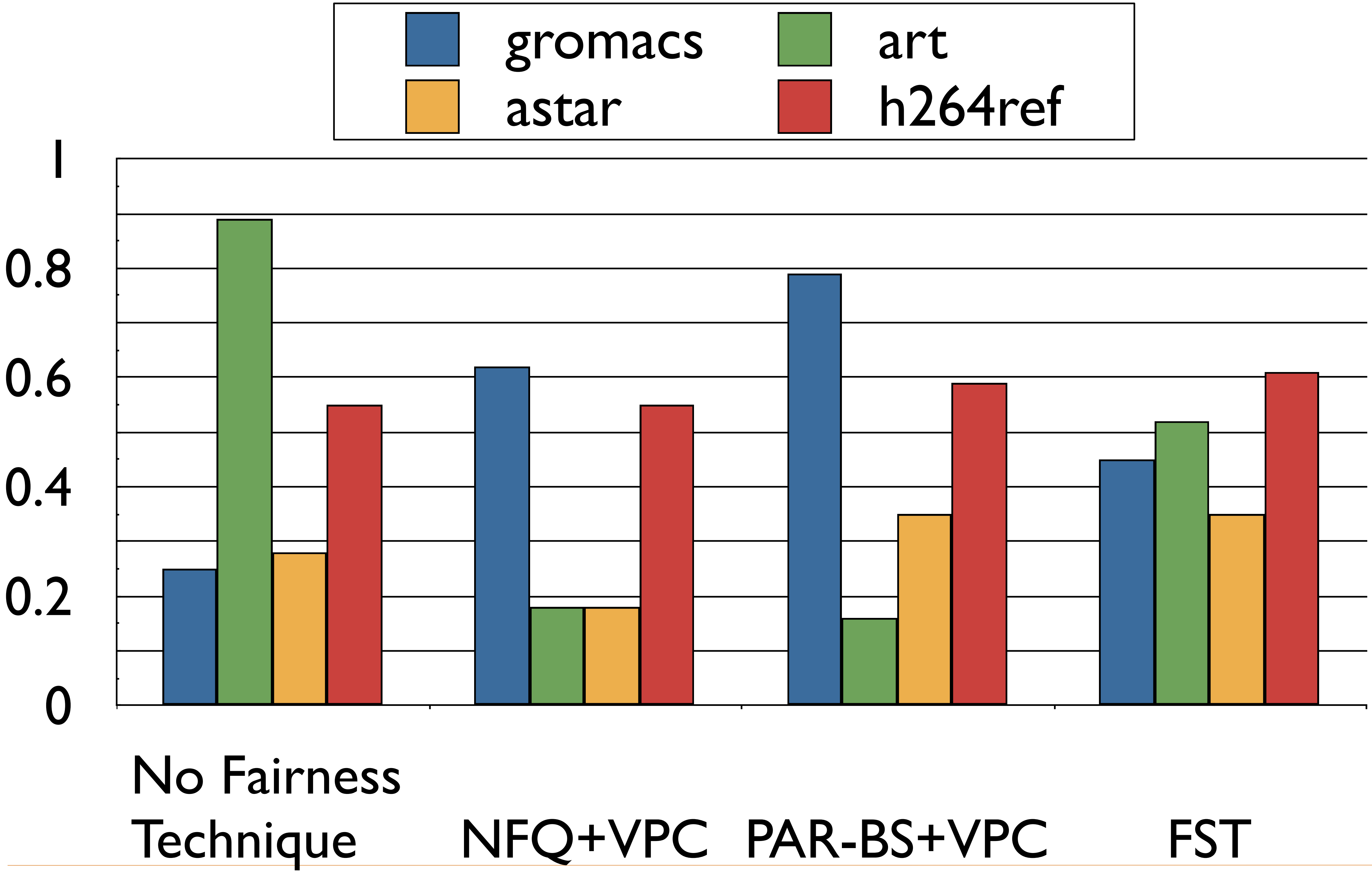
Support For Constraining Max Slowdown



Support For Thread Priorities



Case Study


gromacs
art
astar
h264ref
1
0.8
0.6
0.4
0.2
0
No Fairness Technique
NFQ+VPC
PAR-BS+VPC
FST