Onur Mutlu

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One-Page Biography

Onur Mutlu was born in 1978 in Turkey. He earned his dual Bachelor of Science degrees in Computer Engineering and Psychology from the University of Michigan, and his Master's and PhD in Computer Engineering from the University of Texas at Austin. During his PhD, he invented the Efficient Runahead Execution technique for tolerating long memory latencies in modern processors, variants of which are implemented in commercial microprocessors (e.g., IBM POWER6, Sun/Oracle Rock). His dissertation's influence on academic and industrial research on the topic still continues. Between 2001-2005, he worked in the cutting-edge microprocessor design and research groups at Intel Corporation and Advanced Micro Devices, where he adapted his Efficient Runahead Execution [Mutlu+, HPCA'03, ISCA'05] and Feedback-Directed Data Prefetching [Srinath+, HPCA'07] mechanisms for future systems.

In 2006, he joined Microsoft Research Redmond to start the Computer Architecture Group. During his 2.5-year tenure there, he conducted seminal research into memory systems for multi-core processors. His research into memory controllers spearheaded a fresh research area in computer architecture, which continues to thrive. With his collaborator Thomas Moscibroda, he discovered that existing multi-core memory controllers were vulnerable to denial service attacks [Moscibroda+, USENIX Security'07]. In a series of works published at top venues in computer architecture since 2007, he devised new memory control algorithms that provide high system performance, fairness, and quality of service. These techniques turned memory controllers into a center of attention in computer architecture. In particular, his MICRO'07 paper on "Stall-Time Fair Memory Access Scheduling" and ISCA'08 paper on "Parallelism-Aware Batch Scheduling" have greatly ignited academic research on memory controllers by exposing new problems and new solutions. Variants of his Parallelism-Aware Batch Scheduler [Mutlu+, ISCA'08] are implemented in some memory controllers designed by Samsung.

In 2009, he moved to Carnegie Mellon University as an Assistant Professor. He continued attacking the "memory problem" from all angles, with impact on both major academic research directions and commercial products. He advocated and analyzed the use of Phase Change Memory technology as part of the main memory of a computing system [Lee+, ISCA'09], starting a new area in computer architecture: how to enable/exploit emerging non-volatile memory technologies. This work is considered a precursor of 3D XPoint by Intel and other technologies that are being designed for main memory.

His work on flash memory reliability, starting with his paper entitled "Error Patterns in MLC NAND Flash Memory: Measurement, Characterization, and Analysis" [Cai+, DATE'12], uncovered new error mechanisms, provided precious experimental data, and greatly improved flash memory lifetime. These works are regarded as prime resources for educating engineers in leading flash memory companies, Samsung, SK Hynix, Seagate, Sandisk, Micron.

His work on key DRAM challenges (refresh, latency, energy, variability, reliability, scaling) ignited substantial academic research and influenced industry directions. For example, his Subarray-Level Parallelism work [Kim+, ISCA'12] is advocated by Intel and Samsung to be in future DRAM standards [Kang+, Memory Forum'14]. He pioneered recent research on solving the DRAM refresh problem [Liu+, ISCA'12], igniting academic and industrial research on the topic. His research showed that refresh is the key scaling limiter of the DRAM technology, experimentally discovered novel problems related to it and provided precious experimental data (in another seminal work [Liu+, ISCA'13]), and developed practical solutions to the refresh problem (e.g., [Qureshi+, DSN'15]). His work experimentally demonstrated, analyzed, and provided architectural solutions for critical DRAM issues (e.g., refresh [Liu+, ISCA'13][Khan+, SIGMETRICS'14][Qureshi+, DSN'15], latency [Lee+, HPCA'13, HPCA'15], variability [Chang+, SIGMETRICS'16], energy [David+, ICAC'11], reliability [Meza+, SIGMETRICS'15]) by analyzing modern DRAM chips using real FPGA-based experimental platforms [Hasan+, HPCA'17], providing precious data available nowhere else.

In 2014, his group discovered the RowHammer problem [Kim+, ISCA'14], a failure mechanism affecting most real DRAM chips. This work shook the fundamentals of systems security: Google and others demonstrated attacks that exploit RowHammer to take over an otherwise-secure system. RowHammer is the first example of a hardware failure mechanism that causes a practical and widespread system security vulnerability. It continues to have widespread impact on systems, security, software, and hardware communities, both academic and industrial: e.g., it caused a new Hammer Test to be included in standard memory test programs, and Apple cited the work [Kim+, ISCA'14] in its critical security release that introduced a hardware patch to mitigate RowHammer.

For his contributions, he received the endowed Strecker Early Career Professorship at Carnegie Mellon (2013), the first IEEE Computer Society Young Computer Architect Award (2011), the first Intel Early Career Faculty Award (2012), and the Ladd Research Award from CMU (2012). 11 of his papers were chosen as Top Picks by IEEE Micro, and more than 14 received Best Paper recognitions. He received numerous Faculty Awards from Facebook, Google, HP, IBM, Intel, Microsoft, NSF.

He spent significant time in industry, enabling technology transfer of his ideas. He was with Intel (Summer'01-'03 and '12) and AMD (Summer'04-'05), researching novel microprocessor designs, and with VMware (Spring-Summer'16) and Google (Summer'16), exploring new memory and system architectures. He continues to collaborate with industry on both fundamental and cutting-edge technology issues.

He has advocated open sharing of teaching and research artifacts to democratize education/research worldwide. His computer architecture course videos/materials and his group's research artifacts are freely available online. They are used by many educators, researchers and practitioners, including companies like Google.

In September 2015, he was appointed Full Professor of Computer Science at ETH Zürich, where he started in May 2016. He continues to thrive on research, education, and service for the community. More information is available on his webpage: https://people.inf.ethz.ch/omutlu/.

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Research, Teaching and Consulting Interests

- Computer architecture and systems. Memory systems. Multi/many-core systems. Scalable, QoS-aware, latency-tolerant systems.
- Computer architectures for secure and robust operating systems (OS). OS/architecture interaction.
- Architectural support for safe/managed/parallel programming languages (PL) and programmer productivity. PL/architecture interaction.
- Fault tolerant and bug-tolerant architectures. Dependable systems.
- System-wide resource management and QoS, especially in multi-core and multithreaded systems.
- Novel computer architectures for health, biological, medical, and bioinformatics applications. Bio-inspired systems.
- Bioinformatics algorithms and architectures. Genome sequence analysis and assembly techniques.

Education

University of Texas at Austin
September 2000 - August 2006

Ph.D., Computer Engineering, August 2006
Dissertation Title: *Efficient Runahead Execution Processors*
Nominated for the ACM Doctoral Dissertation Award by UT-Austin
M.S.E., Computer Engineering, May 2002

University of Michigan, Ann Arbor
September 1997 - August 2000

B.S.E., *summa cum laude*, Computer Engineering, August 2000
B.S., *with highest distinction*, Psychology, August 2000

Professional Experience

ETH Zürich, Dept. of Computer Science (D-INFK), Full Professor, ***September 2015 - Present***
Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Adjunct Professor, ***June 2016 - Present***
Bilkent University, Dept. of Computer Engineering, Adjunct Professor, ***November 2015 – Present***
Google, Visiting Research Scientist, ***May 2016 – September 2016***
VMware, Scholar in Residence, ***February 2016 – September 2016***
Carnegie Mellon University, Dept. of ECE, Dr. William D. and Nancy W. Strecker Endowed Early Career Professor, ***January 2013 - June 2016***
Intel Corporation, Visiting Researcher, ***June 2012 – August 2012***
Carnegie Mellon University, Dept. of Electrical and Computer Engineering, Assistant Professor, ***January 2009 - January 2013***
Carnegie Mellon University, Dept. of Computer Science, Courtesy Professor, ***January 2009 - Present***
Microsoft Research, Computer Architecture Group (Redmond, WA), Researcher, ***August 2006 - January 2009***
University of Texas at Austin, Dept. of Electrical and Computer Engineering, Research Fellow, ***August 2007 - January 2009***
University of Texas at Austin, Dept. of Electrical and Computer Engineering, Research and Teaching Assistant, ***August 2000 - August 2006***
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, ***May – August 2005***
Advanced Micro Devices, Architecture/Performance Modeling Group (Sunnyvale, CA), Co-op Engineer, ***May – August 2004***
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, ***May – August 2003***
Intel Corporation, Microprocessor Research Labs (Hillsboro, OR), Graduate Technical Intern, ***May – August 2002***
Intel Corporation, Desktop Platforms Group (Hillsboro, OR), Graduate Technical Intern, ***May – August 2001***

Honors and Awards

- Google Faculty Research Award, 2015, 2016
- Microsoft Research Software Engineering Innovation Foundation Award, 2014
- Dr. William D. and Nancy W. Strecker Early Career Professorship, January 2013
- IBM Faculty Partnership Award, 2012, 2013
- Intel Early Career Faculty Honor Program Award, 2012
- Carnegie Mellon University College of Engineering George Tallman Ladd Research Award, 2012
- IEEE Computer Society Technical Committee on Computer Architecture Young Computer Architect Award, 2011
- Hewlett-Packard Laboratories Innovation Research Program Award, 2012
- Nvidia CUDA Center of Excellence Award, 2012, 2013 (with multiple CMU Faculty members)
- Keynote, plenary and invited talks at many conferences and workshops, including ISMM 2016, DAC 2016, RSP 2016, ARM Research Summit 2016, FABULOUS 2016, MST 2016, NoCArc 2015, CASS 2015, SBAC-PAD 2015, SAMOS 2015, ISC 2015, ASAP 2014, DaMoN 2014, Summer Supercomputing Academy of Moscow State University 2014, IMW 2013, ISMM 2011.
- Best paper award at RTAS 2014
  Bounding Memory Interference Delay in COTS-based Multi-Core Systems
- Best paper award at ICCD 2012 (Computer Systems and Applications Track)
  Row Buffer Locality Aware Caching Policies for Hybrid Memories

- Best paper award at ASPLOS 2010
  Fairness via Source Throttling: A Configurable and High-Performance Fairness Substrate for Multi-Core Memory Systems
- Best paper award at VTS 2010 (awarded in 2011)
  Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips
- One paper selected as Honorable Mention for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2015
  A Scalable Processing-in-Memory Accelerator for Parallel Graph Processing
- One paper (of 12 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2011
  Kilo-NOC: A Heterogeneous Network-on-Chip Architecture for Scalability and Service Guarantees
- Three papers (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2010
  Thread Cluster Memory Scheduling: Exploiting Differences in Memory Access Behavior
  Aergia: Exploiting Packet Latency Slack in On-Chip Networks
  Data Marshaling for Multi-core Architectures
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2009
  Accelerating Critical Section Execution with Asymmetric Multi-Core Architectures
  Architecting Phase Change Memory as a Scalable DRAM Alternative
- One paper (of 12 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2008
  Parallelism-Aware Batch Scheduling: Enabling High-Performance and Fair Memory Controllers
- One paper (of 11 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2006
  Diverge-Merge Processor (DMP): Generalized and Energy-Efficient Dynamic Predication
- Two papers (of 13 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2005
  Efficient Runahead Execution: Power-efficient Memory Latency Tolerance
  Wish Branches: Enabling Adaptive and Aggressive Predicated Execution
- One paper (of 15 total) selected for IEEE Micro's "Top Picks from Computer Architecture Conferences," 2003
  Runahead Execution: An Effective Alternative to Large Instruction Windows
- One paper selected for CACM's "Research Highlights," 2009
  Architecting Phase Change Memory as a Scalable DRAM Alternative
- Best Paper Session at MICRO 2016: *Continuous Runahead: Transparent Hardware Acceleration for Memory Intensive Workloads*
- Best Paper Session (Runner-Up) at HPCA 2015: *Data Retention in MLC NAND Flash Memory: Characterization, Optimization and Recovery*
- Best Paper Session at HPCA 2014: *Improving Cache Performance by Exploiting Read-Write Disparity*
- Best Paper Session at HPCA 2010: *ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers*
- Best Paper Session at HPCA 2009: *Techniques for Bandwidth-Efficient Prefetching of Linked Data Structures in Hybrid Prefetching Systems*
- Best paper award nominations at MICRO 2016, NOCS 2015, NOCS 2012, HPCA 2015, HPCA 2014, HPCA 2010, HPCA 2009, HPCA 2007, MICRO 2006, and MICRO 2005 conferences
- Selected to the ISCA and MICRO Halls of Fame, 2009
- Selected to the HPCA Hall of Fame, 2010
- NSF CAREER Award, 2010 (*QoS-Aware, High-Performance, and Scalable Many-Core Memory Systems*)
- Microsoft Gold Star Award, 2008
- Distinguished Lecture at Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, 28 June 2012.
- PhD Dissertation nominated by UT-Austin for the ACM Doctoral Dissertation Award, 2006
- University Co-op/George H. Mitchell Award for Excellence in Graduate Research (Awarded to 6 out of 271 nominees at UT-Austin), 2005
- Intel Foundation Ph.D. Fellowship, 2004
- University of Texas Graduate School Continuing Fellowship, 2003
- University of Michigan EECS Dept. Summer Research Fellowship, 1999, 2000
- University of Michigan EECS Dept. William Harvey Seeley Award (money award given to the top undergraduate junior), 1999
- University of Michigan Branstrom Freshman Prize, 1998

Publications

(Please visit `https://people.inf.ethz.ch/omutlu/projects.htm` for electronic copies.)
(Please visit `http://scholar.google.com/citations?user=7XyGUGkAAAAJ&hl=en` for citations.)
(H-index: 61, I10-index: 157, Citation count: 13136 – according to Google Scholar, as of March 11, 2017)

Book Chapters

1. Vivek Seshadri, Onur Mutlu, "Simple Operations in Memory to Reduce Data Movement," to appear in *Advances in Computers*, Elsevier, 2017.
2. Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Abhishek Bhowmick, Rachata Ausavarungnirun, Chita Das, Mahmut Kandemir, Todd C. Mowry, Onur Mutlu,"A Framework for Accelerating Bottlenecks in GPU Execution with Assist Warps," in *Advances in GPU Computing and Practice*, Elsevier, 2016.
3. Onur Mutlu, "Main Memory Scaling: Challenges and Solution Directions," in *More Than Moore Technologies for Next Generation Computer Design*, *Springer*, January 2015.
4. Yoongu Kim, Onur Mutlu, "Memory Systems," in *Computing Handbook: Computer Science and Software Engineering*, *CRC Press*, April 2014.

5. Chris Fallin, Greg Nazario, Xiangyao Yu, Kevin Chang, Rachata Ausavarungnirun, Onur Mutlu, "Bufferless and Minimally-Buffered Deflection Routing," in *Routing Algorithms in Networks-on-Chip*, *Springer*, 2014.
6. M. Aater Suleman, Onur Mutlu, "Accelerating Critical Section Execution with Multi-Core Architectures," in *Multicore Technology: Architecture, Reconfiguration, and Modeling*, *CRC Press*, July 2013.

Refereed Conference (and Major Workshop) Publications

7. Minesh Patel, Jeremie Kim, Onur Mutlu, "The Reach Profiler (REAPER): Enabling the Mitigation of DRAM Retention Failures via Profiling at Aggressive Conditions," *Proceedings of the 44th International Symposium on Computer Architecture (**ISCA**)*, Toronto, Canada, June 2017.
8. Kaan Kara, Dan Alistarh, Ce Zhang, Onur Mutlu, Gustavo Alonso, "FPGA-accelerated Dense Linear Machine Learning: A Precision-Convergence Trade-off," *Proceedings of the 25th International Symposium on Field-Programmable Custom Computing Machines (**FCCM**)*, Napa, CA, USA, April 2017.
9. Kevin Hsieh, Aaron Harlap, Nandita Vijaykumar, Dimitris Konomis, Gregory R. Ganger, Phillip B. Gibbons, Onur Mutlu, "Gaia: Geo-Distributed Machine Learning Approaching LAN Speeds," *Proceedings of the 14th USENIX Symposium on Networked Systems Design and Implementation (**NSDI**)*, Boston, MA, USA, March 2017.
10. Onur Mutlu, "The RowHammer Problem and Other Issues We May Face as Memory Becomes Denser," *Proceedings of the Design, Automation, and Test in Europe Conference (**DATE**)*, Lausanne, Switzerland, March 2017. **Invited Paper and Presentation.**
11. Aya Fukami, Saugata Ghose, Yixin Luo, Yu Cai, Onur Mutlu, "Improving the Reliability of Chip-Off Forensic Analysis of NAND Flash Memory Devices," *Proceedings of the Digital Forensics Conference (**DFRWS EU**)*, Lake Constance, Germany, March 2017.
12. Hasan Hassan, Nandita Vijaykumar, Samira Khan, Saugata Ghose, Kevin Chang, Gennady Pekhimenko, Donghyuk Lee, Oguz Ergin, Onur Mutlu, "SoftMC: A Flexible and Practical Open-Source Infrastructure for Enabling Experimental DRAM Studies," *Proceedings of the 23rd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Austin, TX, USA, February 2017.
13. Yu Cai, Saugata Ghose, Yixin Luo, Ken Mai, Onur Mutlu, Erich F. Haratsch, "Vulnerabilities in MLC NAND Flash Memory Programming: Experimental Analysis, Exploits, and Mitigation Techniques," *Proceedings of the 23rd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Austin, TX, USA, February 2017.
14. Khanh Nguyen, Lu Fang, Guoqing Xu, Brian Demsky, Shan Lu, Sanazsadat Alamian, Onur Mutlu, "Yak: A High-Performance Big-Data-Friendly Garbage Collector," *Proceedings of the 12th USENIX Symposium on Operating Systems Design and Implementation (**OSDI**)*, Savannah, GA, USA, November 2016.
15. Himanshu Chauhan, Irina Calciu, Vijay Chidambaram, Eric Schkufza, Onur Mutlu, Pratap Subrahmanyam, "NVMove: Helping Programmers Move to Byte-Based Persistence," *4th Workshop on Interactions of NVM/Flash with Operating Systems and Workloads (**INFLOW**)*, Savannah, GA, USA, November 2016.
16. Nandita Vijaykumar, Kevin Hsieh, Gennady Pekhimenko, Samira Khan, Saugata Ghose, Ashish Shreshtha, Adwait Jog, Phillip P. Gibbons, Onur Mutlu, "Proteus: Enhancing Programming Ease, Portability, and Performance with Fluid GPU Resources," *Proceedings of the 49th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, Taipei, Taiwan, October 2016.
17. Milad Hashemi, Onur Mutlu, Yale N. Patt, "Continuous Runahead: Transparent Hardware Acceleration for Memory Intensive Workloads," *Proceedings of the 49th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, Taipei, Taiwan, October 2016. **Best Paper Session.**
18. Kevin Hsieh, Samira Khan, Nandita Vijaykumar, Kevin K. Chang, Amirali Boroumand, Saugata Ghose, Onur Mutlu, "Accelerating Pointer Chasing in 3D-Stacked Memory: Challenges, Mechanisms, Evaluation," *Proceedings of the 34th IEEE International Conference on Computer Design (**ICCD**)*, Phoenix, AZ, USA, October 2016.
19. Xiyue Xiang, Saugata Ghose, Onur Mutlu, Nian-Feng Tzeng, "A Model for Application Slowdown Estimation in On-Chip Networks and Its Use for Improving System Fairness and Performance," *Proceedings of the 34th IEEE International Conference on Computer Design (**ICCD**)*, Phoenix, AZ, USA, October 2016.
20. Ashutosh Pattnaik, Xulong Tang, Adwait Jog, Onur Kayiran, Asit K. Mishra, Mahmut T. Kandemir, Onur Mutlu, Chita R. Das, "Scheduling Techniques for GPU Architectures with Processing-In-Memory Capabilities," *Proceedings of the 25th ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, Haifa, Israel, September 2016.
21. Onur Kayiran, Adwait Jog, Ashutosh Pattnaik, Rachata Ausavarungnirun, Xulong Tang, Mahmut T. Kandemir, Gabriel H. Loh, Onur Mutlu, Chita R. Das, "μC-States: Fine-grained GPU Datapath Power Management," *Proceedings of the 25th ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, Haifa, Israel, September 2016.
22. Samira Khan, Donghyuk Lee, Onur Mutlu, "PARBOR: An Efficient System-Level Technique to Detect Data-Dependent Failures in DRAM," *Proceedings of the 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN**)*, Toulouse, France, June 2016.
23. Kevin Hsieh, Eiman Ebrahimi, Gwangsun Kim, Niladrish Chatterjee, Mike O'Connor, Nandita Vijaykumar, Onur Mutlu, Stephen W. Keckler, "Transparent Offloading and Mapping (TOM): Enabling Programmer-Transparent Near-Data Processing in GPU Systems," *Proceedings of the 43rd International Symposium on Computer Architecture (**ISCA**)*, Seoul, South Korea, June 2016.
24. Milad Hashemi, Khubaib, Eiman Ebrahimi, Onur Mutlu, Yale N. Patt, "Accelerating Dependent Cache Misses with an Enhanced Memory Controller," *Proceedings of the 43rd International Symposium on Computer Architecture (**ISCA**)*, Seoul, South Korea, June 2016.

25. Kevin Chang, Abhijith Kashyap, Hasan Hassan, Samira Khan, Kevin Hsieh, Donghyuk Lee, Saugata Ghose, Gennady Pekhimenko, Tianshi Li, Onur Mutlu, "Understanding Latency Variation in Modern DRAM Chips: Experimental Characterization, Analysis, and Optimization," *Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems (**SIGMETRICS**)*, Antibes Juan-Les-Pins, France, June 2016.
26. Adwait Jog, Onur Kayiran, Ashutosh Pattnaik, Mahmut T. Kandemir, Onur Mutlu, Ravishankar Iyer, and Chita R. Das, "Exploiting Core Criticality for Enhanced GPU Performance," *Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems (**SIGMETRICS**)*, Antibes Juan-Les-Pins, France, June 2016.
27. Wayne Burleson, Onur Mutlu, Mohit Tiwari, "Who Is the Major Threat to Tomorrow's Security? You, the Hardware Designer," *Proceedings of the 53rd Design Automation Conference (**DAC**)*, Austin, TX, USA, June 2016. **Invited Paper and Presentation.**
28. Yang Li, Di Wang, Saugata Ghose, Jie Liu, Sriram Govindan, Sean James, Eric Peterson, John Siegler, Rachata Ausavarungnirun, Onur Mutlu, "SizeCap: Efficiently Handling Power Surges in Fuel Cell Powered Data Centers," *Proceedings of the 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Barcelona, Spain, March 2016.
29. Kevin K. Chang, Prashant J. Nair, Saugata Ghose, Donghyuk Lee, Moinuddin K. Qureshi, Onur Mutlu, "Low-Cost Inter-Linked Subarrays (LISA): Enabling Fast Inter-Subarray Data Movement in DRAM," *Proceedings of the 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Barcelona, Spain, March 2016.
30. Hasan Hassan, Gennady Pekhimenko, Nandita Vijaykumar, Vivek Seshadri, Donghyuk Lee, Oguz Ergin, Onur Mutlu, "ChargeCache: Reducing DRAM Latency by Exploiting Row Access Locality,"*Proceedings of the 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Barcelona, Spain, March 2016.
31. Gennady Pekhimenko, Evgeny Bolotin, Nandita Vijaykumar, Onur Mutlu, Todd C. Mowry, Stephen W. Keckler, "A Case for Toggle-Aware Compression for GPU Systems,"*Proceedings of the 22nd IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Barcelona, Spain, March 2016.
32. Lavanya Subramanian, Vivek Seshadri, Arnab Ghosh, Samira Khan, Onur Mutlu, "The Application Slowdown Model: Quantifying and Controlling the Impact of Inter-Application Interference at Shared Caches and Main Memory," *Proceedings of the 48th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, Waikiki, Hawaii, December 2015.
33. Vivek Seshadri, Thomas Mullins, Amirali Boroumand, Onur Mutlu, Phillip B. Gibbons, Michael A. Kozuch, Todd C. Mowry, "Gather-Scatter DRAM: In-DRAM Address Translation to Improve the Spatial Locality of Non-unit Strided Accesses," *Proceedings of the 48th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, Waikiki, Hawaii, December 2015.
34. Jinglei Ren, Jishen Zhao, Samira Khan, Jongmoo Choi, Yongwei Wu, Onur Mutlu, "ThyNVM: Enabling Software-Transparent Crash Consistency in Persistent Memory Systems," *Proceedings of the 48th IEEE/ACM International Symposium on Microarchitecture (**MICRO**)*, Waikiki, Hawaii, December 2015.
35. Donghyuk Lee, Lavanya Subramanian, Rachata Ausavarungnirun, Jongmoo Choi, Onur Mutlu, "Decoupled Direct Memory Access: Isolating CPU and I/O Traffic by Leveraging a Dual-Port DRAM," *Proceedings of the 24th ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, San Francisco, CA, October 2015.
36. Rachata Ausavarungnirun, Onur Kayiran, Saugata Ghose, Gabriel Loh, Chita Das, Mahmut Kandemir, Onur Mutlu, "Exploiting Inter-Warp Heterogeneity to Improve GPGPU Performance," *Proceedings of the 24th ACM International Conference on Parallel Architectures and Compilation Techniques (**PACT**)*, San Francisco, CA, October 2015.
37. Mohammad Fattah, Antti Airola, Rachata Ausavarungnirun, Nima Mirzaei, Pasi Liljeberg, Juha Plosila, Siamak Mohammadi, Tapio Pahikkala, Onur Mutlu, Hannu Tenhunen, "A Low-Overhead, Fully-Distributed, Guaranteed-Delivery Routing Algorithm for Faulty Network-on-Chips," *Proceedings of the 9th International Networks-On-Chip Symposium (**NOCS**)*, Vancouver, BC, Canada, September 2015. **One of the 3 papers nominated for the Best Paper Award by the Program Committee.**
38. Nandita Vijaykumar, Gennady Pekhimenko, Adwait Jog, Abhishek Bhowmick, Rachata Ausavarungnirun, Chita Das, Mahmut Kandemir, Todd C. Mowry, Onur Mutlu,"A Case for Core-Assisted Bottleneck Acceleration in GPUs: Enabling Efficient Data Compression with Assist Warps," *Proceedings of the 42nd International Symposium on Computer Architecture (**ISCA**)*, Portland, OR, June 2015.
39. Vivek Seshadri, Gennady Pekhimenko, Olatunji Ruwase, Onur Mutlu, Phillip Gibbons, Michael Kozuch, Todd C. Mowry, Trishul Chilimbi, "Page Overlays: An Enhanced Virtual Memory Framework to Enable Fine-grained Memory Management," *Proceedings of the 42nd International Symposium on Computer Architecture (**ISCA**)*, Portland, OR, June 2015.
40. Junwhan Ahn, Sungjoo Yoo, Onur Mutlu, Kiyoung Choi, "PIM-Enabled Instructions: A Low-Overhead, Locality-Aware Processing-in-Memory Architecture," *Proceedings of the 42nd International Symposium on Computer Architecture (**ISCA**)*, Portland, OR, June 2015.
41. Junwhan Ahn, Sungpack Hong, Sungjoo Yoo, Onur Mutlu, Kiyoung Choi, "A Scalable Processing-in-Memory Accelerator for Parallel Graph Processing," *Proceedings of the 42nd International Symposium on Computer Architecture (**ISCA**)*, Portland, OR, June 2015. **IEEE Micro Top Picks Honorable Mention.**
42. Justin Meza, Qiang Wu, Sanjeev Kumar, Onur Mutlu, "A Large-Scale Study of Flash Memory Failures in the Field," *Proceedings of the ACM International Conference on Measurement and Modeling of Computer Systems (**SIGMETRICS**)*, Portland, OR, June 2015.
43. Yu Cai, Yixin Luo, Saugata Ghose, Onur Mutlu, "Read Disturb Errors in MLC NAND Flash Memory: Characterization and Mitigation," *Proceedings of the 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN**)*, Rio De Janeiro, Brazil, June 2015.

44. Justin Meza, Qiang Wu, Sanjeev Kumar, Onur Mutlu, "Revisiting Memory Errors in Large-Scale Production Data Centers: Analysis and Modeling of New Trends from the Field," *Proceedings of the 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN**)*, Rio De Janeiro, Brazil, June 2015.
45. Moinuddin Qureshi, Dae Hyun Kim, Samira Khan, Prashant Nair, Onur Mutlu, Chris Wilkerson, "AVATAR: A Variable-Retention-Time (VRT) Aware Refresh for DRAM Systems," *Proceedings of the 45th Annual IEEE/IFIP International Conference on Dependable Systems and Networks (**DSN**)*, Rio De Janeiro, Brazil, June 2015.
46. Yixin Luo, Yu Cai, Saugata Ghose, Jongmoo Choi, Onur Mutlu, "WARM: Improving NAND Flash Memory Lifetime with Write-hotness Aware Retention Management," *Proceedings of the 31st International Conference on Massive Storage Systems and Technologies (**MSST**)*, Santa Clara, CA, June 2015.
47. Dongwoo Kang, Seungjae Baek, Jongmoo Choi, Donghee Lee, Sam H. Noh, Onur Mutlu, "Amnesic Cache Management for Non-Volatile Memory,"*Proceedings of the 31st International Conference on Massive Storage Systems and Technologies (**MSST**)*, Santa Clara, CA, June 2015.
48. Hui Wang, Canturk Isci, Lavanya Subramanian, Jongmoo Choi, Depei Qian, Onur Mutlu, "A-DRM: Architecture-aware Distributed Resource Management of Virtualized Clusters," *Proceedings of the 11th ACM SIGPLAN/SIGOPS International Conference on Virtual Execution Environments (**VEE**)*, Istanbul, Turkey, March 2015.
49. Yu Cai, Ken Mai, Onur Mutlu, "Comparative Evaluation of FPGA and ASIC Implementations of Bufferless and Buffered Routing Algorithms for On-Chip Networks," *Proceedings of the 16th International Symposium on Quality Electronic Design (**ISQED**)*, Santa Clara, CA, March 2015.
50. Yu Cai, Yixin Luo, Erich F. Haratsch, Ken Mai, Onur Mutlu, "Data Retention in MLC NAND Flash Memory: Characterization, Optimization and Recovery," *Proceedings of the 21st IEEE International Symposium on High Performance Computer Architecture (**HPCA**)*, Bay Area, CA, February 2015. **Best Paper Session.**
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151. Yixin Luo, Saugata Ghose, Yu Cai, Erich F. Haratsch, Onur Mutlu, "Enabling Accurate and Practical Online Flash Channel Modeling for Modern MLC NAND Flash Memory," ***IEEE Journal on Selected Areas in Communications (JSAC)***, September 2016.
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195. Onur Mutlu, Rich Belgard, "Common Bonds: MIPS, HPS, Two-Level Branch Prediction, and Compressed Code RISC Processor," ***IEEE Micro***, July/August 2016.
196. Onur Mutlu, Rich Belgard, "The 2014 MICRO Test of Time Award Winners: From 1978 to 1992," ***IEEE Micro***, January/February 2016.
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200. Damla Senol, Jeremie Kim, Saugata Ghose, Can Alkan, Onur Mutlu, "Nanopore Sequencing Technology and Tools: Computational Analysis of the Current State, Bottlenecks and Future Directions," *Pacific Symposium on Biocomputing (**PSB**) Poster Session*, Hawaii, January 2016.
201. Jeremie Kim, Damla Senol, Hongyi Xin, Donghyuk Lee, Mohammed Alser, Hasan Hassan, Oguz Ergin, Can Alkan, Onur Mutlu, "Genome Read In-Memory (GRIM) Filter: Fast Location Filtering in DNA Read Mapping using Emerging Memory Technologies," *Pacific Symposium on Biocomputing (**PSB**) Poster Session*, Hawaii, January 2016.
202. Onur Mutlu, "ThyNVM: Software-Transparent Crash Consistency for Persistent Memory," *Proceedings of the Flash Memory Summit **(FMS)***, Santa Clara, CA, August 2016.
203. Onur Mutlu, "Large-Scale Study of In-the-Field Flash Failures," *Proceedings of the Flash Memory Summit **(FMS)***, Santa Clara, CA, August 2016.
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205. Jeremie Kim, Damla Senol, Hongyi Xin, Donghyuk Lee, Mohammed Alser, Hasan Hassan, Oguz Ergin, Can Alkan, Onur Mutlu, "Genome Read In-Memory (GRIM) Filter: Fast Location Filtering in DNA Read Mapping with Emerging Memory Technologies," *Flash Talk and Poster at 20th Annual International Conference on Research in Computational Molecular Biology (**RECOMB**)*, Santa Monica, CA, USA, April 2016.
206. Onur Mutlu, "Read Disturb Errors in MLC NAND Flash Memory," *Proceedings of the Flash Memory Summit **(FMS)***, Santa Clara, CA, August 2015.
207. Hongyi Xin, Richard Zhu, Sunny Nahar, John Emmons, Gennady Pekhimenko, Carl Kingsford, Can Alkan, Onur Mutlu, "Optimal Seed Solver: Optimizing Seed Selection in Read Mapping," *Poster at High Throughput Sequencing Algorithms and Applications (**HITSEQ**)*, Dublin, Ireland, July 2015.
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209. Gennady Pekhimenko, Todd C. Mowry, Onur Mutlu, "Energy-Efficient Data Compression for GPU Memory Systems," *Short Student Research Competition paper at the 20th International Conference on Architectural Support for Programming Languages and Operating Systems (**ASPLOS**)*, Istanbul, Turkey, March 2015. **First place in ACM Student Research Competition.**
210. Onur Mutlu, "Error Analysis and Management for MLC NAND Flash Memory," *Proceedings of the Flash Memory Summit **(FMS)***, Santa Clara, CA, August 2014.
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212. Hongyi Xin, John Greth, John Emmons, Gennady Pekhimenko, Carl Kingsford, Can Alkan, Onur Mutlu, "Shifted Hamming Distance (SHD): A Fast and Accurate SIMD-Friendly Filter for Local Alignment in Read Mapping," *Poster at High Throughput Sequencing Algorithms and Applications (**HITSEQ**)*, Boston, MA, July 2014.
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234. Chang Joo Lee, Veynu Narasiman, Eiman Ebrahimi, Onur Mutlu, Yale N. Patt, "DRAM-Aware Last-Level Cache Writeback: Reducing Write-Caused Interference in Memory Systems," HPS Technical Report, TR-HPS-2010-002, April 2010.
235. Onur Mutlu, "Efficient Runahead Execution Processors," Ph.D. Dissertation, HPS Technical Report, TR-HPS-2006-007, July 2006. **Nominated for the ACM Doctoral Dissertation Award by the University of Texas at Austin**

Patents and Invention Disclosures (filed while in Industry)

1. William H. Mangione Smith, Onur Mutlu, "Reliable Communications in On-chip Networks," US Patent 8473818, June 2013.
2. Thomas Moscibroda, Onur Mutlu, "Bufferless Routing in On-Chip Interconnection Networks," US Patent 8509078, August 2013.
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4. Thomas Moscibroda, Onur Mutlu, "Coordination among Multiple Memory Controllers," US Patent 8266393, September 2012.
5. Thomas Moscibroda, Onur Mutlu, "Controlling Interference in Shared DRAM Systems using Batch Scheduling," US Patent 8180975, May 2012.
6. Onur Mutlu, José A. Joao, "Feedback Mechanism for Dynamic Predication of Indirect Jumps," US Patent 7818551, October 2010.
7. José A. Joao, Onur Mutlu, "Target-Frequency based Indirect Jump Prediction for High-Performance Processors," US Patent 7870371, January 2011.
8. Onur Mutlu, Thomas Moscibroda, "A Software-Configurable and Stall-Time Fair Memory Access Scheduling Mechanism for Shared Memory Systems," US Patent 8245232, August 2012.
9. Thomas Moscibroda, Onur Mutlu, "Multi-level DRAM Controller to Manage Access to DRAM," US Patent 8001338, August 2011.
10. Onur Mutlu, Thomas Moscibroda, "Parallelism-Aware Memory Request Scheduling in Shared Memory Controllers," US Patent Application filed August 2007.
11. Thomas Moscibroda, Onur Mutlu, "Fairness in Memory Systems," US Patent Application filed July 2007.
12. Jared Stark, Chris Wilkerson, Onur Mutlu,"Apparatus for Memory Communication During Runahead Execution," US Patent Application filed December 2002.
13. Eric Sprangle, Onur Mutlu, "Method and Apparatus to Control Memory Accesses," US Patent 6799257, September 2004.

Invited Talks and Lectures

(Please visit `https://people.inf.ethz.ch/omutlu/talks.htm` for some electronic copies.)

1. "Solving the Memory Problem"
   - ETH Systems Group Industry Retreat, Engelberg, Switzerland, 18 January 2016.
   - ETH Systems Group Industry Retreat, Engelberg, Switzerland, 30 January 2017.
2. "Rethinking Memory System Design (and the Computing Platforms We Design Around It)" or "Rethinking Memory Systems: Challenges and Opportunities" or "Rethinking Memory System Design (for Data-Intensive Computing)" or "Memory Scaling: A Systems Architecture Perspective" (many variants on the same theme with varying content)
   - **Special invited talk** at the 5th IEEE International Memory Workshop, Monterey, CA, 27 May 2013.
   - MemCon, San Jose, CA, 6 August 2013.
   - Facebook, Menlo Park, CA, 7 August 2013.
   - Huawei, Sonoma, CA, 8 August 2013.
   - Samsung, San Jose, 9 September 2013.
   - Intel Science and Technology Center for Cloud Computing Retreat, Pittsburgh, PA, 8 November 2013.
   - IBM Research, Yorktown Heights, NY, 12 November 2013.
   - D.E. Shaw Research, New York, NY, 13 November 2013.
   - Intel Memory Hierarchy Workshop, Hillsboro, OR, 5 December 2013.
   - **Keynote talk** at Industry-Academia Partnership Stanford Cloud Workshop, Mountain View, CA, 6 December 2013.
   - Columbia University, New York, NY, 11 March 2014.
   - **Keynote talk** at Huawei Strategy and Technology Workshop, Santa Clara, CA, 18 March 2014.
   - **Keynote talk** at Industry-Academia Partnership Carnegie Mellon Cloud Workshop, Pittsburgh, PA, 4 April 2014.
   - New York University, Brooklyn, NY, 24 April 2014.
   - **Opening talk** at Future Memory Systems Workshop, Carnegie Mellon University, Pittsburgh, PA, 7 May 2014.
   - **Keynote talk** at Huawei Strategy and Technology Workshop, Shenzhen, China, 14 May 2014.
   - **Keynote talk** at the 9th International Conference on Green, Pervasive and Cloud Computing, Wuhan, China, 27 May 2014.
   - **Keynote talk** at the 25th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), Zürich, Switzerland, 20 June 2014.
   - ETH Zürich, Zürich, Switzerland, 23 June 2014.
   - **Plenary talk** at the Summer Supercomputing Academy, Moscow State University, Moscow, Russia, 2 July 2014.
   - Marmara University, Istanbul, Turkey, 9 July 2014.
   - Microsoft Research, Redmond, WA, 17 July 2014.
   - Google, Mountain View, CA, 23 July 2014.
   - Huawei, Santa Clara, CA, 6 August 2014.
   - International Summer School of AP Education Consortium, Hsinchu, Taiwan, 11 August 2014.
   - National Taiwan University, Taipei, Taiwan, 14 August 2014.
   - MediaTek, Hsinchu, Taiwan, 15 August 2014.
   - ARM, Austin, TX, 20 August 2014.
   - Broadcom, Santa Clara, CA, 21 August 2014.
   - SanDisk, San Jose, CA, 22 August 2014.
   - Micron, Boise, ID, 26 September 2014.
   - Hanyang University, Seoul, Korea, 21 October 2014.
   - SK Hynix, Korea, 23 October 2014.
   - Samsung, Korea, 24 October 2014.
   - Carnegie Mellon University Parallel Data Laboratory Retreat Opening Talk, 27 October 2014.
   - Northwestern University, Evanston, IL, 10 November 2014.
   - **Keynote talk** at the 4th Workshop on Irregular Applications: Architectures and Algorithms, held with Supercomputing (SC), New Orleans, LA, 17 November 2014.
   - Bogazici University, Istanbul, Turkey, 6 January 2015.

- Koc University, Istanbul, Turkey, 13 March 2015.
- Intel, Hillsboro, OR, 5 May 2015.
- ETH Zürich, Zürich, Switzerland, 11 May 2015.
- **Keynote talk** at 11th International Workshop on Data Management on Novel Hardware (DaMoN) with SIGMOD, Melbourne, Australia, 1 June 2015.
- University of Melbourne, Melbourne, Australia, 2 June 2015.
- Australian National University, Canberra, Australia, 3 June 2015.
- University of New South Wales and National Information and Communications Technology Research Centre of Excellence, Sydney, Australia, 4 June 2015.
- HP Labs, Palo Alto, CA, 25 June 2015.
- **Special invited talk** at ISC High Performance (International Supercomputing Conference), Frankfurt, Germany, 14 July 2015.
- SAP, Walldorf, Germany, 16 July 2015.
- **Keynote talk** at SAMOS XV (15th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation), Samos, Greece, 20 July 2015.
- Bilkent University, Ankara, Turkey, 29 July 2015.
- Turku Center for Computer Science, Turku, Finland, 18 August 2015.
- KTH - Swedish Royal Institute of Technology, Stockholm, Sweden, 24 August 2015.
- Yale University, New Haven, CT, 10 September 2015.
- University of British Columbia, Vancouver, BC, Canada, 17 September 2015.
- Apple, Inc., Cupertino, CA, 22 September 2015.
- Stanford University (Systems Seminar), Palo Alto, CA, 23 September 2015.
- **Keynote talk** at the 18th International Symposium on Computer Architecture and Digital Systems (CADS), 7 October 2015.
- **Keynote talk** at the 27th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD), Florianopolis, Brazil, 21 October 2015.
- **Keynote talk** at the 5th IEEE Circuits and Systems Society Workshop (CASS), Porto Alegre, Brazil, 22 October 2015.
- University of Campinas (UNICAMP), Campinas, Brazil, 23 October 2015.
- SAP, Dublin, CA, 6 November 2015.
- VMware, Palo Alto, CA, 10 November 2015.
- University of Chicago, Chicago, IL, 16 November 2015.
- Kadir Has University, Istanbul, Turkey, 23 December 2015.
- TOBB Economics and Technology University, Ankara, Turkey, 4 January 2016.
- Istanbul Technical University, Istanbul, Turkey, 6 January 2016.
- VMware, Palo Alto, CA, 3 March 2016.
- **Distinguished lecture** at Triangle Computer Science Distinguished Lecture Series, Raleigh, NC, 11 April 2016.
- University of California, Irvine, CA, 22 April 2016.
- ARM, Austin, TX, 10 June 2016.
- Intel, Austin, TX, 10 June 2016.
- **Keynote talk** at the ACM SIGPLAN International Symposium on Memory Management (ISMM), Santa Barbara, CA, 14 June 2016.
- Stony Brook University, Stony Brook, NY, USA, 13 July 2016.
- SK Telecom, Seoul, Korea, 16 August 2016.
- **Keynote talk** at the First ARM Research Summit, Cambridge, UK, 15 September 2016.
- **Keynote talk** at the 2nd Workshop on Mobile System Technologies (MST), Milan, Italy, 23 September 2016.
- **Keynote talk** at the 27th International Symposium on Rapid System Prototyping (RSP), Pittsburgh, PA, USA, 6 October 2016.
- **Keynote talk** at the 2nd EAI International Conference on Future Access Enablers of Ubiquitous and Intelligent Infrastructures (FABULOUS), Belgrade, Serbia, 24 October 2016.
- IBM Research Zürich, Ruschlikon, Switzerland, 2 November 2016.
- Xilinx, San Jose, CA, 8 December 2016.
- Intel Labs, Santa Clara, CA, 9 December 2016.
- TU Dresden, Dresden, Germany, 27 February 2017.
- **Special Invited talk** at the Dagstuhl Seminar "Databases on Future Hardware", Germany, 9 March 2017.

3. "Rethinking Memory System Design (along with Interconnects)"
   - **Keynote talk** at the 8th International Workshop on Network on Chip Architectures (NoCArc), Honolulu, Hawaii, 5 December 2015.

4. Short Course on "Memory Systems" or "Memory Systems in the Multi-Core Era (An Accelerated Course)" or "Scalable Memory Systems in the Multi-Core Era" or "Rethinking Memory Systems Design"
   - Beihang University, 3-day Lecture Series (16 hours), Beijing, China, June 17, 25, 26, 2012.
   - Seoul National University, 2-day Lecture Series (6 hours), Seoul, Korea, June 18, 20, 2012. (Memory Scaling and Memory QoS)
   - Bogazici University, 3-day Lecture Series (15 hours), Istanbul, Turkey, June 13, 14, 17, 2013.
   - INRIA Rennes, 3-day Lecture Series (6 hours), July 4, 8, 9, 2013.
   - HiPEAC ACACES Summer School (6 hours), Fiuggi, Italy, July 15-19, 2013.
   - Turku Center for Computer Science (16 hours), Turku, Finland, August 19-21, 2015.
   - Pohang Institute of Science and Technology - POSTECH (7 hours), Pohang, Korea, 17-18 August 2016.
   - Korea Advanced Institute of Science and Technology - KAIST (7 hours), Daejeon, Korea, 19 August 2016.

5. "Processing Data Where It Makes Sense: Enabling In-Memory Computation"
   - Bogazici University, Istanbul, Turkey, 6 August 2015.
   - Google, Mountain View, CA, 9 November 2015.
   - Intel, Hillsboro, OR, 10 January 2017.

6. "Opportunities and Challenges of New Memory Technologies"
   - Samsung MRAM Global Innovation Forum, San Jose, CA, 11 November 2015.
7. "Reliability and Security Issues of DRAM and NAND Flash Scaling"
   - Memory Reliability Forum at HPCA, Barcelona, Spain, 13 March 2016.
   - SNU International Workshop on Recent Advances in Neural Networks and Non-Volatile Memory, Seoul, Korea, 16 August 2016.
8. "The RowHammer Problem and Other Issues We May Face as Memory Becomes Denser" or "The DRAM RowHammer Problem (and Its Reliability and Security Implications)"
   - Carnegie Mellon University CyLab Partners Conference, Pittsburgh, PA, 30 September 2015.
   - JEDEC RowHammer Task Force, 2 December 2015.
   - **Special Invited Talk** at the Design Automation Conference (DAC), 9 June 2016.
9. "ThyNVM: Software-Transparent Crash Consistency for Persistent Memory"
   - Flash Memory Summit, Santa Clara, CA, 8 August 2016.
   - Google, Mountain View, CA, 22 August 2016.
10. "Large-Scale Study of In-the-Field Flash Failures"
    - Flash Memory Summit, Santa Clara, CA, 10 August 2016.
11. "Read Disturb Errors in MLC NAND Flash Memory"
    - Flash Memory Summit, Santa Clara, CA, 12 August 2015.
12. "Rethinking the Systems We Design"
    - Visions for the Future (Celebrating Yale@75) Workshop, UT-Austin, TX, 19 September 2014.
13. "A Case for Autonomous Memory"
    - Google Systems Research Workshop, San Francisco, CA, 26 June 2015.
14. "Integrated Techniques for Scalable Management of Main Memory Performance, Energy, and QoS"
    - SRC (Semiconductor Research Corporation) Annual Review, Intel, Hillsboro, OR, 1 May 2013.
    - SRC (Semicaonductor Research Corporation) Annual Review, Carnegie Mellon University, Pittsburgh, PA, 6 May 2014.
    - SRC (Semiconductor Research Corporation) Annual Review, Intel, Hillsboro, OR, 6 May 2015.
    - SRC (Semiconductor Research Corporation) Annual Review, Intel, Hillsboro, OR, 29 April 2016.
    - Google, Mountain View, CA, 20 July 2016.
15. "Error Analysis and Management for MLC NAND Flash Memory"
    - Flash Memory Summit (45-minute talk), Santa Clara, CA, 7 August 2014.
16. "Some New Ideas in Memory System Design for Data-Intensive Computing"
    - Intel Science and Technology Center for Cloud Computing Retreat, Hillsboro, OR, 4 September 2014.
17. "A Fresh Look at DRAM Architecture: New Techniques to Improve DRAM Latency, Parallelism, and Energy Efficiency"
    - MIT, Cambridge, MA, 22 May 2013.
    - INRIA Rennes, 4 July 2013.
    - Intel Memory Hierarchy Workshop, Hillsboro, OR, 13 March 2014.
18. "Enabling Low-Latency DRAM Architectures"
    - Intel Low Latency Architectures Workshop, Hillsboro, OR, 2 December 2016.
    - Intel Low Latency Architectures Workshop, Hillsboro, OR, 11 December 2015.
    - Intel Low Latency Architectures Workshop, Hillsboro, OR, 7 November 2014.
19. "Understanding and Overcoming Challenges of DRAM Refresh"
    - Extreme Scale Scientific Computing Workshop, Moscow, Russia, 30 June 2014.
20. "Multi-core Architectures and Shared Resource Management: Fundamentals and Recent Research"
    - Seoul National University, Lecture Series (12 hours), Seoul, Korea, July 6-9, 2010.
    - Korea Advanced Institute of Science and Technology, Global Lecture Series (15 hours), Daejeon, Korea, July 26-29, 2010.
    - Beihang University, 2-day Lecture Series (13 hours), Beijing, China, August 9, 12, 2011.
    - Bogazici University, 3-day Lecture Series (15 hours), Istanbul, Turkey, June 6, 7, 10, 2013.
21. "Scaling the Main Memory System in the Many-Core Era" or "Main Memory Scaling: Some Ideas to Improve DRAM and Enable Hybrid Memory Systems" or "Main Memory Scaling: Some Challenges and Solution Directions"
    - IBM, Poughkeepsie, NY, 21 May 2012.
    - Invited Talk, ACM Design Automation Conference More Than Moore Technologies Workshop, San Francisco, CA, 3 June 2012.
    - Samsung Information Systems America, San Jose, CA, 4 June 2012.
    - Rambus, Sunnyvale, CA, 5 June 2012.
    - POSTECH, Pohang, Korea, 19 June 2012.
    - Samsung, Memory Division, Hwasung City, Korea, 21 June 2012.
    - SK Hynix, Seoul, Korea, 23 June 2012.
    - **Distinguished lecture** at Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, 28 June 2012.
    - Intel, Hillsboro, OR, 26 July 2012.
    - Advanced Micro Devices, Austin, TX, 21 September 2012.
    - McGill University, Montreal, Quebec, Canada, 1 October 2012.
    - Sabanci University, Istanbul, Turkey, 4 January 2013.

- Nvidia, Austin, TX, 22 March 2013.
- EMC, Hopkinton, MA, 20 May 2013.
- Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, Barcelona, Spain, 26 July 2013.
- Nvidia, Santa Clara, CA, 5 August 2013.

22. "Architecting and Exploiting Asymmetry in Multi-Core Architectures"
    - Intel, Santa Clara, CA, 9 March 2011.
    - Rambus, Sunnyvale, CA, 5 June 2012.
    - Samsung, System LSI Division, Hwasung City, Korea, 22 June 2012.
    - Intel, Hillsboro, OR, 26 July 2012.
    - Advanced Micro Devices, Bellevue, WA, 3 August 2012.
    - Intel Archfest, Hillsboro, OR, 10 August 2012.
    - Intel Science and Technology Center on Cloud Computing Board of Advisors Meeting, Pittsburgh, PA, 16 August 2012.
    - Intel Science and Technology Center on Cloud Computing Retreat, Pittsburgh, PA, 29 November 2012.
    - Bogazici University, Istanbul, Turkey, 26 December 2012.
    - Bilkent University, Ankara, Turkey, 28 December 2012.
    - EMC, Hopkinton, MA, 20 May 2013.
    - TUBITAK, Gebze, Turkey, 19 June 2013.
    - INRIA Rennes, Rennes, France, 2 July 2013.
    - Barcelona Supercomputing Center and Universitat Politecnica de Catalunya, Barcelona, Spain, 23 July 2013.
    - International Summer School of AP Education Consortium, Hsinchu, Taiwan, 11 August 2014.
    - International Workshop on Heterogeneous Computing Platforms, held with ICCAD, San Jose, CA, 6 November 2014.

23. "Some Ideas in Designing Scalable and Efficient Multi-Core Systems"
    - Apple, Cupertino, CA, 6 June 2012.

24. "Concurrent Autonomous Self-Test for Uncore Components in SoCs"
    - SK Hynix, Seoul, Korea, 23 June 2012.

25. "Designing QoS-Aware Memory Systems" or "Predictable Memory Systems for the Many-Core Era"
    - IBM, Poughkeepsie, NY, 21 May 2012.
    - SK Hynix, Seoul, Korea, 23 June 2012.
    - Intel, Hillsboro, OR, 1 August 2012.
    - VMware, Palo Alto, CA, 17 October 2012.

26. "Main Memory Issues (Both Volatile and Non-Volatile)"
    - Carnegie Mellon University Parallel Data Lab Retreat, Bedford, PA, 6 November 2012.
    - Carnegie Mellon University Parallel Data Lab Visit Day, Pittsburgh, PA, 11 May 2012.

27. "Some (Security-Related) Challenges in Future Computing Platforms"
    - Carnegie Mellon University College of Engineering Deans Council Meeting, Pittsburgh, PA, 26 April 2012.

28. "Some Opportunities and Obstacles in Cross-Layer and Cross-Component (Power) Management"
    - NSF Workshop on Cross-Layer Power Optimization and Management, Los Angeles, CA, 10 February 2012.

29. "Memory Systems in the Many-Core Era: Challenges, Opportunities, and Solution Directions"
    - **Joint Keynote Talk**, International Symposium on Memory Management (ISMM) and ACM Workshop on Memory System Performance and Correctness (MSPC), San Jose, CA, 5 June 2011.
    - Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China, 10 August 2011.
    - Tsinghua University, Beijing, China, 11 August 2011.
    - Microsoft Research Asia, Beijing, China, 15 August 2011.
    - Massachusetts Institute of Technology, 4 November 2011.
    - University of California at Berkeley (PARLAB seminar), 15 November 2011.

30. "Issues in DRAM and NVM based Main Memory"
    - Carnegie Mellon University Parallel Data Lab Retreat, Bedford Springs, PA, 8 November 2011.

31. "Computer 'Performance"'
    - Carnegie Mellon University ECE Department Advisory Board Presentation, 21 September 2011.

32. "Application-Aware Memory Controllers" or "Thread Cluster Memory Scheduling"
    - Xilinx Labs, San Jose, CA, 8 June 2011.
    - Gigascale Systems Research Center Mid-Year Review, Yorktown Heights, NY, 27 May 2011.

33. "Architecture and System-Level Challenges Related to Memory"
    - Focus Center Research Program Memory Cross-Cut Workshop, Cambridge, MA, 12 May 2011.

34. "Towards Practical Bufferless On-Chip Networks"
    - Intel, Santa Clara, CA, 9 March 2011.

35. "Some Ideas for Efficient and High-Performance Core Design"
    - Intel Corporation ARO Swiss Army Processor Workshop, Hillsboro, OR, 29 April 2011.

36. "PCM (NVM) as Main Memory: Opportunities and Challenges"
    - Carnegie Mellon University, Parallel Data Lab Retreat, Pittsburgh, PA, October 25, 2010.

37. "Research Challenges in Future Computing Platforms"
    - Carnegie Mellon University, ECE Department Faculty Retreat, Wheeling, WV, August 12, 2010.
    - Carnegie Mellon University, Sophomore Electrical Engineering Seminar, September 23, 2010.
    - Carnegie Mellon University, ECE/SCS Alumni Event, Austin, TX, March 24, 2013.

38. "End-to-end QoS-aware, High-Performance and Customizable Many-Core Memory Systems"
    - Intel Memory Hierarchy Meeting, Hillsboro, OR, 8 October 2010.

39. "Rethinking Core Design in the Power-Constrained Many-Core Era"
    - Intel Core Workshop, Hillsboro, OR, 27 September 2010.

40. "Some Ideas for ILP Research"
    - CRA Workshop on Advancing Computer Architecture Research, Seattle, WA, 20 September 2010.

41. "Designing High-Performance and Fair Shared Multi-core Memory Systems: Two Approaches" or "QoS-Aware Multi-Core Memory System Management"
    - Gigascale Systems Research Center E-Seminar, 23 March 2010.
    - Pennsylvania State University, CSE Colloquium, 26 March 2010.
    - ARM, Inc., Austin, TX, 8 April 2010.
    - Advanced Micro Devices, Austin, TX, 9 April 2010.
    - Microsoft Research, Redmond, WA, 27 April 2010.
    - HP Laboratories, Palo Alto, CA, 25 May 2010.
    - VMware, Palo Alto, CA, 26 May 2010.
    - Intel Corporation, Hillsboro, OR, 27 May 2010.
    - Gigascale Systems Research Center Annual Review, San Jose, CA, 29 September 2010.
    - Intel Corporation ArchFest, Hillsboro, OR, 8 October 2010.
    - ASPLOS 2011 Program Committee Symposium, Pittsburgh, PA, 22 October 2010.
    - Advanced Micro Devices, Sunnyvale, CA, 10 March 2011.
    - Oracle, Redwood Shores, CA, 11 March 2011.
    - Princeton University, Princeton, NJ, 18 March 2011.

42. "Rethinking Memory System Design in the Nanoscale Many-Core Era"
    - Intel Memory Hierarchy Workshop, Hillsboro, OR, 22 January 2010.
    - ASPLOS Workshop on Architecting Memory Technologies, Pittsburgh, PA, 14 March 2010.

43. "Asymmetry Everywhere (with Automatic Resource Management)"
    - CRA Workshop on Advancing Computer Architecture Research, San Diego, CA, 22 February 2010.

44. "Preventing Memory Performance Attacks in Multi-Core Systems"
    - ECE Seminar, Carnegie Mellon University, 5 February 2009.
    - Massachusetts Institute of Technology, 23 April 2008.
    - Carnegie Mellon University, 15 April 2008.

45. "Parallelism-aware Batch Scheduling: Enhancing both Performance and Fairness of Shared DRAM Systems"
    - IBM Austin Research Laboratory, Austin, TX, 19 June 2009.
    - Advanced Micro Devices Research Lab, Redmond, WA, 6 March 2009.
    - Beihang University, Beijing, China, 21 June 2008.

46. "ATLAS: A Scalable and High-Performance Scheduling Algorithm for Multiple Memory Controllers"
    - Advanced Micro Devices Research Lab, Redmond, WA, October 2009.
    - Freescale Semiconductor, Austin, TX, 8 April 2010.

47. "Memory Performance Attacks and Fair Memory Scheduling"
    - University of British Columbia and IEEE Computer Society, Vancouver, BC, Canada, 6 March 2008.
    - ASPLOS PC Meeting Research Seminar, Microsoft Research, 18 October 2007.
    - Multi-Core Virtual Team Meeting, Microsoft, 5 October 2007.

48. "MSR Computer Architecture Group: Vision and Projects"
    - Presentation to Rico Malvar, MSR-Redmond Director, Microsoft Research, 12 December 2007.

49. "Hardware-Based Devirtualization of Virtual Function Calls"
    - MSR Systems and Networking Seminar, Microsoft Research, 7 December 2006.

50. "Runahead Execution and AVD Prediction: A Power-efficient Processing Paradigm for Tolerating Long Main Memory Latencies"
    - University of Illinois Urbana-Champaign, Computer Engineering Seminar, Urbana, IL, USA, 23 January 2007.
    - Xilinx Labs, San Jose, CA, USA, 16 June 2006.
    - Microsoft Research, Redmond, WA, USA, 12 June 2006.
    - Stanford University, Department of EE, Computer Architecture Seminar, Stanford, CA, USA, 7 June 2006.
    - MIPS Technologies, Mountain View, CA, USA, 6 June 2006.
    - IBM T.J. Watson Research Center, Yorktown Heights, NY, USA, 1 June 2006.
    - Carnegie Mellon University, Department of ECE, CALCM Seminar, Pittsburgh, PA, USA, 30 May 2006.
    - Hewlett-Packard Laboratories, Palo Alto, CA, USA, 4 May 2006.
    - University of California, San Diego, Department of Computer Science and Engineering, CA, USA, 21 April 2006.
    - University of Texas at Austin, Department of ECE, Guest Lecture for EE382N (Microarchitecture), 11-12 April 2006.

51. "Efficient Runahead Execution"
    - Advanced Micro Devices, Sunnyvale, CA, USA, May 2005.
    - Intel Barcelona Research Center, Barcelona, Spain, November 2005.
52. "Runahead Execution"
    - Advanced Micro Devices, Sunnyvale, CA, USA, May 2004.
    - Instituto de Informatica, Universidade Federal Rio Grande do Sul (UFRGS), Porto Alegre, Brazil, October 2004.
53. "Runahead Execution: A Mechanism to Approximate the Performance of Large Instruction Windows"
    - Enterprise Platforms Group, Intel Corporation, Santa Clara, CA, USA, August 2002.
    - Desktop Platforms Group, Intel Corporation, Hillsboro, OR, USA, August 2002.

Conference Talks (including some Keynote, Invited, and Plenary Speeches)

54. "Rethinking Memory System Design: Business As Usual in the Next Decade?" *Keynote talk at 2nd EAI International Conference on Future Access Enablers of Ubiquitous and Intelligent Infrastructures (FABULOUS)*, Belgrade, Serbia, October 2016.
55. "Rethinking Memory System Design" *Keynote talk at 27th International Symposium on Rapid System Prototyping (RSP)*, Pittsburgh, PA, USA, October 2016.
56. "Rethinking Memory System Design: Business As Usual in the Next Decade?" *Keynote talk at 2nd Workshop on Mobile System Technologies (MST)*, Milan, Italy, September 2016.
57. "Rethinking Memory System Design: Business As Usual in the Next Decade?" *Keynote talk at the First ARM Research Summit*, Cambridge, UK, September 2016.
58. "Large-Scale Study of In-the-Field Flash Failures," *Flash Memory Summit*, Santa Clara, CA, August 2016.
59. "ThyNVM: Software-Transparent Crash Consistency for Persistent Memory," *Flash Memory Summit*, Santa Clara, CA, August 2016.
60. "Rethinking Memory System Design," *Keynote talk at the ACM SIGPLAN International Symposium on Memory Management (ISMM)*, Santa Barbara, CA, 14 June 2016.
61. "The RowHammer Problem and Other Issues We May Face as Memory Becomes Denser," *Special invited talk and paper at Design Automation Conference (DAC)*, 9 June 2016.
62. "Reliability and Security Issues of DRAM and NAND Flash Scaling," *Invited talk at the Memory Reliability Forum at HPCA*, Barcelona, Spain, March 2016.
63. "Rethinking Memory System Design (along with Interconnects)," *Keynote talk at the 8th International Workshop on Network on Chip Architectures (NoCArc)*, Honolulu, Hawaii, December 2015.
64. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at the 5th IEEE Circuits and Systems Society Workshop (CASS)*, Porto Alegre, Brazil, October 2015.
65. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at the 27th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD)*, Florianopolis, Brazil, October 2015.
66. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at the 18th International Symposium on Computer Architecture and Digital Systems (CADS)*, October 2015.
67. "Read Disturb Errors in MLC NAND Flash Memory," *Flash Memory Summit*, Santa Clara, CA, August 2015.
68. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at SAMOS XV (15th International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation)*, Samos, Greece, July 2015.
69. "Rethinking Memory System Design (for Data-Intensive Computing)," *Special invited talk at ISC High Performance*, Frankfurt, Germany, July 2015.
70. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at 11th International Workshop on Data Management on Novel Hardware (DaMoN), held with SIGMOD*, Melbourne, Australia, June 2015.
71. "Rethinking Memory System Design (for Data-Intensive Computing)," *Keynote talk at the 4th Workshop on Irregular Applications: Architectures and Algorithms, held with Supercomputing (SC)*, New Orleans, LA, November 2014.
72. "Architecting and Exploiting Asymmetry in Multi-Core Architectures," *Invited talk at the International Workshop on Heterogeneous Computing Platforms, held with ICCAD*, San Jose, CA, November 2014.
73. "The Heterogeneous Block Architecture," *32nd IEEE International Conference on Computer Design*, Seoul, South Korea, October 2014.
74. "Error Analysis and Management for MLC NAND Flash Memory," *Flash Memory Summit*, Santa Clara, CA, August 2014.
75. "Rethinking Memory System Design (for Data-Intensive Computing)," *Plenary Talk at the Summer Supercomputing Academy*, Moscow, Russia, July 2014.
76. "Understanding and Overcoming Challenges of DRAM Refresh," *Extreme Scale Scientific Computing Workshop*, Moscow, Russia, June 2014.
77. "Rethinking Memory System Design for Data-Intensive Computing," *Keynote talk at the 25th IEEE International Conference on Application-specific Systems, Architectures and Processors*, Zürich, Switzerland, June 2014.
78. "Rethinking Memory/Storage System Design for Data-Intensive Computing," *Keynote talk at the 9th International Conference on Green, Pervasive and Cloud Computing*, Wuhan, China, May 2014.
79. "Rethinking Memory System Design for Data-Intensive Computing," *Keynote talk at the Industry-Academia Partnership Cloud Workshop*, Pittsburgh, PA, April 2014.

80. "Rethinking Memory System Design for Data-Intensive Computing," *Keynote talk at the Industry-Academia Partnership Cloud Workshop*, Mountain View, CA, December 2013.
81. "Memory Scaling: A Systems Architecture Perspective," *MemCon 2013*, Santa Clara, CA, August 2013.
82. "An Experimental Study of Data Retention Behavior in Modern DRAM Devices: Implications for Retention Time Profiling Mechanisms," *40th International Symposium on Computer Architecture*, Tel-Aviv, Israel, June 2013.
83. "A Case for Efficient Hardware-Software Cooperative Management of Storage and Memory," *5th Workshop on Energy-Efficient Design*, Tel-Aviv, Israel, June 2013.
84. "Memory Scaling: A Systems Architecture Perspective," *Invited talk at the 5th International Memory Workshop*, Monterey, CA, May 2013.
85. "Scalable Memory, Compute and Communication Architectures," *Industry-Academia Partnership Cloud Workshop*, Cambridge, MA, May 2013.
86. "Flash Correct-and-Refresh: Retention-Aware Error Management for Increased Flash Memory Lifetime," *30th International Conference on Computer Design*, Montreal, Quebec, Canada, September 2012.
87. "Bottleneck Identification and Scheduling in Multithreaded Applications," *17th International Conference on Architectural Support for Programming Languages and Operating Systems*, London, UK, March 2012.
88. "Data Marshaling for Multi-core Architectures," *37th International Symposium on Computer Architecture*, St. Malo, France, June 2010.
89. "Parallelism-aware Batch Scheduling: Enhancing both Performance and Fairness of Shared DRAM Systems," *35th International Symposium on Computer Architecture*, Beijing, China, June 2008.
90. "Stall-Time Fair Memory Access Scheduling," *40th International Symposium on Microarchitecture*, Chicago, IL, USA, December 2007.
91. "Memory Performance Attacks: Denial of Memory Service in Multi-Core Systems," *16th USENIX Security Symposium*, Boston, MA, USA, August 2007.
92. "Address-Value Delta Prediction," *38th International Symposium on Microarchitecture*, Barcelona, Spain, November 2005.
93. "Techniques for Efficient Processing in Runahead Execution Engines," *32nd International Symposium on Computer Architecture*, Madison, WI, USA, June 2005.
94. "Wrong Path Events and Their Application to Early Misprediction Detection and Recovery," *37th International Symposium on Microarchitecture*, Portland, OR, USA, December 2004.
95. "Cache Filtering Techniques to Reduce the Negative Impact of Useless Speculative Memory References on Processor Performance," *16th Symposium on Computer Architecture and High Performance Computing*, Foz do Iguacu, Brazil, October 2004.
96. "Runahead Execution: An Alternative to Very Large Instruction Windows for Out-of-order Processors," *9th International Conference on High Performance Computer Architecture*, Anaheim, CA, USA, February 2003.

Panel Talks and Discussions

97. "It's time: top-tier academic computer system venues should mandate authors to make their data and code publicly available upon publication" *Panel at the 20th International Conference on Architectural Support for Programming Languages and Operating Systems*, Istanbul, Turkey, March 2015.
98. "Memory and System Balance," *Panel at 4th Workshop on Irregular Applications: Architectures and Algorithms, held with Supercomputing (SC)*, New Orleans, LA, November 2014.
99. "Meeting the Future Needs of the Data Center," *Panel at the Industry-Academia Partnership Cloud Workshop*, Cambridge, MA, May 2013.

Teaching Experience

(Please visit `https://people.inf.ethz.ch/omutlu/teaching.html` for online course materials – free for all my courses).
(Please visit `https://www.youtube.com/user/cmu18447/` for online lecture videos for my courses.)

ETH Zürich, Computer Science Department, Co-Instructor for Graduate Seminar on Hardware Acceleration for Data Processing, ***Fall 2016***
Carnegie Mellon University, ECE Department, Instructor for Undergraduate Computer Architecture Course ECE-447, ***Spring 2012, 2013, 2014, 2015***

- Instructor rating: 4.12/5.0 (S12, 34/47), 4.33/5.0 (S13, 21/30), 4.55/5.0 (S14, 33/37), 4.54/5.0 (S15, 24/30)
- Spring 2015 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece447/s15/`
- Spring 2014 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece447/s14/`
- Spring 2013 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece447/s13/`

Carnegie Mellon University, ECE Department, Instructor for Graduate Computer Architecture Course CS/ECE-740, ***Fall 2010, 2011, 2013, 2015***

- Instructor rating: 4.42/5.0 (F10, 43/53), 4.7/5.0 (F11, 19/24), 4.29/5.0 (F13, 28/33), 4.58/5.0 (F15, 12/18)
- Fall 2013 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece740/f15/`
- Fall 2013 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece740/f13/`
- Fall 2011 online course materials: `http://www.ece.cmu.edu/~ece740/f11/`
- Fall 2010 online course materials: `http://www.ece.cmu.edu/~ece740/f10/`

Carnegie Mellon University, ECE Department, Instructor for Parallel Computer Architecture Course ECE-742, ***Spring 2010, 2011, Fall 2012, 2014***

- Instructor rating: 4.44/5.0 (S10, 18/20), 4.71/5.0 (S11, 7/10), 4.22/5.0 (F12, 9/14), 5.00/5.00 (F14, 5/5)
- Fall 2014 online course materials, including lecture videos: `http://www.ece.cmu.edu/~ece742/f14/`

- Fall 2012 online course materials, including lecture videos: http://www.ece.cmu.edu/~ece742/f12/
- Spring 2011 online course materials: http://www.ece.cmu.edu/~ece742/2011spring/

Carnegie Mellon University, ECE Department, Instructor for Advanced Computer Architecture Course ECE-741, ***Spring 2009***

- Instructor rating based on student evaluations: 4.6/5.0 (25/35 students responded)

University of Texas at Austin, ECE Department, Teaching Assistant for Senior-level Computer Architecture Course EE360N, ***Spring 2001, 2003***

- Instructor rating: 4.8/5.0 (S01, 30/50), 4.7/5.0 (S03, 59/70)

University of Texas at Austin, ECE Department, Teaching Assistant for Freshman-level Intro. to Computing Course EE306, ***Fall 2000***

- Instructor rating based on student evaluations: 4.7/5.0 (35/55 students responded)

Supervised Students and Trainees

(Please visit http://www.ece.cmu.edu/~safari/people.html for a partial list of supervised students).

PhD Alumni

1. Lavanya Subramanian, "Providing High and Controllable Performance in Multicore Systems Through Shared Resource Management," CMU ECE, defended April 2015, currently at Intel Labs, Santa Clara, CA, USA.
2. Yoongu Kim, "Architectural Techniques to Enhance DRAM Scaling," CMU ECE, defended May 2015, currently at Software Robotics, Boston, MA, USA.
3. Donghyuk Lee, "Reducing DRAM Latency at Low Cost by Exploiting Heterogeneity," CMU ECE, defended December 2015, currently at Nvidia Research, Austin, TX, USA
4. Vivek Seshadri, "Simple DRAM and Virtual Memory Abstractions to Enable Highly Efficient Memory Subsystems," CMU CS, defended March 2016, currently at Microsoft Research, Bangalore, India.
5. Gennady Pekhimenko, "Practical Data Compression for Modern Memory Hierarchies," CMU CS, defended July 2016, currently Assistant Professor at the University of Toronto CS Department, Canada.

Post-doctoral Researcher Alumni

1. Samira Khan, CMU ECE, September 2012 to September 2015, currently Assistant Professor at the University of Virginia.
2. Saugata Ghose, CMU ECE, September 2014 to September 2016, currently Special Faculty Member at Carnegie Mellon University.

Current PhD Students

1. Mohammed Alser, Bilkent CS, since 2016 (co-advised)
2. Rachata Ausavarungnirun, CMU ECE, since 2010
3. Amirali Boroumand, CMU ECE, since 2014
4. Lukas Breitwieser, ETH Zürich D-INFK, since February 2017 (hosted at CERN)
5. Kevin Chang, CMU ECE, since 2011
6. Hasan Hassan, ETH Zürich D-INFK, since December 2016
7. Kevin Hsieh, CMU ECE, since 2014 (co-advised)
8. Jeremie Kim, CMU ECE, since 2015
9. Yang Li, CMU ECE, since 2013
10. Yixin Luo, CMU CSD, since 2012
11. Justin Meza, CMU ECE, since 2010 (on leave)
12. Minesh Patel, CMU ECE, since 2015
13. Ivan Puddu, ETH Zürich D-INFK, since February 2017 (co-advised)
14. Damla Senol, CMU ECE, since 2015 (co-advised)
15. Nandita Vijaykumar, CMU ECE, since 2013 (co-advised)
16. Hongyi Xin, CMU CSD, since 2011

Current Post-Doctoral Researchers

1. Arash Tavakkol, ETH Zürich D-INFK, since August 2016.
2. Yaohua Wang, ETH Zürich D-INFK, since November 2016.
3. Lois Orosa, ETH Zürich D-INFK, since January 2017.

Current Masters Research Students

1. Nika Mansouri Ghiasi, ETH Zürich D-ITET, since September 2016.
2. Ashish Shrestha, CMU ECE

Current Undergraduate Research Students

1. Alexander Breuss, ETH Zürich D-INFK
2. Raghav Gupta, CMU ECE
3. Evan Lee, CMU ECE
4. Sunny Nahar, CMU CSD

Past Undergraduate Research Students at CMU (incomplete)
Hitesh Arora (IIT Guwahati), Sean Buckley, Rui Cai, Albert Cho, Jared Choi, Vidushi Dadu, Parag Dixit, John Emmons (Drake), Arnab Ghosh (IIT Kanpur), John Greth, Matthias Grundmann (Karlsruhe Inst of Tech), Raghav Gupta, Arjun Hans, Yuchen Hao (Tsinghua), Rachael Harding (grad. Dec 2010), Tyler Huberty, Jeremie Kim, Ji Hye Lee, Tianshi Li (Peking), Jason Lin, Connor Maines, Tom Mullins, Sunny Nahar, Naman Nandan, Gregory Nazario, Karthic Palaniappan, Harsha Rastogi (BITS Pilani), Eddie Sears, Kevin Woo, Weikun Yang (Peking), Samihan Yedkar, Xiangyao Yu (Tsinghua), Richard Zhu

Past Masters Research Students at CMU (incomplete)
Ameya Ambardekar, Abhishek Bhowmick (IIT Bombay), Chris Craik (grad. Aug 2011), Chris Fallin (Aug 2013), Mughda Satish Dharkar, Hasan Hassan (TOBB ETU), Ben Jaiyen (Dec 2012), Abhijith Kashyap (May 2016), Jamie Liu (Dec 2012), Huimin Yang, HanBin Yoon

Past High School Research Students at CMU (incomplete)
Aaron Cutright (Pittsburgh Allderdice High School), Steven Barash (Pittsburgh Allderdice High School), Nolan Dickey (Pittsburgh Allderdice High School)

Past Visiting Researchers at CMU (incomplete)
Jongmoo Choi (Dankook Univ.), Hiroyuki Usui (Toshiba), Rui Wang (Beihang).

Past Interns (incomplete)
Rishi Agarwal (IIT-Kanpur), Kypros Constantinides (Michigan), Alejandro Cornejo (MIT), Reetuparna Das (Penn State), Eiman Ebrahimi (UT-Austin), Mohammad Fattah (Turku), Boris Grot (UT-Austin), Engin Ipek (Cornell), Jamie Jablin (Brown), Jose Joao (UT-Austin), Yanjing Li (Stanford), Youyou Lu (Tsinghua), Gregory Nazario (CMU), Arthur Perais (INRIA), Xuehai Qian (Illinois), Jinglei Ren (Tsinghua), Hui Wang (Beihang), Ying Wang (ICT-CAS), Gulay Yalcin (BSC), Xiangyao Yu (Tsinghua), Jishen Xhao (Penn State)

Ph.D. Thesis Committee Member (incomplete)
Akkarit Sangpetch (CMU), Asit Mishra (Penn State), Chen-Ling Chou (CMU), Reetuparna Das (Penn State), Eiman Ebrahimi (UT-Austin), Michael Ferdman (CMU), Boris Grot (UT-Austin), Engin Ipek (Cornell), Lei Jin (Pitt), Jose Joao (UT-Austin), Adwait Jog (Penn State), Onur Kayiran (Penn State), Karthik Lakshmanan (CMU), Chang Joo Lee (UT-Austin), Michel Papamichael (CMU), Tim Rogers (UBC), Olatunji Ruwase (CMU), Marek Telgarsky (CMU), Yu Cai (CMU), Hyoseung Kim (CMU), Jishen Zhao (Penn State)

Professional Service

Technical Journal Editorships
Associate Editor, ACM Transactions on Architecture and Code Optimization (TACO), Feb. 2010 - Present.
Associate Editor, ACM Transactions on Storage (TOS), Sep. 2016 - Present.
Editorial Board Member, IEEE Micro, March 2016 - Present.
Editorial Board Member, International Journal of Supercomputing Frontiers and Innovations. Nov. 2014 - Present.
Editorial Board Member, International Journal of Big Data Intelligence (IJBDI), Sep. 2014 - Present.
Co-Guest Editor, IEEE Micro special issue (May/June 2008) on "The Interaction of Computer Architecture and Operating Systems in the Many-core Era," May/June 2008.
Co-Guest Editor, IEEE Micro special issue (Jan/Feb 2011) on "Micro's Top Picks from Computer Architecture Conferences," Jan/Feb 2011.

Technical Conference and Award Committee Chairmanships
MICRO Steering Committee Co-Chair, 2017-onwards.
MICRO Test of Time Award Committee Chair, 2015-Present.
IEEE TCCA Young Computer Architect Award Committee Chair, 2017-Present.
ICS Program Co-Chair, ACM International Conference on Supercomputing, 2016.
NVMSA Program Co-Chair, IEEE International Conference on Non-Volatile Memory Systems and Applications, 2016.
HiPEAC Program Chair, 10th International Conference on High-Performance and Embedded Architectures and Compilers, 2015.
VLSI-SoC Track Co-Chair, 21st IFIP/IEEE International Conference on Very Large Scale Integration, 2013.
MICRO Program Chair, 45th ACM/IEEE International Symposium on Microarchitecture, 2012.
MSPC Program Chair, ACM SIGPLAN Workshop on Memory System Performance and Correctness, 2012.
IEEE Micro Top Picks Selection Committee Co-Chair, IEEE Micro Special Issue on Top Picks from Computer Architecture Conferences, 2011.
IISWC Program Co-Chair, 4th IEEE International Symposium on Workload Characterization (IISWC), 2008.

Technical Conference and Award Committee Memberships
MICRO Steering Committee Member, 2013-Present.

MICRO Test of Time Award Committee Member, 2014-Present.
ICS Steering Committee Member, 2016-Present.
IEEE TCCA Young Computer Architect Award Committee Member, 2016-Present.
IEEE Micro Top Picks Selection Committee Member, IEEE Micro Special Issue on Top Picks from Computer Architecture Conferences, 2017, 2015, 2013, 2012, 2011, 2010, 2009.
MICRO Program Committee Member, International Symposium on Microarchitecture, 2017, 2015, 2014, 2012, 2008, 2007 (Did not accept invitation in 2013, 2011, 2010 due to paper submission or acceptance limits).
MICRO External Review Committee Member, International Symposium on Microarchitecture, 2016.
ISCA Program Committee Member, International Symposium on Computer Architecture, 2017, 2010, 2008 (Did not accept invitation in 2016, 2015 due to paper submission or acceptance limits).
ISCA External Review Committee Member, International Symposium on Computer Architecture, 2016, 2015.
PLDI Program Committee Member, ACM SIGPLAN conference on Programming Language Design and Implementation, 2017.
ASPLOS Program Committee Member, Intl. Conf. on Architectural Support for Programming Lang. and Operating Systems, 2016, 2012, 2011, 2009.
ASPLOS External Review Committee Member, Intl. Conf. on Architectural Support for Programming Lang. and Operating Systems, 2014.
HPCA Program Committee Member, International Symposium on High Performance Computer Architecture, 2017, 2015, 2012, 2010, 2009.
HPCA External Review Committee Member, International Symposium on High Performance Computer Architecture, 2016.
DSN Program Committee Member, IEEE/IFIP International Conference on Dependable Systems and Networks, 2016.
DAC Program Committee Member, Design Automation Conference, 2016, 2015, 2014.
DATE Program Committee Member, Design Automation Test in Europe Conference, 2016.
PACT Program Committee Member, International Conference on Parallel Architectures and Compilation Techniques, 2013.
PACT External Review Committee Member, International Conference on Parallel Architectures and Compilation Techniques, 2016, 2014.
ICS Program Committee Member, ACM International Conference on Supercomputing, 2017, 2016.
HotStorage Program Committee Member, USENIX Workshop on Hot Topics in Storage and File Systems, 2017.
ISMM Program Committee Member, International Symposium on Memory Management, 2013.
ISMM External Review Committee Member, International Symposium on Memory Management, 2016, 2015.
ICAC Program Committee Member, International Conference on Autonomic Computing, 2013.
ICCD Program Committee Member, IEEE International Conference on Computer Design, 2014, 2013, 2012, 2011, 2010, 2009.
IISWC Program Committee Member, IEEE International Symposium on Workload Characterization, 2014, 2011, 2009, 2008.
IISWC Steering Committee Member, IEEE International Symposium on Workload Characterization, 2008-Present.
MSPC Program Committee Member, ACM SIGPLAN Workshop on Memory Systems Performance and Correctness, 2012, 2008
IGCC Program Committee Member, International Green Computing Conference, 2013, 2012.
ASAP Program Committee Member, International Conference on Application-specific Systems, Architectures and Processors, 2013.
SBAC-PAD Program Committee Member, International Symposium on Computer Architecture and High Performance Computing, 2016, 2013.
NVMSA Program Committee Member, IEEE International Conference on Non-Volatile Memory Systems and Applications, 2017, 2016.
MEMSYS Program Committee Member, International Symposium on Memory Systems, 2017.

Technical Workshop and Tutorial Committee Memberships and Chairmanships

The Memory Forum Co-organizer, 2014. (held with ISCA)
Future Memory Systems Workshop Organizer (held at Carnegie Mellon University), May 2014.
First ASPLOS Doctoral Workshop Program Committee Co-Chair, 2012.
FCRP Memory Cross-Cut Workshop Co-organizer, 2011.
WIOSCA Co-organizer, Workshop on the Interaction between Operating Systems and Computer Architecture, 2007-2010. (Held with ISCA).
JILP Memory Scheduling Championship Program Committee Member, 2012. (held with ISCA)
ALCHEMY Program Committee Member, Architecture, Languages, Compilation and Hardware support for Emerging ManYcore systems, 2014.
WEED Program Committee Member, Workshop on Energy-Efficient Design, 2013, 2010. (held with ISCA)
MoBS Program Committee Member, Workshop on Modeling, Benchmarking, and Simulation, 2010. (held with ISCA)
PESPMA Program Committee Member, Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures, 2010, 2009. (held with ISCA)
CATARS Program Committee Member, Workshop on Compiler/Architectural Techniques for Application Reliability/Security, 2009, 2008. (held with DSN)
WDA Program Committee Member, Workshop on Dependable Architectures, 2008, 2006. (held with MICRO)
RAAW Program Committee Member, Reconfigurable and Adaptive Architecture Workshop, 2007. (held with MICRO)

Technical Reviewer for Journals (incomplete)

ACM Transactions on Architecture and Code Optimization, ACM Transactions on Design Automation of Electronic Systems, ACM Transactions on Embedded Computing Systems, Communications of the ACM, IEEE Computer, IEEE Micro, IEEE Transactions on Computers, IEEE Transactions on Computer Aided Design, IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Reliability, IEEE Transactions on Nanotechnology, IEEE Transactions on VLSI Systems, IEEE Transactions on Circuits and Systems, IEEE Computer Architecture Letters, HiPEAC Journal, Journal of Parallel and Distributed Computing, ACM/IEEE Transactions on Networking, Nature Communications.

Technical Reviewer for Conferences (incomplete)
ISCA, MICRO, HPCA, ASPLOS, Usenix Security Symposium, HotOS, DAC, DATE, DSN, ICS, PACT, RTSS, IPDPS, ISPASS, HiPEAC, Euro-Par, SBAC-PAD, WASP, SBCCI, IGCC, MSPC, IISWC.

Expert Reviewer for Research Proposals (incomplete)
NSF Review Panel Participant, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014, 2015.
DOE Review Panel Participant, 2010.
Reviewer for Research Proposals in Australia, Belgium, European Union, Canada, Norway, Switzerland, 2013, 2014, 2015, 2016, 2017.
Microsoft Research Breakthrough Research Grant Proposal Reviewer, 2007.
Microsoft Research New Faculty Fellowship Candidate Reviewer, 2006, 2007.
Microsoft Research Reviewer for Miscellaneous Requests for Proposals, 2007, 2008.
Microsoft Research PhD Fellowship Candidate Reviewer, 2006, 2007, 2008.

Departmental Committee Memberships
ETH D-INFK: Doctoral Studies Committee (2016-Present), Doctoral Admissions Committee (2016-Present)
CMU ECE: Faculty Search Committee (2011-2016), Admissions Committee (2011-2014), Seminar Committee (2010-2011)
CMU CSD: ACM Doctoral Dissertation Award Committee (Fall 2012), Faculty Hiring Committee (2010)

Other Committee Memberships
Local Arrangements Chair, ASPLOS 2010.
Publicity Chair, HiPEAC 2017, HiPEAC 2016, ASPLOS 2015, HPCA 2014, HPCA 2013, HPCA 2010, IISWC 2009, ASPLOS 2008.
Publications Chair, ICS 2007.

Open Source Educational and Research Artifacts

Lecture Videos and Course Materials
Please visit `https://people.inf.ethz.ch/omutlu/teaching.html` for online course materials.
Please visit `https://www.youtube.com/user/cmu18447` for online computer architecture lecture videos.

Source Code Releases
Please visit `http://www.ece.cmu.edu/~safari/tools.html` and `https://github.com/CMU-SAFARI`.

Professional Memberships

Senior Member of IEEE and ACM
Member of IEEE Computer Society, ACM SIGARCH, ACM SIGMICRO
Member of Eta Kappa Nu Electrical Engineering Honor Society and Tau Beta Pi Engineering Honor Society, since 1998