A Case for Small Row Buffers in Non-Volatile Main Memories

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1 Motivation / Background

DRAM devices have destructive reads and buffer large rows of cells to reduce cost

System trends reduce the amount of data accessed from buffer (<10% for some 8-core systems)

- Due to contention among many cores
- Due to data mapping schemes

Buffering large rows is energy-inefficient

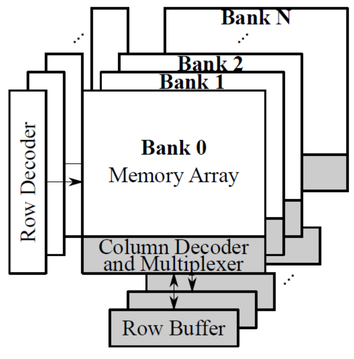
2 Enabling Small Row Buffers

Non-volatile memories (NVMs) have non-destructive reads

- Leverage to reduce row buffer size
- We examine the system-level trade-offs of reducing row buffer size in NVMs

Swap row buffer and column mux in NVM datapath

Read an entire NVM row, but select and buffer only a portion of its data



3 Evaluation

8-cores, DDR3-1066 simulator; modified for NVM timing and energy; 31 workloads

(Relative to DRAM)	PCM	STT-RAM
Energy (Read/Write)	2x/100x	0.5x/1x
Latency (Read/Write)	5x/10x	1x/1x

4 Results

47/67% less main memory energy for PCM/ STT-RAM with 64B row buffer size

Small rows achieve similar performance to large rows due to low system row locality

Better performance with similar technology parameters (STT-RAM) due to relaxed timing constraints compared to DRAM